STA505

40V 3.5A QUAD POWER HALF BRIDGE

1 FEATURES

- MULTIPOWER BCD TECHNOLOGY
- MINIMUM INPUT OUTPUT PULSE WIDTH DISTORTION
- 200mΩ R_{dsON} COMPLEMENTARY DMOS OUTPUT STAGE
- CMOS COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- THERMAL WARNING OUTPUT
- UNDER VOLTAGE PROTECTION

Figure 1. Package

PowerSO36

Table 1. Order Codes

Part Number	Package
STA505	PowerSO36
STA50513TR	in Tape & Reel

2 DESCRIPTION

STA505 is a monolithic quad half bridge stage in Multipower BCD Technology. The device can be used as dual bridge or reconfigured, by connecting CONFIG pin to Vdd pin, as single bridge with double current capability, and as half bridge (Binary mode) with half current capability.

The device is particularly designed to make the output stage of a stereo All-Digital High Efficiency (DDX™) amplifier capable to deliver 50 + 50W @ THD = 10% at V_{cc} 30V output power on 8Ω load and 80W @ THD = 10% at V_{cc} 36V on 8Ω load in single BTL configuration. The input pins have threshold proportional to V_L pin voltage.

Figure 2. Audio Application Circuit (Dual BTL)Pin Description

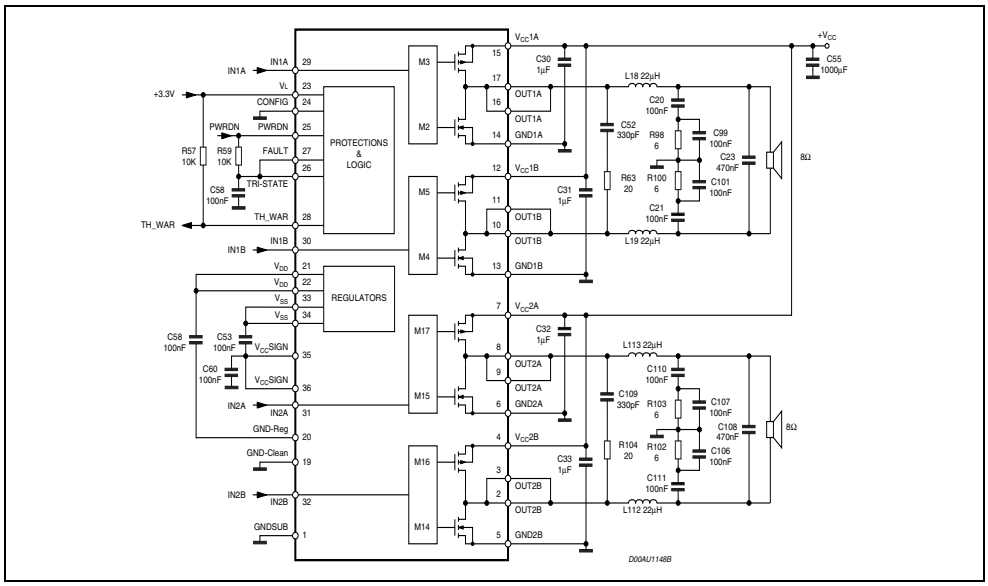


Table 2. Pin Function

N°	Pin	Description
1	GND-SUB	Substrate ground
2 ; 3	OUT2B	Output half bridge 2B
4	Vcc2B	Positive Supply
5	GND2B	Negative Supply
6	GND2A	Negative Supply
7	Vcc2A	Positive Supply
8 ; 9	OUT2A	Output half bridge 2A
10 ; 11	OUT1B	Output half bridge 1B
12	Vcc1B	Positive Supply
13	GND1B	Negative Supply
14	GND1A	Negative Supply
15	Vcc1A	Positive Supply
16 ; 17	OUT1A	Output half bridge 1A
18	NC	Not connected
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator Vdd
21 ; 22	Vdd	5V Regulator referred to ground
23	VL	High logical state setting voltage
24	CONFIG	Configuration pin
29	IN1A	Input of half bridge 1A
25	PWRDN	Stand-by pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
33 ; 34	Vss	5V Regulator referred to +Vcc
35 ; 36	Vcc Sign	Signal Positive Supply

Table 3. Functional Pin Status

PIN NAME	Logical value	IC -STATUS
FAULT	0	Fault detected (Short circuit, or Thermal ..)
FAULT (*)	1	Normal Operation
TRI-STATE	0	All powers in Hi-Z state
TRI-STATE	1	Normal operation
PWRDN	0	Low absorpion
PWRDN	1	Normal operation
THWAR	0	Temperature of the IC =130C
THWAR(*)	1	Normal operation
CONFIG	0	Normal Operation
CONFIG(**)	1	OUT1A=OUT1B ; OUT2A=OUT2B (IF IN1A = IN1B; IN2A = IN2B)

(*) : The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.
(**): To put CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (Vdd)

Figure 3. Pin Connection

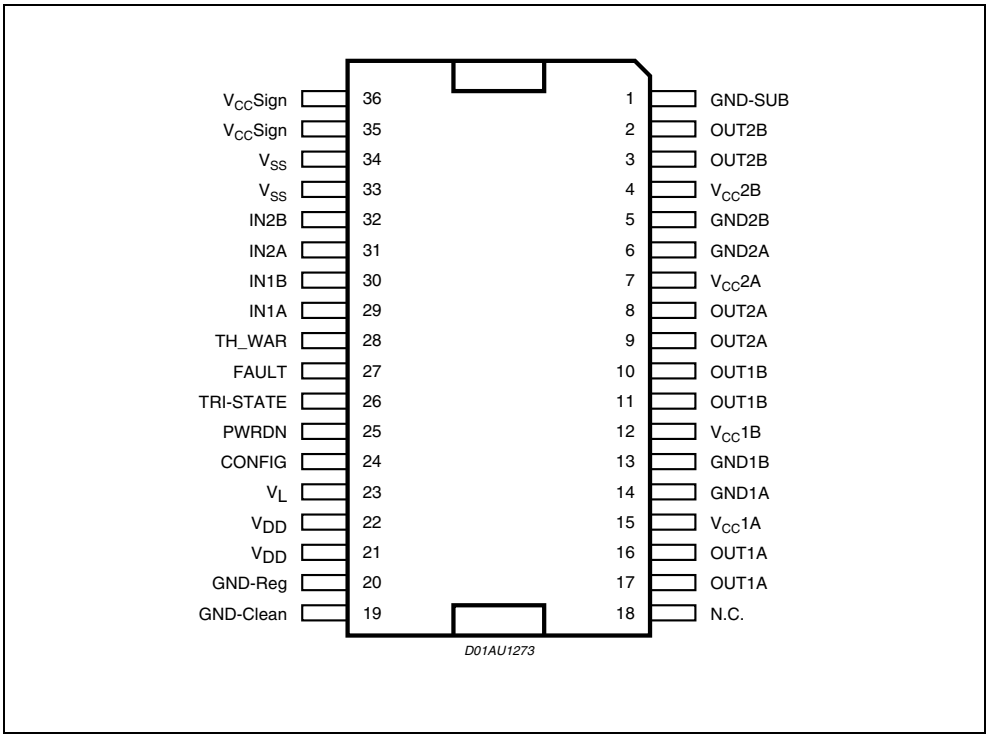


Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Pin 4,7,12,15)	40	V
V_{max}	Maximum Voltage on pins 23 to 32	5.5	V
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

Table 5. Thermal Data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{j\text{-}case}$	Thermal Resistance Junction to Case (thermal pad)			2.5	°C/W
T_{jSD}	Thermal shut-down junction temperature		150		°C
T_{warn}	Thermal warning temperature		130		°C
t_{hSD}	Thermal shut-down hysteresis		25		°C

Table 6. Electrical Characteristcs (V_L = 3.3V; V_{cc} = 30V; T_{amb} = 25°C; f_{sw} = 384Khz; unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power Pchannel/Nchannel MOSFET RdsON	Id=1A;		200	270	mΩ
I_{dss}	Power Pchannel/Nchannel leakage Idss	Vcc=35V			50	µA
g_N	Power Pchannel RdsON Matching	Id=1A	95			%
g_P	Power Nchannel RdsON Matching	Id=1A	95			%
Dt_s	Low current Dead Time (static)	see test circuit no.1; see fig. 1		10	20	ns
Dt_d	High current Dead Time (dinamic)	L=22µH; C = 470nF; Rl = 8 Ω Id=3.5A; see fig. 3			50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load			100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load; as fig.1;			25	ns
t_f	Fall time	Resistive load; as fig. 1;			25	ns
V_{CC}	Supply voltage operating voltage		10		36	V
$V_{IN\text{-}High}$	High level input voltage				$V_L/2$ +300mV	V
$V_{IN\text{-}Low}$	Low level input voltage		$V_L/2$ - 300mV			V
$I_{IN\text{-}H}$	High level Input current	Pin voltage = V_L		1		µA
$I_{IN\text{-}L}$	Low level input current	Pin voltage = 0.3V		1		µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{PWRDN-H}$	High level PWRDN pin input current			35		µA
V_{Low}	Low logical state voltage VLow (pin PWRDN, TRISTATE) (note 1)	V_L = 3.3V	0.8			V
V_{High}	High logical state voltage VHigh (pin PWRDN, TRISTATE) (note 1)	V_L = 3.3V			1.7	V
$I_{VCC-PWRDN}$	Supply current from Vcc in Power Down	PWRDN = 0			3	mA
I_{FAULT}	Output Current pins FAULT -TH-WARN when FAULT CONDITIONS	Vpin = 3.3V		1		mA
$I_{VCC-hiz}$	Supply current from Vcc in Tri-state	Tri-state=0		22		mA
I_{VCC}	Supply current from Vcc in operation both channel switching)	Input pulse width = 50% Duty; Switching Frequency = 384KHz; No LC filters;		50		mA
I_{VCC-q}	Isc (short circuit current limit) (note 2)		3.5	6	8	A
V_{UV}	Undervoltage protection threshold			7		V
t_{pw-min}	Output minimum pulse width	No Load	70		150	ns

Table 7.

Notes: 1. The following table explains the VLow, VHigh variation with V_L

V_L	VLow min	VHigh max	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Note 2: See relevant Application Note AN1994

Table 8. Logic Truth Table (see fig. 5)

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	OUTPUT MODE
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 4. Test Circuit.

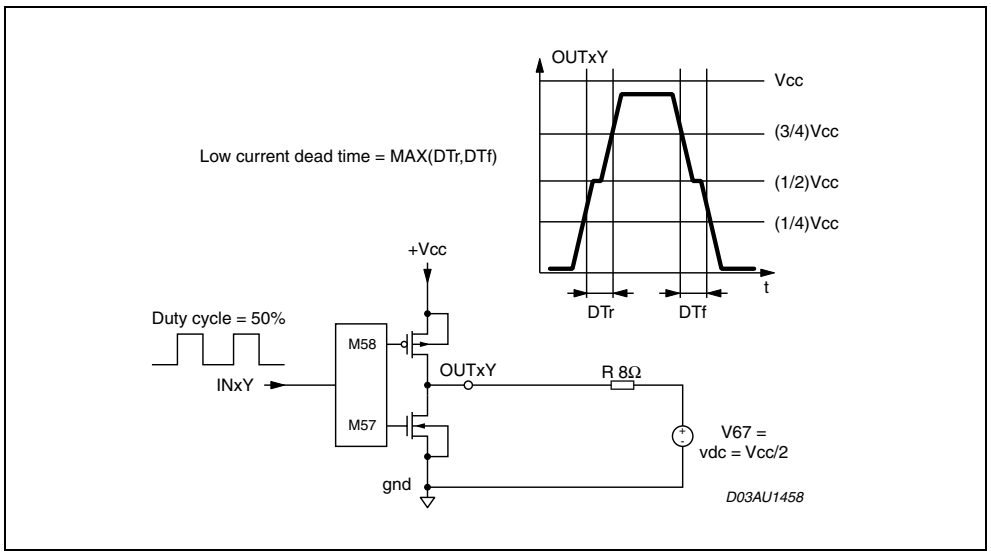


Figure 5.

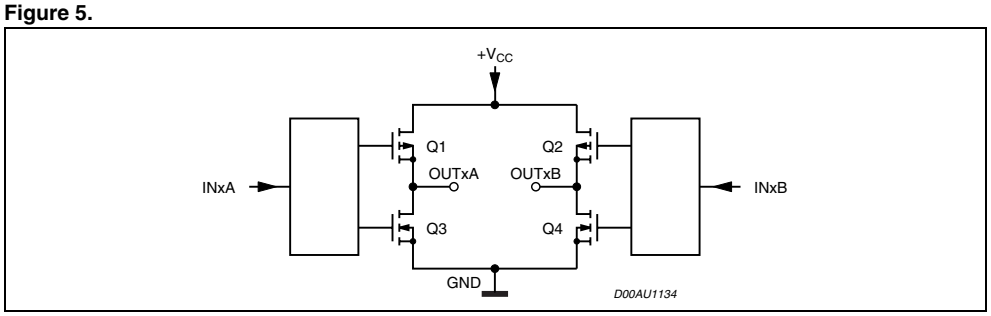


Figure 6.

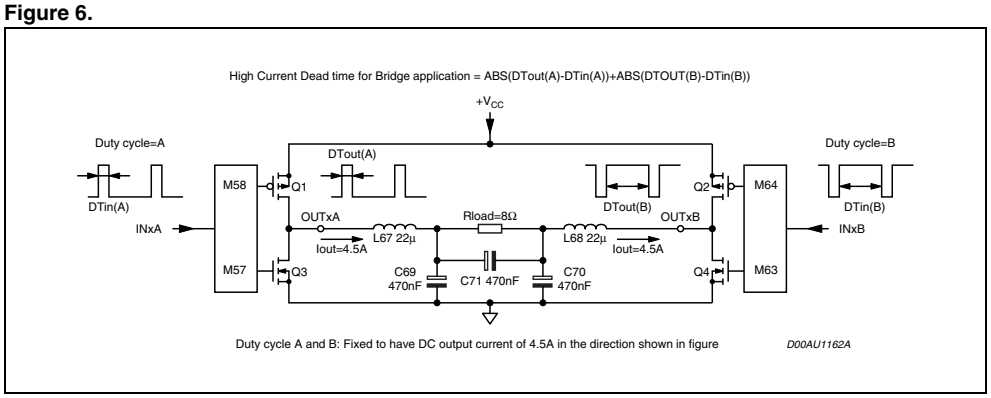
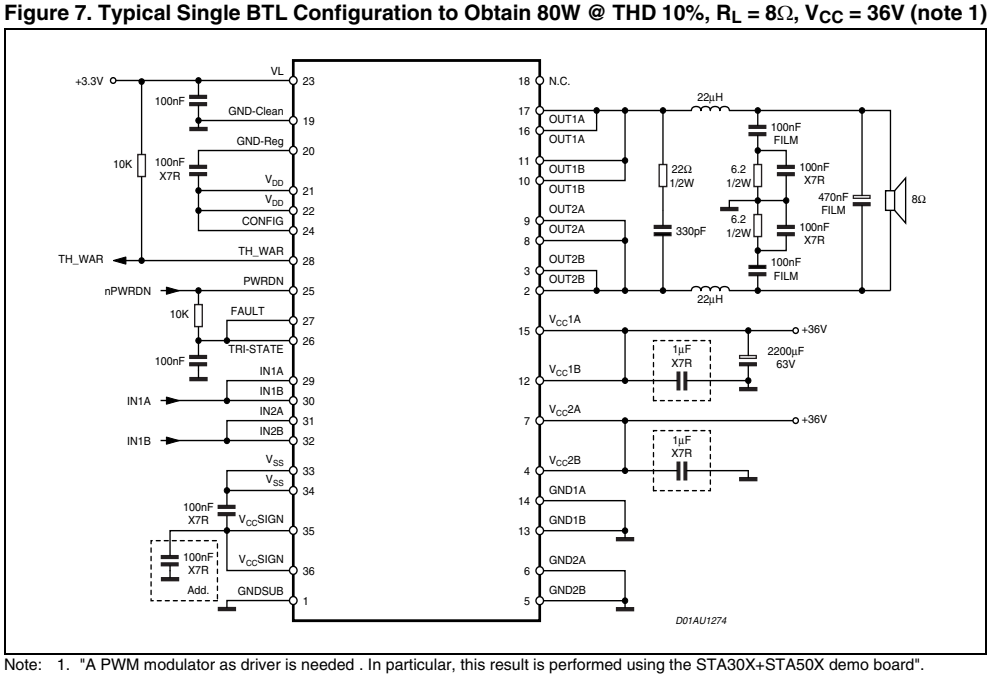
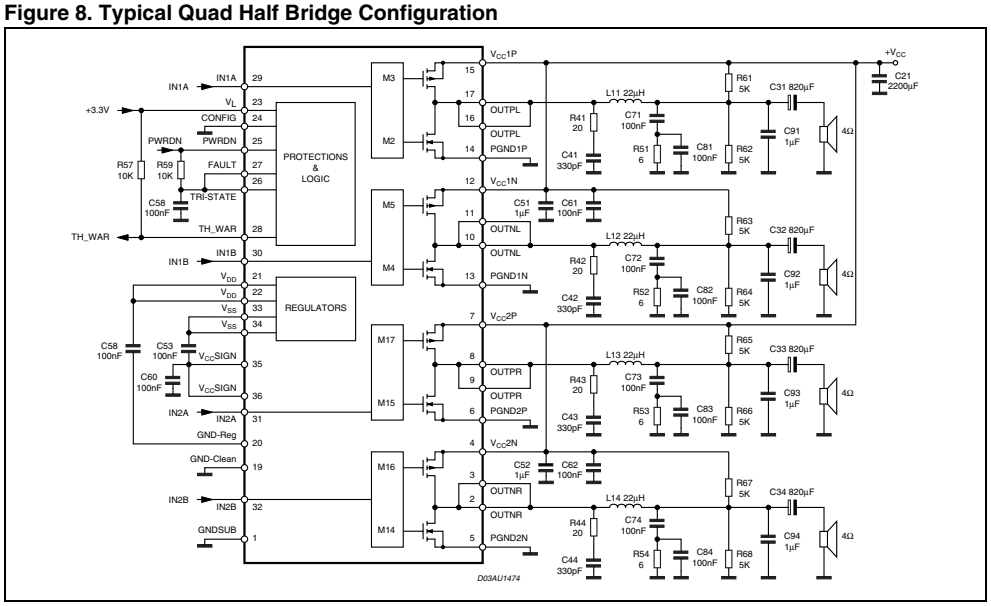


Figure 7. Typical Single BTL Configuration to Obtain 80W @ THD 10%, R_L = 8Ω, V_{CC} = 36V (note 1)



Note: 1. "A PWM modulator as driver is needed . In particular, this result is performed using the STA30X+STA50X demo board".

Figure 8. Typical Quad Half Bridge Configuration



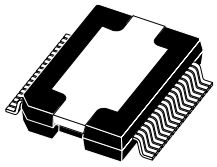
For more information refer to the application notes AN1456 and AN1661

Figure 9. Power SO36 (Slug up) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.43	0.128		0.135
A2	3.1		3.2	0.122		0.126
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0.030		-0.040	0.0011		-0.0015
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.075	0		0.003
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N			10°			10°
s			8 °			8°

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.

OUTLINE AND MECHANICAL DATA



PowerSO36 (SLUG UP)

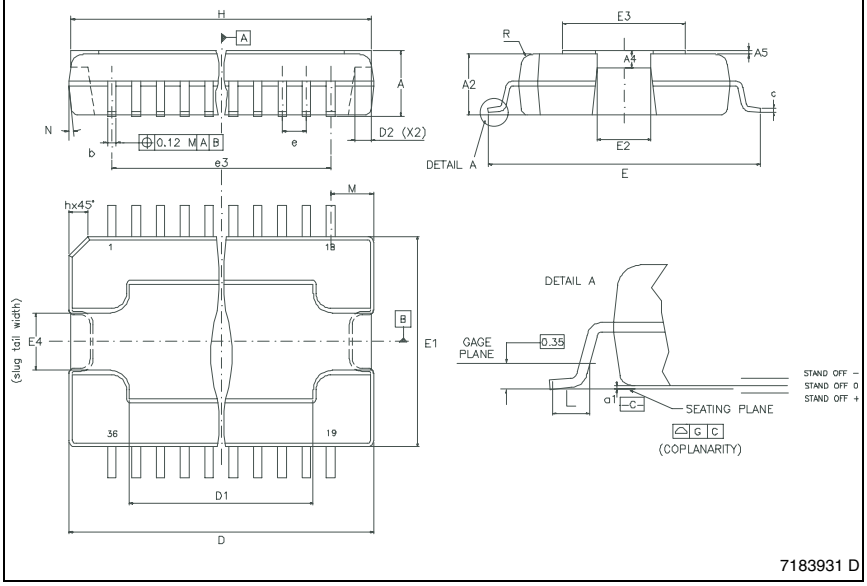


Table 9. Revision History

Date	Revision	Description of Changes
December 2003	8	First Issue in EDOCS DMS
June 2004	9	Note 2: See relevant Application Note AN1994
November 2004	10	Changed Vcc in Electrical Characteristics from 9 min to 10 min