DATA SHEET

SAA5254
Integrated VIP and teletext decoder (IVT1.1X)

Preliminary specification
Supersedes data of July 1993
File under Integrated Circuits, IC02

1996 Nov 07

Philips
Semiconductors

PHILIPS

Integrated VIP and teletext decoder (IVT1.1X)

SAA5254

FEATURES

- Complete teletext decoder including page memory and FASTEXT links in a 40-pin DIP package
- Automatic processing of extension packet 26 for widest possible language decoding. All our standard language options can be available, and language option is readable via I²C-bus
- 100% hardware compatible with the SAA5244A; plug-in replacement and extra market
- 100% hardware compatible with the SAA5244A, except if the special OSD symbols were used with the SAA5244A, except ROM identification number
- The device is pin-aligned with the other members of the new Philips teletext decoder family, i.e. SAA5280 and the SAA5249, making one hardware solution for the full range
- Low software overhead for the control microprocessor
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Separate text and video signal quality detectors.

DESCRIPTION

The Integrated VIP and Teletext decoder (IVT1.1X) is designed to decode 625-line based World System Teletext transmissions. This single-chip teletext decoder hardware is based on the SAA5244A with which it is completely compatible.

Like the SAA5244A the device contains all the hardware necessary to decode the teletext, but the SAA5254 also contains extra hardware to process the extension packet 26 characters automatically, extending the markets to which the TV chassis can be shipped and opening the possibility of many more language options.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5254P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	90	120	mA
V_{sync}	sync voltage amplitude	0.1	0.3	0.6	V
V_{video}	video voltage amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

BLOCK DIAGRAM

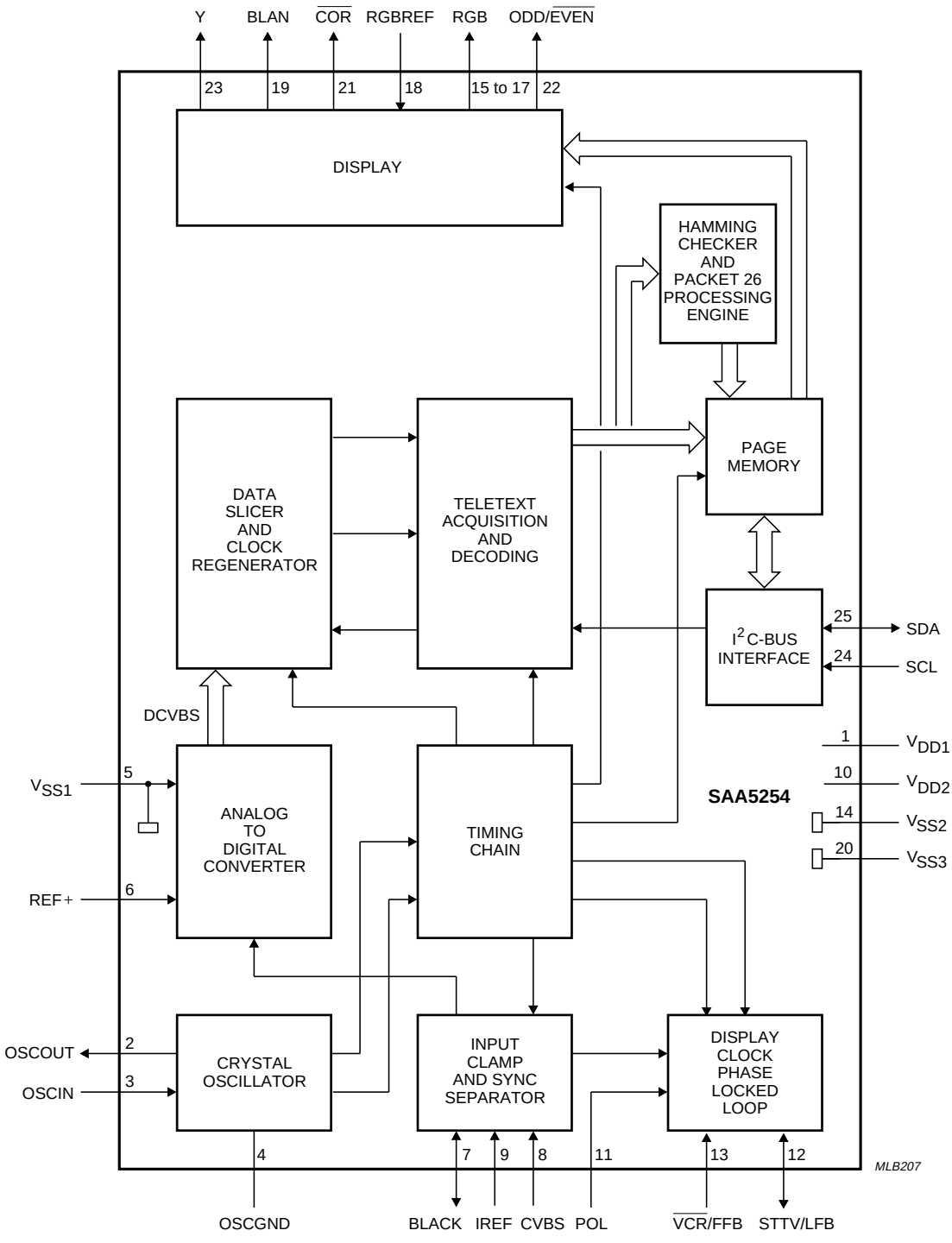


Fig.1 Block diagram; SOT129 (DIP40).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD1}	1	+5 V supply 1
OSCOUT	2	27 MHz crystal oscillator output
OSCIN	3	27 MHz crystal oscillator input
OSCGND	4	0 V crystal oscillator ground
V_{SS1}	5	0 V ground 1
REF+	6	Positive reference voltage for the ADC. This pin should be connected to +5 V.
BLACK	7	Video black level storage pin, connected to ground via a 100 nF capacitor.
CVBS	8	Composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
IREF	9	Reference current input pin, connected to ground via a 27 kΩ resistor.
V_{DD2}	10	+5 V supply 2
POL	11	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	Sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode).
$\overline{VCR}$/FFB	13	PLL time constant switch/field flyback input pin. Function controlled by an internal register bit (scan sync mode).
V_{SS2}	14	0 V ground 2
R	15	Dot rate character output of the RED colour information.
G	16	Dot rate character output of the GREEN colour information.
B	17	Dot rate character output of the BLUE colour information.
RGBREF	18	DC input voltage to define the output high level on the RGB pins.
BLAN	19	Dot rate fast blanking output.
V_{SS3}	20	0 V ground 3
$\overline{COR}$	21	Programmable active LOW output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open drain output.
ODD/$\overline{EVEN}$	22	25 Hz output synchronized with the CVBS inputs field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents.
Y	23	Dot rate character output of teletext foreground colour information; open drain output.
SCL	24	Serial clock input for the I^2C-bus. It can still be driven during power-down of the device.
SDA	25	Serial input/output data port for the I^2C-bus; open drain output. It can still be driven during power-down of the device.
i.c.	26 to 40	Internally connected. Must be left open-circuit in application.

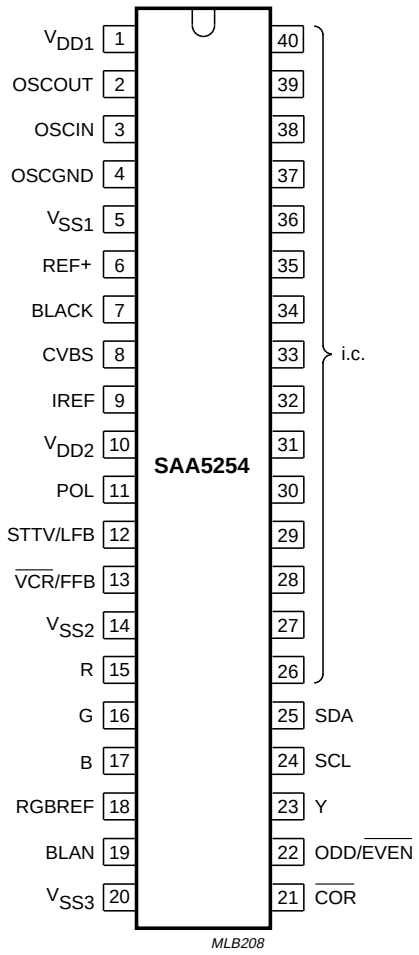


Fig.2 Pin configuration; SOT129 (DIP40).

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Business group *"Consumer Integrated Circuits SNW-FQ-611-Part E"*. The principal requirements are shown in Tables 1 to 4.

Group A

Table 1 Acceptance tests per lot

TEST	CONDITIONS	REQUIREMENTS(1)
Mechanical		cumulative target < 100 ppm
Electrical		cumulative target < 100 ppm

Group B

Table 2 Processability tests (by package family)

TEST	CONDITIONS	REQUIREMENTS(1)
Solderability		< 7% LTPD
Mechanical		< 15% LTPD
Solder heat resistance		< 15% LTPD

Group C

Table 3 Reliability tests (by process family)

TEST	CONDITIONS	REQUIREMENTS(1)
Operational life	168 hours at T_j = 150 °C	< 1500 FPM; equivalent to < 100 FITS at T_j = 70 °C
Humidity life	temperature, humidity, bias (1000 hours, 85 °C, 85% RH or equivalent test)	< 2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	< 2000 FPM

Table 4 Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS(1)
ESD and latch-up	ESD Human body model 2000 V, 100 pF, 1.5 kΩ	< 15% LTPD
	ESD Machine model 200 V, 100 pF, 1.5 kΩ	< 15% LTPD
	latch-up 100 mA, $1.5 \times V_{DD}$ (absolute maximum)	< 15% LTPD

Notes to Tables 1 to 4

1. ppm = fraction of defective devices, in parts per million.
   LTPD = Lot Tolerance Percent Defective.
   FPM = fraction of devices failing at test condition, in Failures Per Million.
   FITS = Failures In Time Standard.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	–0.3	+6.5	V
V_I	input voltage (any input)	–0.3	V_{DD} + 0.5	V
V_O	output voltage (any output)	–0.3	V_{DD} + 0.5	V
I_O	output current (each output)	–10	+10	mA
I_{IOK}	DC input or output diode current	–20	+20	mA
T_{amb}	operating ambient temperature	–20	+70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = –20 to +70 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.5	5.0	5.5	V
$I_{DD(tot)}$	total supply current		–	90	120	mA
Inputs						
CVBS						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$t_{d(sync)}$	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		–150	0	+150	ns
$\Delta t_{d(sync)}$	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{video(p-p)}$	video input voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
PLL_{catch}	display PLL catching range		±7	–	–	%
Z_{source}	source impedance		–	–	250	Ω
C_i	input capacitance		–	–	10	pF
IREF						
R_{GND}	resistance to ground		–	27	–	kΩ
POL						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LBF						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_I	input current	note 1	–1	–	+1	mA
$t_{d(LFB)}$	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_I	input current	note 1	–1	–	+1	mA
RGBREF (note 2)						
V_I	input voltage		–0.3	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_{DC}	DC current		–	–	10	mA
SCL						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
f_{SCL}	clock frequency		0	–	100	kHz
$t_{i(r)}$	input rise time	10% to 90%	–	–	2	µs
$t_{i(f)}$	input fall time	90% to 10%	–	–	2	µs
C_i	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
G_v	small signal voltage gain		3.5	–	–	
G_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
C_i	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
BLACK						
C_{black}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
$t_{i(r)}$	input rise time	10% to 90%	–	–	2	µs
$t_{i(f)}$	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
$t_{o(f)}$	output fall time	3 to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
Outputs						
STTV						
G_{STTV}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{TCS}	TCS voltage amplitude		0.2	0.3	0.45	V
$V_{DCshift}$	DC voltage shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD} – 2 V	RGBREF –0.25 V	RGBREF	RGBREF +0.25 V	V
$\lvert Z_o \rvert$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
I_{DC}	DC current		–	–	–3.3	mA
$t_{o(r)}$	output rise time	10% to 90%	–	–	20	ns
$t_{o(f)}$	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
		I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
$V_{O(max)}$	allowed output voltage at pin	with external pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
$t_{o(r)}$	output rise time	10% to 90%	–	–	20	ns
$t_{o(f)}$	output fall time	90% to 10%	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ODD/$\overline{\text{EVEN}}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
$t_{o(r)}$	output rise time	0.6 to 2.2 V	–	–	50	ns
$t_{o(f)}$	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{\text{COR}}$ AND Y (OPEN DRAIN)						
V_{pu}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
$t_{o(f)}$	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} – 0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
T_{skew}	skew delay between display outputs R, G, B, $\overline{\text{COR}}$, Y and BLAN		–	–	20	ns
Timing						
I^2C-BUS (see Fig.3)						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ±1 mA.
2. RGBREF is the positive supply for the RGB output pins and it must be able to source the I_{OH} current from the R, G and B pins. The leakage specification on RGBREF only applies when there is no current load on the RGB pins.

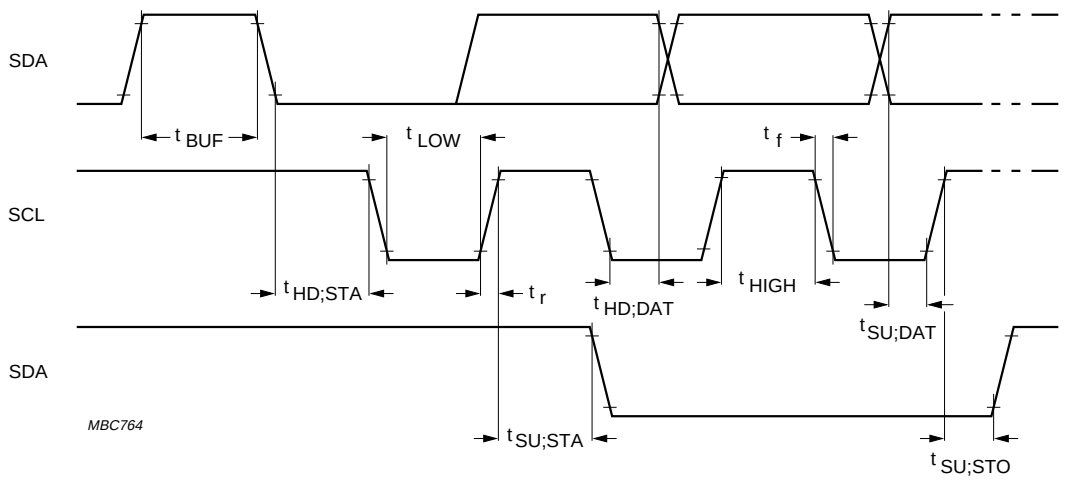
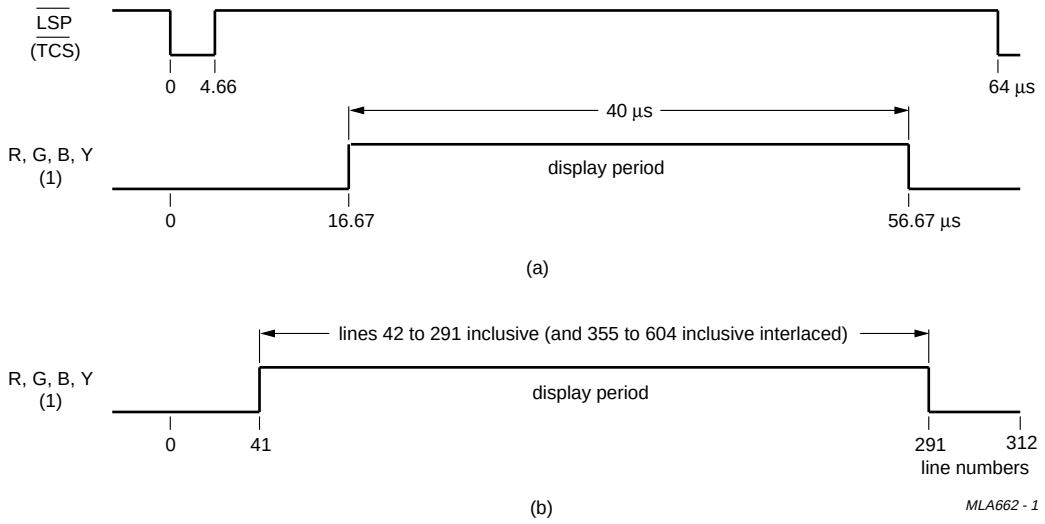


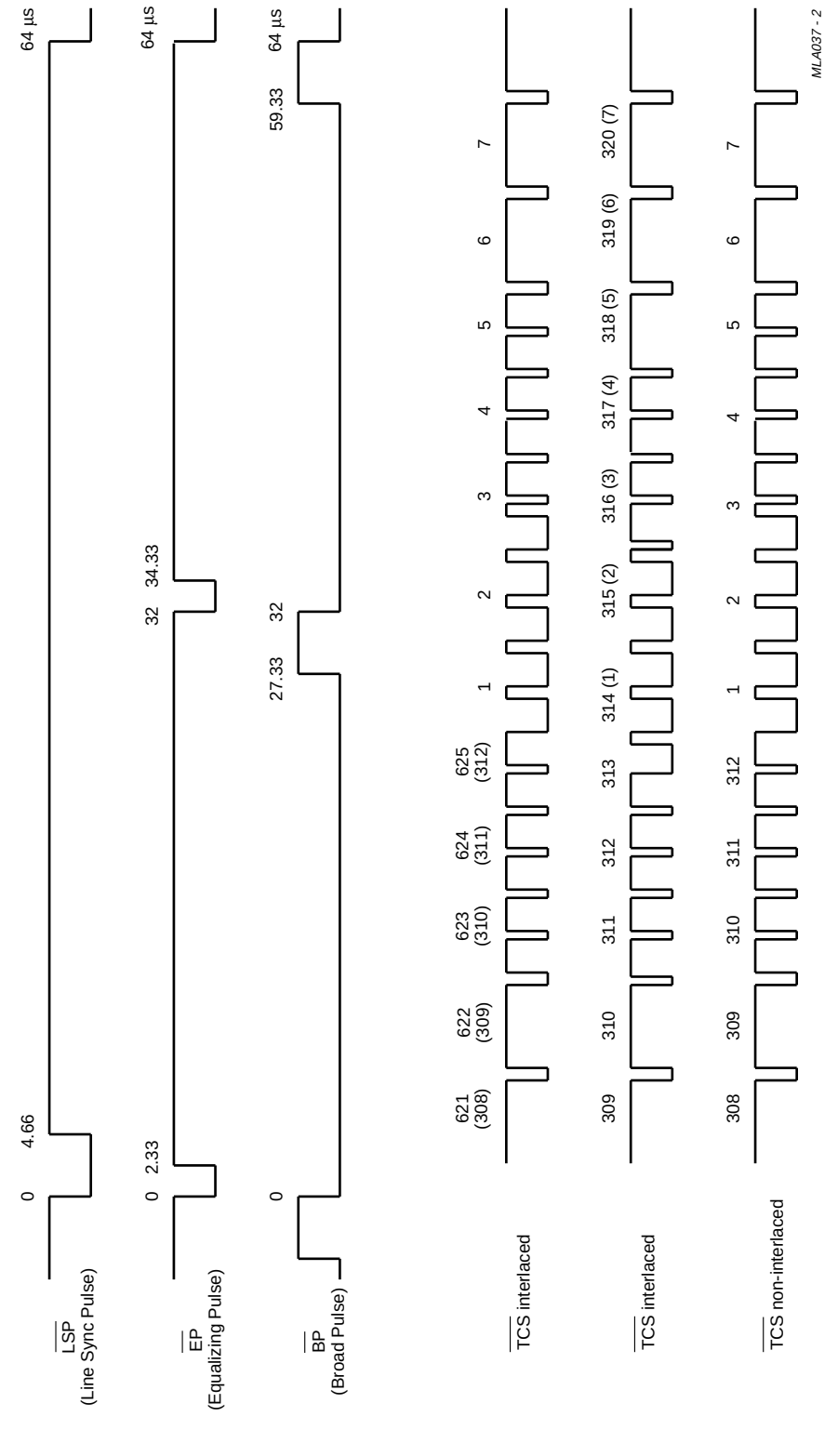
Fig.3 I²C-bus timing.

TIMING CHAIN



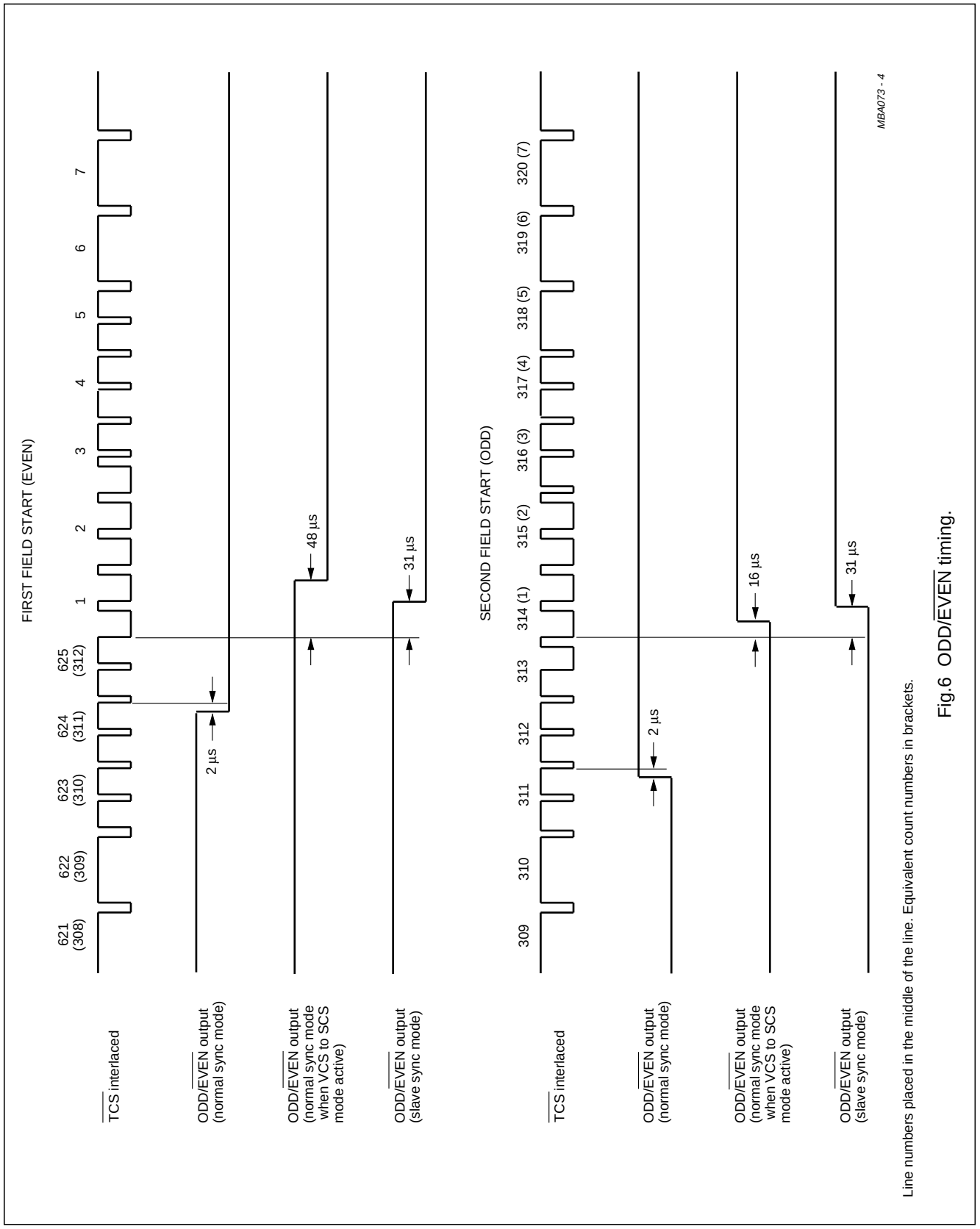
(1) Also BLAN in character and box blanking.

Fig.4 Display output timing (a) line rate (b) field rate.



LSP, EP and BP are combined to give TCS as shown. All timings are measured from falling edge of LSP.
Line numbers placed in the middle of the line.
Equivalent count numbers in brackets.
TCS is available on STTV/LFB pin.

Fig.5 Composite sync waveforms.



Line numbers placed in the middle of the line. Equivalent count numbers in brackets.

Fig.6 ODD/$\overline{\text{EVEN}}$ timing.

ON-CHIP MEMORY

SAA5254 page memory organization

The organization of the page memory is shown in Fig.7. The device provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; Row 24 is available for software generated status messages and FLOF/FASTEXT prompt information.

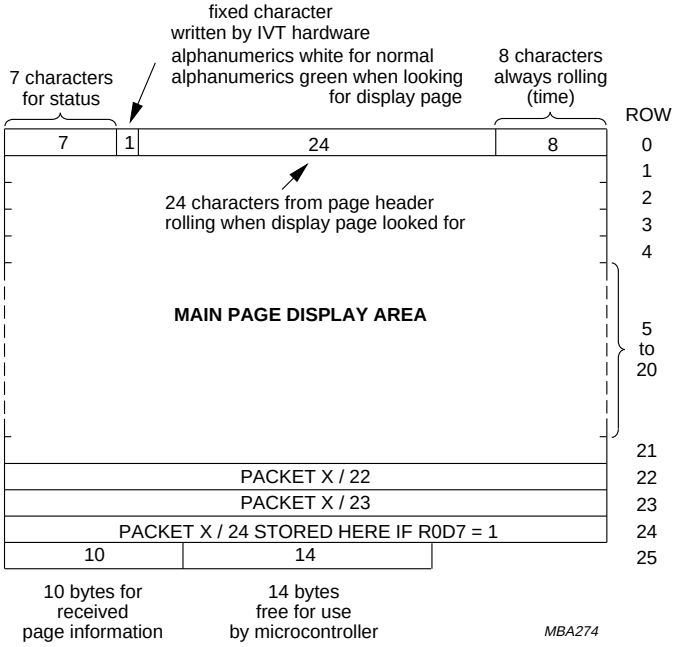


Fig.7 Basic page memory organization.

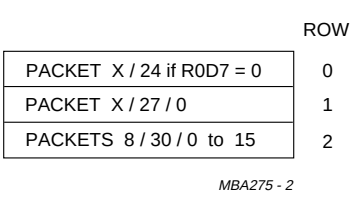


Fig.8 Organization of the extension memory.

REMARK TO Fig.7

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by the SAA5254 to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 5. The remaining 14 bytes are free for use by the microcontroller.

Table 5 Row 25 received control data format

ROW 25										
D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Table 6 Page number and sub-code for Table 5

BIT NAME	DESCRIPTION
Page number	
MAG	magazine
PU	page units
PT	page tens
PBLF	page being looked for
$\overline{\text{FOUND}}$	LOW for page has been found
HAM.ER	Hamming error in corresponding byte
Page sub-code	
MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens
C4 to C14	transmitted control bits

Register maps

SAA5254 mode registers R0 to R11 are shown in Table 7. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 9.

Table 7 Register map (notes 1 to 5)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
NAME	No.								
Advanced control	0	X/24 POS	FREE RUN PLL	AUTO ODD/$\overline{\text{EVEN}}$	DISABLE HDR ROLL	DISPLAY STATUS ROW ONLY	DISABLE ODD/$\overline{\text{EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7 + P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	DISABLT PKT 26	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX ON 24	BOX ON 1 to 23	BOX ON 0
		–	–	–	–	–	–	–	–
Cursor row	9	–	CLEAR MEMORY	A0	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Notes to Table 7

1. The dash (–) indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in Registers R0 to R13 are cleared to logic 0 on power-up except bits D0 and D1 of Registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to space (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is alpha white (00000111) as the acquisition circuit is enabled but all pages are on hold.
4. TB must be set to logic 0 for normal operation.
5. The I^2C-bus slave address is 00110001.

Table 8 Register description

REGISTER BIT D0 TO D7	FUNCTION
R0 AVANCED CONTROL - auto-increments to Register 1	
$\overline{R11}$/R11B SELECT	Selects reading of R11 if LOW or if HIGH R11B.
DISABLE ODD/$\overline{EVEN}$	Forces ODD/$\overline{EVEN}$ output LOW when logic 1.
DISPLAY STATUS ROW	When SET = 1 and R1D6 = 1 open (8-bit mode) then all the text display is blanked out apart from the status row, this allows the page memory to be used for non-textural data, such as in the German TOP system.
DISABLE HDR ROLL	Disables green rolling header and time.
AUTO ODD/$\overline{EVEN}$	When $\overline{SET}$ forces ODD/$\overline{EVEN}$ LOW if any TV picture displayed, if DISABLE ODD/$\overline{EVEN}$ = 0
FREE RUN PLL	Will force the display PLL to free run in all conditions.
X/24 POS	Automatic display of FASTEXT prompt row when logic 1.
R1 MODE - auto-increments to Register 2	
T0, T1	Interlace/non-interlace 312/313 line control (see Table 10).
TCS ON	Text composite sync or direct sync select (see Table 10 for FFB mode selection).
$\overline{DEW}$/FULL FIELD	Field-flyback or full-channel mode.
ACQ $\overline{ON}$/OFF	Acquisition circuits turned off when logic 1.
$\overline{7 + P}$/8-BIT	7 bits with parity checking or 8-bit mode.
DISABLE PKT 26	Disable automatic processing of packet 26.
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal.
R2 PAGE REQUEST ADDRESS - auto-increments to Register 3	
START COLUMN SC0 to SC2	Point to start column for page request data (see Table 9).
TB	Must be logic 0 for normal operation.
R3 PAGE REQUEST DATA - does not auto-increment (see Table 9)	
R5 NORMAL DISPLAY CONTROL - auto-increments to Register 6	
R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto-increments to Register 7; note 1	
PON	Picture on.
TEXT	Text on.
COR	Contrast reduction on.
BKGND	Background colour on.

REGISTER BIT D0 TO D7	FUNCTION
R7 DISPLAY MODE - does not auto-increment	
BOX ON 0	Boxing function allowed on Row 0.
BOX ON 1 to 23	Boxing function allowed on Rows1 to 23.
BOX ON 24	Boxing function allowed on Row 24.
DOUBLE HEIGHT	To display double height text.
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1.
REVEAL ON	To reveal concealed text.
CURSOR ON	To display cursor.
STATUS TOP	Row 25 displayed above or below the main text.
R9 CURSOR ROW - auto-increments to Register 10	
R0 to R4	Active row for data written to or read from memory via the I^2C-bus.
A0	Selects display memory page (when = 0) or extension memory (when = 1).
CLEAR MEM	When set to logic 1, clears the display memory. This bit is automatically reset.
R10 CURSOR COLUMN - auto-increments to Register 11 or 11B	
C0 to C5	Active column for data written to or read from memory via the I^2C-bus.
R11 CURSOR DATA - does not auto-increment	
D0 to D7	Data read from/written to memory via I^2C-bus, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed.
R11B DEVICE STATUS - does not auto-increment	
VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase-locked to input video when logic 1.
TEXT SIGNAL QUALITY	If a good teletext signal is being received then logic 1.
ROM VER R0 to R4	Indicated language/ROM variant. For Western European = 11000.
$\overline{625}$/525 SYNC	If the input video is a 525 line signal then logic 1.

Note

1. These functions have IN and OUT referring to inside and outside the boxing function respectively.

Table 9 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	DO CARE Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	DO CARE Page tens	PT3	PT2	PT1	PT0
2	DO CARE Page units	PU3	PU2	PU1	PU0
3	DO CARE Hours tens	X	X	HT1	HT0
4	DO CARE Hours units	HU3	HU2	HU1	HU0
5	DO CARE Minutes tens	X	MT2	MT1	MT0
6	DO CARE Minutes units	MU3	MU2	MU1	MU0

Notes to Table 9

1. Abbreviations are as for Table 5 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, normal or timed page selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I^2C-bus transmission bytes.
5. X = Don't care.

Table 10 Interlace/non-interlace 312/313 line control and ODD/$\overline{\text{EVEN}}$ field detection option

TCS ON FFB MODE(1)	T1	T0	RESULT
X	0	0	interlaced 312.5/312.5 lines
X	0	1	non-interlaced 312/313 lines (note 2)
X	1	0	non-interlaced 312/313 lines (note 2)
0	1	1	SCS (scan composite sync) mode: FFB leading edge in first broad pulse of field
1	1	1	SCS (scan composite sync) mode: FFB leading edge in second broad pulse of field

Notes

1. X = don't care.
2. Reverts to interlaced mode if a newsflash or subtitle is being displayed.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone, as shown in Fig.9. The crystal characteristics are given in Table 11.

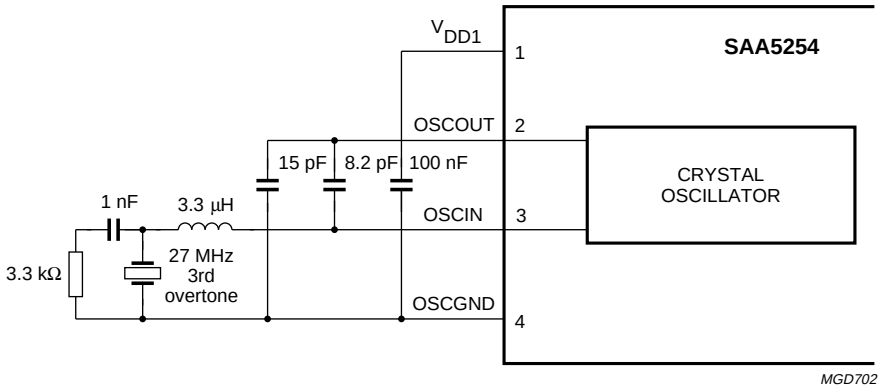


Fig.9 Crystal oscillator application diagram.

Table 11 Crystal characteristics (see Fig.9)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)				
C1	series capacitance	1.7	–	pF
C0	parallel capacitance	5.2	–	pF
C_L	load capacitance	20	–	pF
R_r	resonance resistance	–	50	Ω
R1	series resistance	20	–	Ω
X_a	ageing	–	$\pm 5 \times 10^{-6}$	$year^{-1}$
X_j	adjustment tolerance	–	$\pm 25 \times 10^{-6}$	
X_d	drift	–	$\pm 25 \times 10^{-6}$	

CHARACTER SETS

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Tables 17, 18, 19 and 20 with reference to their table position in the basic character matrix illustrated in Table 16. The SAA5254 automatically decodes transmission bits C12 to C14. Tables 12, 13, 14 and 15 illustrates the character matrixes.

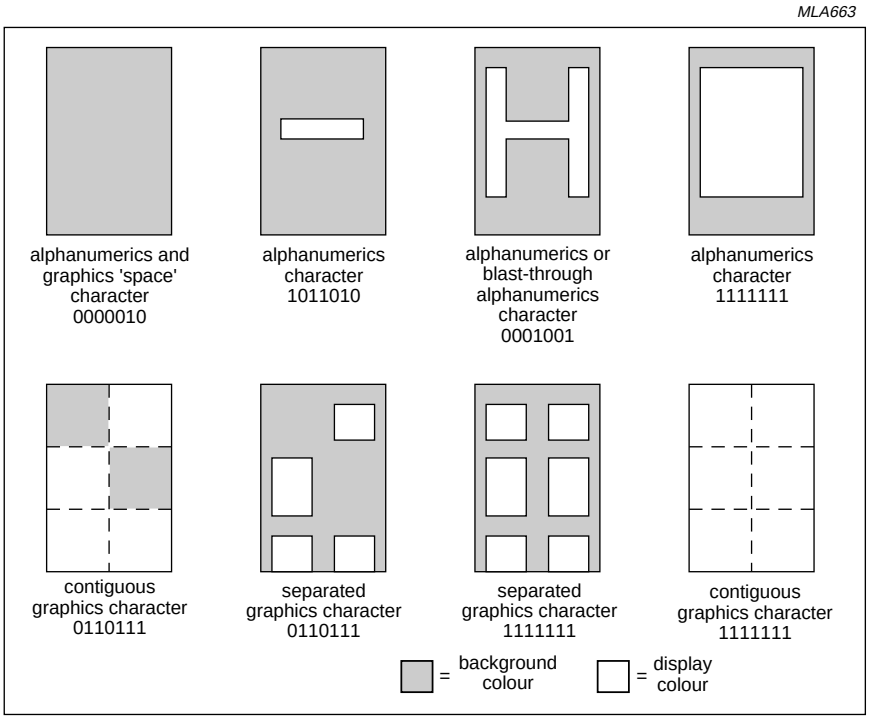


Fig.10 Character format.

Table 12 SAA5254P/E character data input decoding, West European languages; notes 1 to 9
For character version number (11000) see Register 11B.

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7				0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b_6				0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5				0	1	0	1	0	1	0	1	0		1		0	1	0	1	0	1
b_4	b_3	b_2	b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black																
0	0	0	1	1	alpha - numerics red	graphics red																
0	0	1	0	2	alpha - numerics green	graphics green																
0	0	1	1	3	alpha - numerics yellow	graphics yellow																
0	1	0	0	4	alpha - numerics blue	graphics blue																
0	1	0	1	5	alpha - numerics magenta	graphics magenta																
0	1	1	0	6	alpha - numerics cyan	graphics cyan																
0	1	1	1	7	alpha - numerics white (2)	graphics white																
1	0	0	0	8	flash	conceal display																
1	0	0	1	9	steady (2)	contiguous graphics (2)																
1	0	1	0	10	end box (2)	separated graphics																
1	0	1	1	11	start box	ESC (1)																
1	1	0	0	12	normal height (2)	black back - ground (2)																
1	1	0	1	13	double height	new back - ground																
1	1	1	0	14	SO (1)	hold graphics																
1	1	1	1	15	SI (1)	release graphics (2)																

MBA429

Table 13 SAA5254P/H character data input decoding, East European languages; notes 1 to 9

For character version number (11001) see Register 11B.

BITS b_4 b_3 b_2 b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
	b_8	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
	b_7	0	0	0	0	0	0	1	1	1		1		0	0	0	0	1	1
	b_6	0	0	1	1	1	1	0	0	1		1		0	0	0	1	1	1
	b_5	0	1	0	0	1	1	0	1	0		1		0	1	0	1	0	1
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics white (2)	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady (2)	contiguous graphics (2)																
1 0 1 0	10	end box (2)	separated graphics																
1 0 1 1	11	start box	ESC (1)																
1 1 0 0	12	normal height (2)	black back - ground (2)																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO (1)	hold graphics																
1 1 1 1	15	SI (1)	release graphics (2)																

MLA961

Table 14 SAA5254P/T character data input decoding, West European and Turkish languages; notes 1 to 9
For character version number (11010) see Register 11B.

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7				0	0	0	0	1	1	1	1	0	1	1		1	1	0	0	1	1
b_6				0	0	1	1	1	1	0	0	1	1	1		1	1	0	0	1	1
b_5				0	1	0	1	1	1	0	1	0	1	0		1	1	0	1	0	1
b_4	b_3	b_2	b_1	row / column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black															
0	0	0	1	1	alpha - numerics red	graphics red															
0	0	1	0	2	alpha - numerics green	graphics green															
0	0	1	1	3	alpha - numerics yellow	graphics yellow															
0	1	0	0	4	alpha - numerics blue	graphics blue															
0	1	0	1	5	alpha - numerics magenta	graphics magenta															
0	1	1	0	6	alpha - numerics cyan	graphics cyan															
0	1	1	1	7	alpha - numerics white (2)	graphics white															
1	0	0	0	8	flash	conceal display															
1	0	0	1	9	steady (2)	contiguous graphics (2)															
1	0	1	0	10	end box (2)	separated graphics															
1	0	1	1	11	start box	ESC (1)															
1	1	0	0	12	normal height (2)	black back - ground (2)															
1	1	0	1	13	double height	new back - ground															
1	1	1	0	14	SO (1)	hold graphics															
1	1	1	1	15	SI (1)	release graphics (2)															

MBA431

Table 15 SAA5254P/R character data input decoding, Baltic and Cyrillic languages; notes 1 to 9
For character version number (11101) see Register 11B.

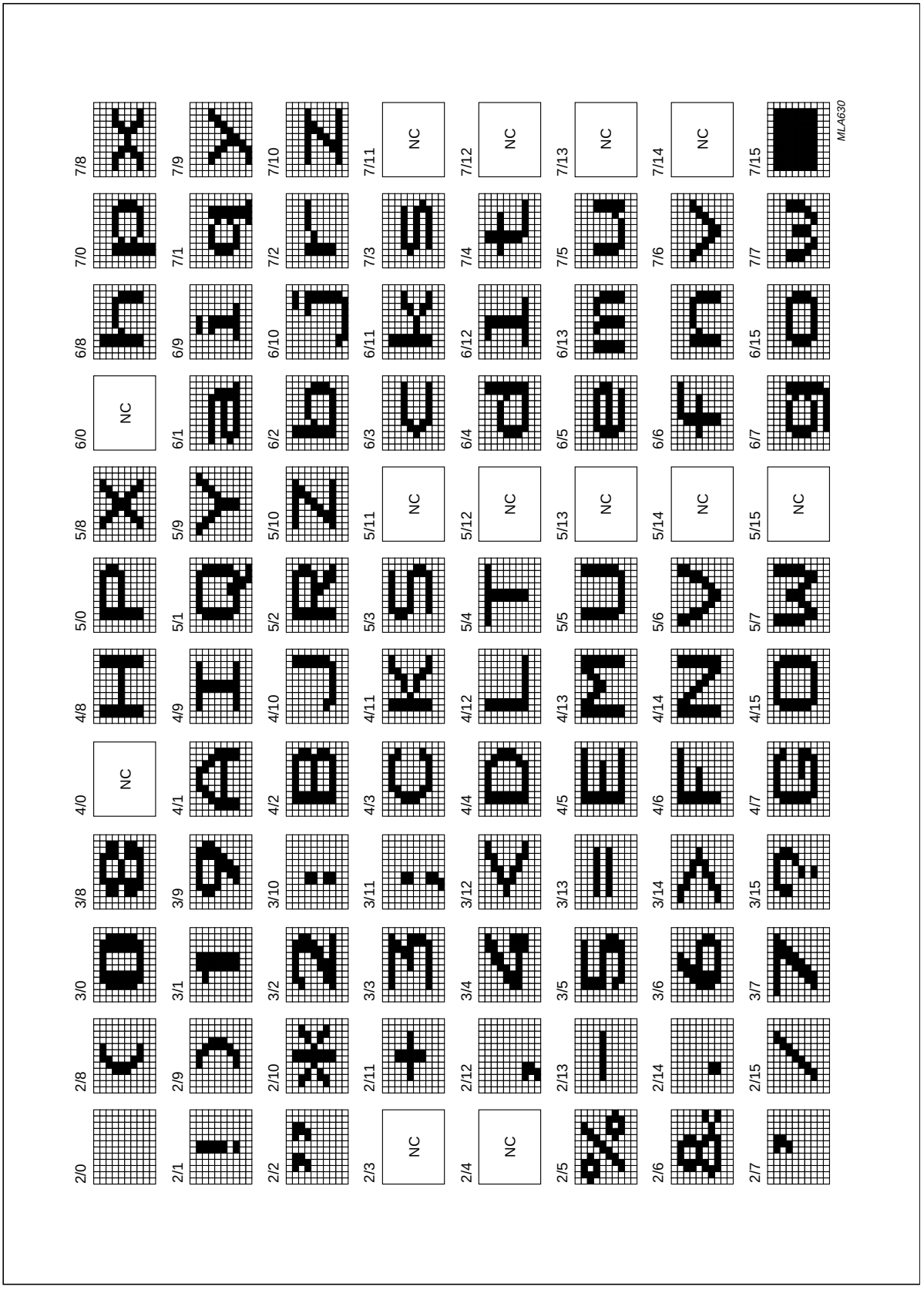
BITS b_4 b_3 b_2 b_1	row	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
		b_8	0	0	0 or 1	0	0 or 1	0	0	0		0		1	1	1	1	1	1
		b_7	0	0	0	1	1	1	1	1		1		0	0	1	1	1	1
		b_6	0	0	1	0	1	0	0	1		1		0	0	0	0	1	1
		b_5	0	1	0	1	1	0	1	0		1		0	1	0	1	0	1
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics white (2)	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady (2)	contiguous graphics (2)																
1 0 1 0	10	end box (2)	separated graphics																
1 0 1 1	11	start box	TWIST																
1 1 0 0	12	normal height (2)	black back - ground (2)																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO (1)	hold graphics																
1 1 1 1	15	SI (1)	release graphics (2)																

MBA648 - 1

Notes to Tables 12, 13 14 and 15

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each row begins.
3. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
4. Characters may be referred to by column and row (for example 2/5 refers to %).
5. Black represents displayed colour. White represents background.
6. The SAA5254 national option characters are illustrated in Tables 17, 18, 19 and 20.
7. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5 (E, H and T codes only).
8. National option characters will be displayed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Tables 17, 18, 19 and 20.
9. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 16 SAA5254 basic character matrix; note 1



Note to Table 16

1. Where: NC = national option character position.

Table 17 SAA5254P/E national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MLB458

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 18 SAA5254P/H national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAKIA	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MLA966

(1) PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 16.

Table 19 SAA5254P/T national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	**2 / 3**	**2 / 4**	**4 / 0**	**5 / 11**	**5 / 12**	**5 / 13**	**5 / 14**	**5 / 15**	**6 / 0**	**7 / 11**	**7 / 12**	**7 / 13**	**7 / 14**
ENGLISH	**0**	**0**	**0**	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	**0**	**0**	**1**	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	**1**	**1**	**0**	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	**0**	**1**	**1**	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	**1**	**0**	**0**	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	**1**	**0**	**1**	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) PHCB are the Page Header Control Bits. Other combinations default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 16.

Table 20 SAA5254P/R national option character set

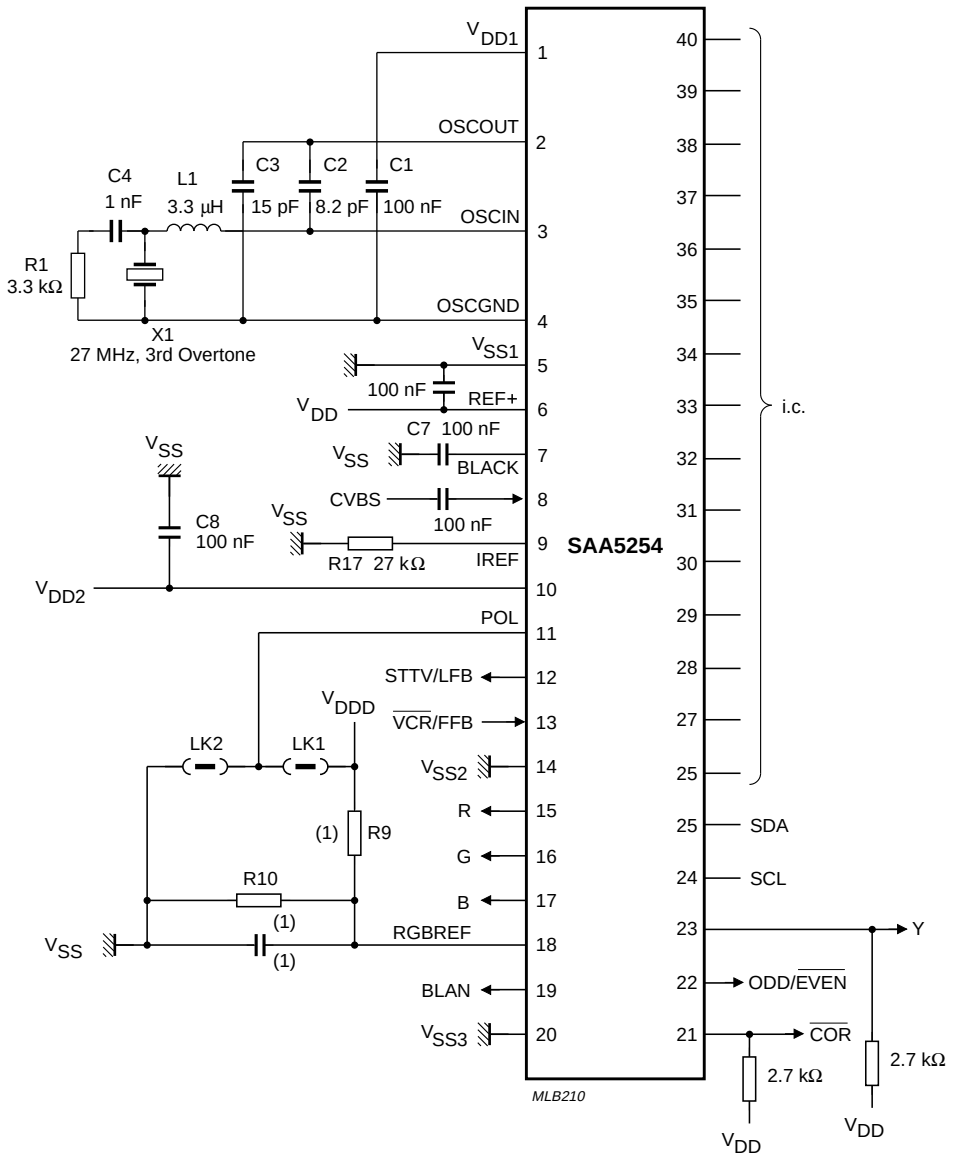
LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ESTONIAN	0	1	0	#	Õ	Š	Ä	Ö	Ž	Ü	Õ	š	ä	ö	ž	ü
LETTISH / LITHUANIAN	0	1	1	#	$	Š	ė	ę	Ž	č	ū	š	ą	ų	ž	į
RUSSIAN	1	0	0													

	2	3	4	5	6	7
0		0	Ю	П	ю	п
1	!	1	А	Я	а	я
2	”	2	Б	Р	б	р
3	#	3	Ц	С	ц	с
4	$	4	Д	Т	д	т
5	%	5	Е	У	е	у
6	ы	6	Ф	Ж	ф	ж
7	’	7	Г	В	г	в
8	(	8	Х	Ь	х	ь
9	)	9	И	Ъ	и	ъ
10	ж	:	Й	З	й	з
11	+	;	К	Ш	к	ш
12	,	<	Л	Э	л	э
13	–	=	М	Щ	м	щ
14	.	>	Н	Ч	н	ч
15	/	?	О	Ы	о	■

MEA597

(1) PHCB are the Page Header Control Bits. Other combinations default to Estonian.

APPLICATION INFORMATION

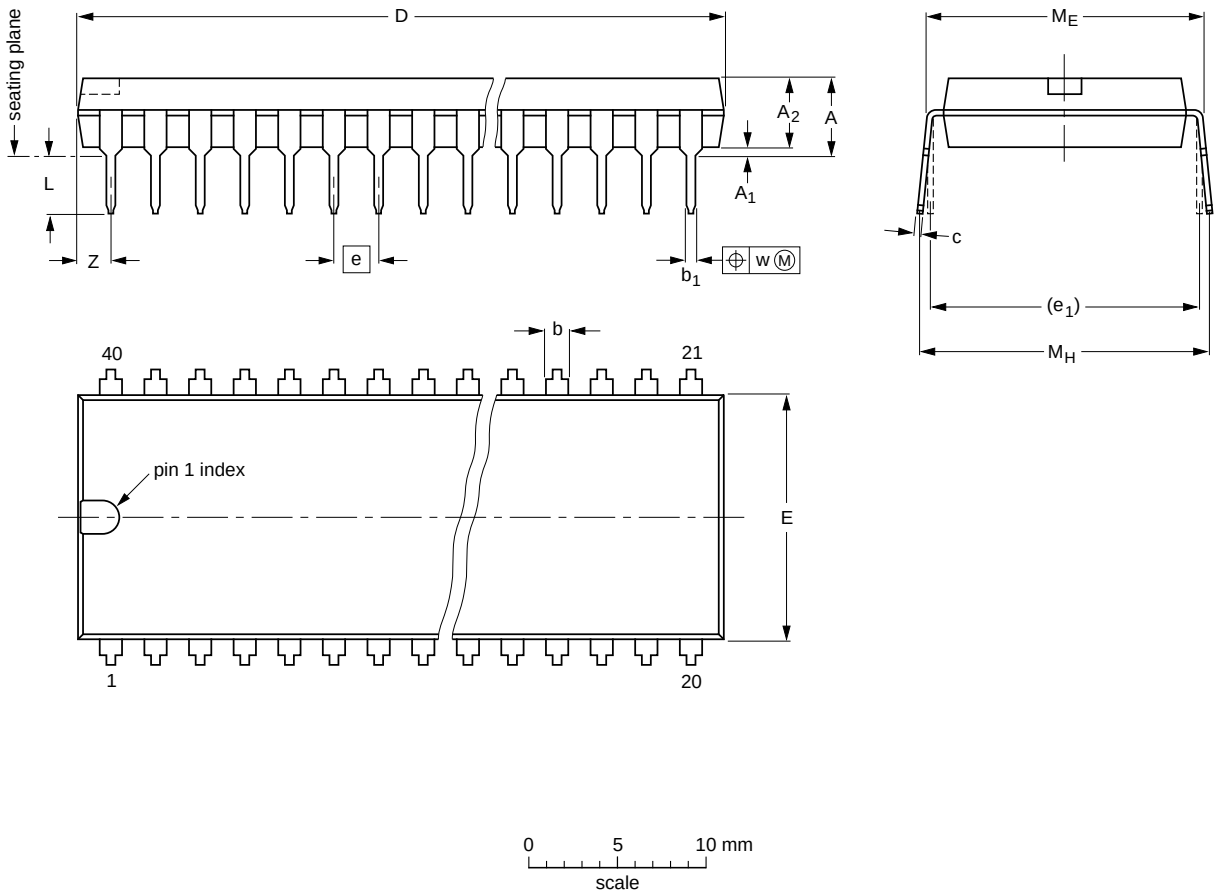


(1) Value dependent on application.

Fig.11 Application diagram; SOT129 (DIP40).

PACKAGE OUTLINE

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 247 9145, Fax. +7 095 247 9144

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 537021/00/02/pp36 Date of release: 1996 Nov 07 Document order number: 9397 750 01015

Let's make things better.

Philips Semiconductors

PHILIPS