

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.6 A, 400 V

$r_{DS(on)} = 2.5 \Omega$

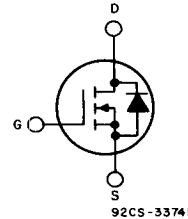
Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The BUZ 76 A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

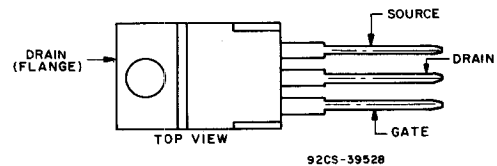
The BUZ 76 A is supplied in the JEDEC TO-220AB plastic package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

MAXIMUM RATINGS, Absolute-Maximum Values ($T_c = 25^\circ\text{C}$):

DRAIN-SOURCE VOLTAGE	V_{DS}	400	V
DRAIN-GATE VOLTAGE, $R_{DS} = 20 \text{ k}\Omega$	V_{DGR}	400	V
GATE-SOURCE VOLTAGE	V_{GS}	± 20	V
DRAIN CURRENT, RMS Continuous $T_c = 30^\circ\text{C}$	I_D	2.6	A
Pulsed $T_c = 25^\circ\text{C}$	I_{DM}	10	A
POWER DISSIPATION @ $T_c = 25^\circ\text{C}$	P_T	40	W
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	$^\circ\text{C}$
DIN HUMIDITY CATEGORY — DIN 40040		E	
IEC CLIMATIC CATEGORY — DIN IEC 68-1		55/150/56	

ELECTRICAL CHARACTERISTICS At Case Temperature (T_c) = 25° C Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS} $V_{GS} = 0\text{ V}$ $I_D = 0.25\text{ mA}$	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$ $V_{DS} = V_{GS}$ $I_D = 1\text{ mA}$	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS} $T_J = 25\text{ °C}$ $T_J = 125\text{ °C}$ $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS} $V_{GS} = 20\text{ V}$ $V_{DS} = 0\text{ V}$	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$ $V_{GS} = 10\text{ V}$ $I_D = 1.5\text{ A}$	—	2.2	2.5	Ω
Forward Transconductance	g_{fs} $V_{DS} = 25\text{ V}$ $I_D = 1.5\text{ A}$	2.1	2.5	—	S
Input Capacitance	C_{iss} $V_{GS} = 0\text{ V}$	—	300	500	pF
Output Capacitance	C_{oss} $V_{DS} = 25\text{ V}$	—	50	80	
Reverse Transfer Capacitance	C_{rss} $f = 1\text{ MHz}$	—	35	60	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r $V_{CC} = 30\text{ V}$ $I_D = 2.4\text{ A}$	— —	15 40	20 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r $V_{GS} = 10\text{ V}$ $R_{GS} = 50\text{ }\Omega$	— —	50 30	65 40	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	≤ 3.1			$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR} $T_C = 25\text{ °C}$	—	—	2.6	A
Pulsed Reverse Drain Current	I_{DRM}	—	—	10	
Diode Forward Voltage	V_{SD} $I_F = 2 \times I_{DR}$ $V_{GS} = 0\text{ V}, T_J = 25\text{ °C}$	—	1.1	1.4	V
Reverse Recovery Time	t_{rr} $T_J = 25\text{ °C}, I_F = I_{DR}$	—	300	—	ns
Reverse Recovered Charge	Q_{RR} $di/dt = 100\text{ A}/\mu\text{s}, V_R = 100\text{ V}$	—	2.5	—	μC

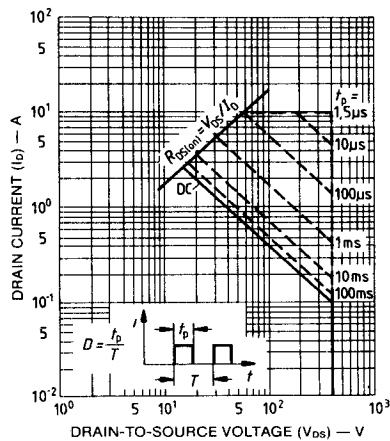


Fig. 1 - Maximum safe operating areas for all types.

BUZ 76 A

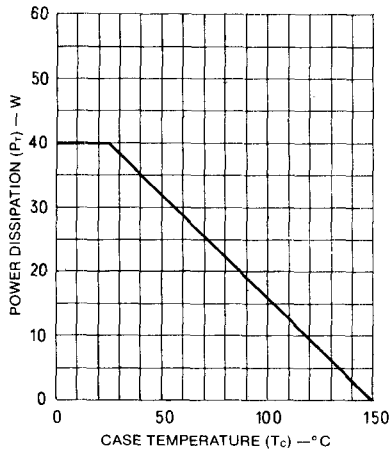


Fig. 2 - Power vs. temperature derating curve for all types.

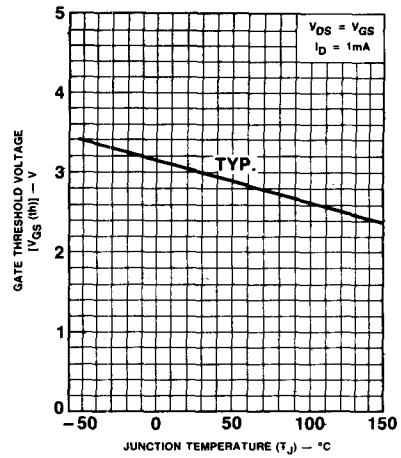


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

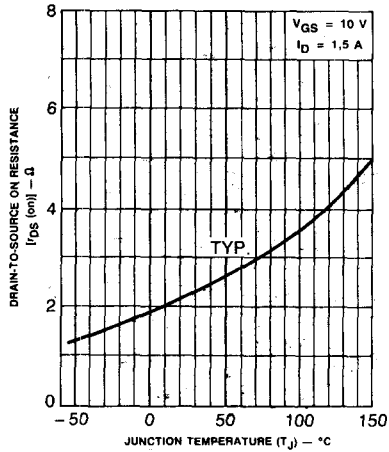


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

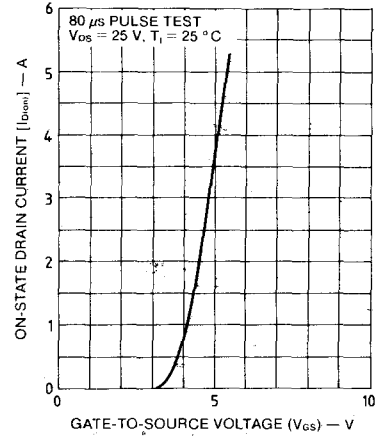


Fig. 5 - Typical transfer characteristics for all types.

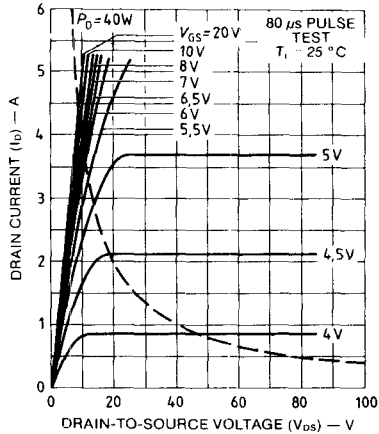


Fig. 6 - Typical output characteristics.

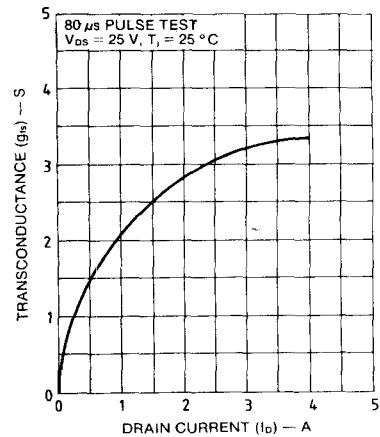


Fig. 7 - Typical transconductance vs. drain current.

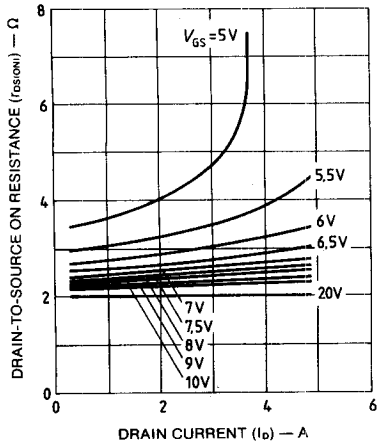


Fig. 8 - Typical on-resistance vs. drain current.

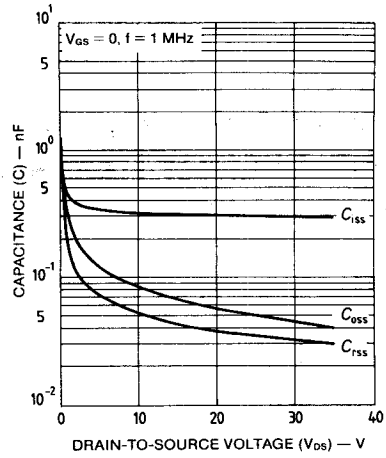


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

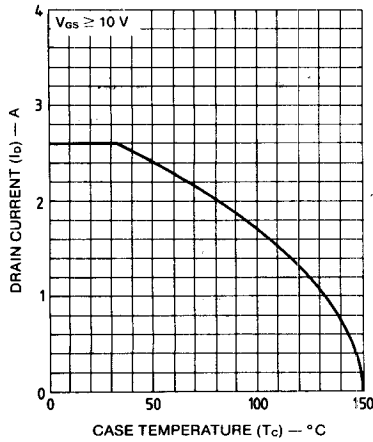


Fig. 10 - Maximum drain current vs. case temperature.

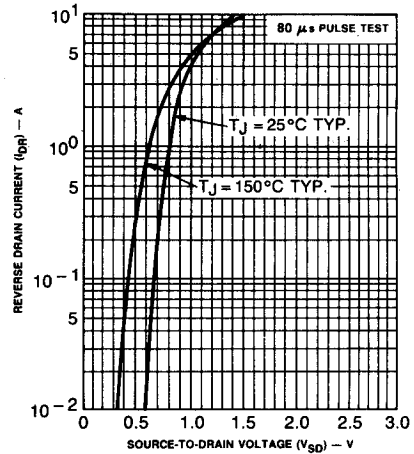


Fig. 11 - Typical source-drain diode forward voltage.

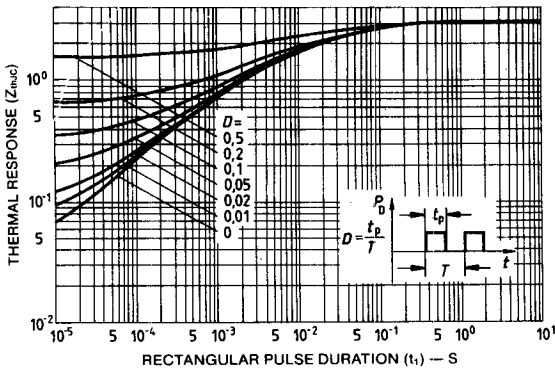


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

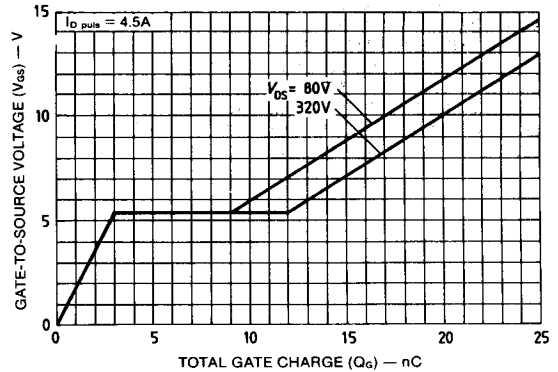


Fig. 13 - Typical gate charge vs. gate-to-source voltage.