National Semiconductor

MM2102A, MM2102AL Family
1024-Bit (1024 x 1) Static RAMs

General Description

The MM2102A family of high speed 1024 x 1-bit static random access read/write memories is manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

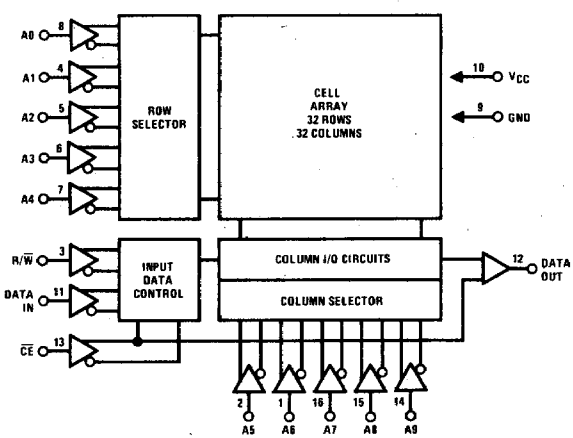
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity.

In addition to the MM2102A, a low power version, the MM2102AL, is also available. This selection offers a maximum operating current of 33 mA and a guaranteed standby mode down to a power supply voltage of 1.5V.

Features

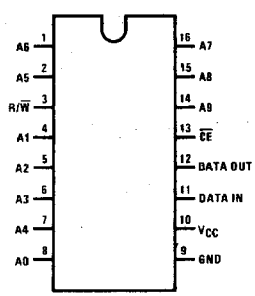
- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

Block Diagram



Connection Diagram

Dual-In-Line Package



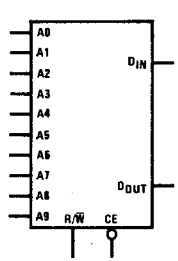
TOP VIEW

Order Number:	Order Number:
MM2102AJ-2L	MM2102AN-2L
MM2102AJ-2	MM2102AN-2
MM2102AJ-L	MM2102AN-L
MM2102AJ	MM2102AN
MM2102AJ-4L	MM2102AN-4L
MM2102AJ-4	MM2102AN-4
MM2102AJ-6L	MM2102AN-6L
MM2102AJ-6	MM2102AN-6
See NS Package J16A	See NS Package N16A

Truth Table

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	Hi-Z	Not selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

Logic Symbol



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Input Low Voltage	−0.5	0.8	V
Input High Voltage	2.0	V_{CC}	V

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = ±5%, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MM2102A, MM2102A-2, MM2102A-4, MM2102A-6		MM2102A-L, MM2102A-2L, MM2102A-4L, MM2102A-6L		UNITS
			MIN	MAX	MIN	MAX	
I_{LI}	Input Load Current	V_{IN} = 0 to 5.25V		10		10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 2.4V		5		5	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 0.4V		−10		−10	μA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 25°C		45		31	mA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 0°C		50		33	mA
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.4		2.4		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

AC Electrical Characteristics

(With standard load) T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified.

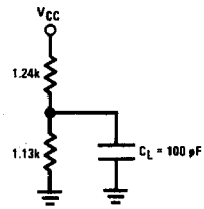
SYMBOL	PARAMETER	MM2102A-2, MM2102A-2L		MM2102A, MM2102A-L		MM2102A-4, MM2102A-4L		MM2102A-6, MM2102A-6L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE *(Figure 1)*										
t_{RC}	Read Cycle	250		350		450		650		ns
t_A	Access Time		250		350		450		650	ns
t_{CO}	Chip Enable to Output Time		100		150		200		200	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40		50		ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0		ns
WRITE CYCLE *(Figure 2)*										
t_{WC}	Write Cycle	250		350		450		650		ns
t_{AW}	Address to Write Set-Up	20		20		20		20		ns
t_{WP}	Write Pulse Width	100		150		200		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Date Set-Up Time	85		125		175		175		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CW}	Chip Enable To Write Set-Up	100		150		200		200		ns

AC Electrical Characteristics $T_A = 25°C$, f = 1 MHz

SYMBOL	PARAMETER	LIMIT (pF)	
		TYP	MAX
CAPACITANCE [2]			
C_{IN}	Input Capacitance (All Inputs V_{IN} = 0V)	3	5
C_{OUT}	Output Capacitance, V_O = 0V	4	6

Note 2: This parameter is guaranteed by periodic testing

AC Test Circuit



Switching Time Waveforms

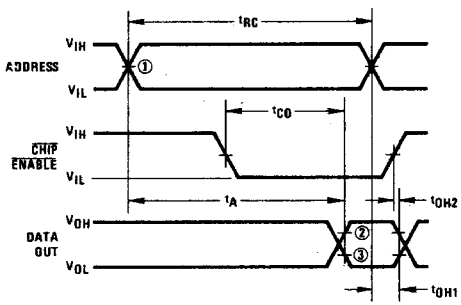


FIGURE 1. Read Cycle

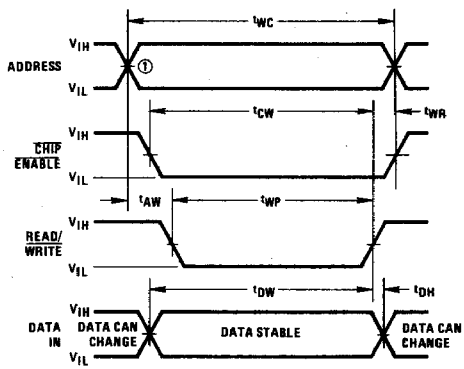


FIGURE 2. Write Cycle

Note ①: Input reference level for timing is 1.5V.
Note ②: V_{OH} = 2V is reference level for output high.
Note ③: V_{OL} = 0.8V is reference level for output low.
Note ④: Input rise and fall times are 10 ns.

Standby Characteristics $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	CONDITIONS	MM2102A, MM2102A-2, MM2102A-4, MM2102-6			MM2102A-L, MM2102A-2L, MM2102A-4L, MM2102A-6L			UNITS
			MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	
V_{PD}	V_{CC} in Standby		1.5			1.5			V
V_{CES}	$\overline{CE}$ Bias in Standby	$2 \leq V_{PD} \leq V_{CCMAX}$	2.0			2.0			V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$1.5 \leq V_{PD} \leq 2$	V_{PD}			V_{PD}			V
I_{PD1}	Standby Current	All Inputs = V_{PD} = 1.5V			28			23	mA
I_{PD2}	Standby Current	All Inputs = V_{PD} = 2V			38			28	mA
t_{CP}	Chip Deselect to Standby Time		0			0			ns
t_R	Recovery Time (Note 4)		t_{RC}			t_{RC}			ns

Note 3: Typical values at $T_A = 25°C$.
Note 4: $t_R = t_{RC}$ = read cycle time.

Standby Waveforms