SONY

CXA2150AQ

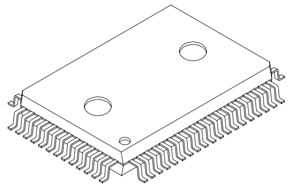
CRT DRIVER

Description

The CXA2150AQ is a bipolar IC which integrates base-band Y/C signal processing, RGB signal processing, horizontal sync signal processing that supports 15.7/31.5/33.75/37.9/45kHz, and a vertical deflection circuit that supports 50/60/100/120Hz into a single chip.

This IC has been developed for DTV, and realizes the configuration of a high-end TV system that supports 960i, 1080i, 720p, etc. in addition to 480i.

64 pin QFP (Plastic)



Features

- I^2C bus supported
- YCbCr input offset adjustment circuit
- LTI and CTI circuits
- Sharpness f0 switching circuit that supports band width of various input sources
- Color (Cr signal) dependent sharpness circuit
- Coring circuit for VM signal
- AKB system
- Various ABL functions
- Two sets of analog RGB inputs
- Horizontal sync processing that supports 15.7/31.5/33.75/37.9/45kHz
- Vertical deflection circuit that supports 50/60/100/120Hz
- Quick responsed VAGC when switching channels etc.
- Deflection compensation circuit capable of supporting various wide modes
- For flat-TV suitable various VSAW waveform and parabola output

Applications

Color TVs (4:3, 16:9)

Structure

Bipolar silicon monolithic IC

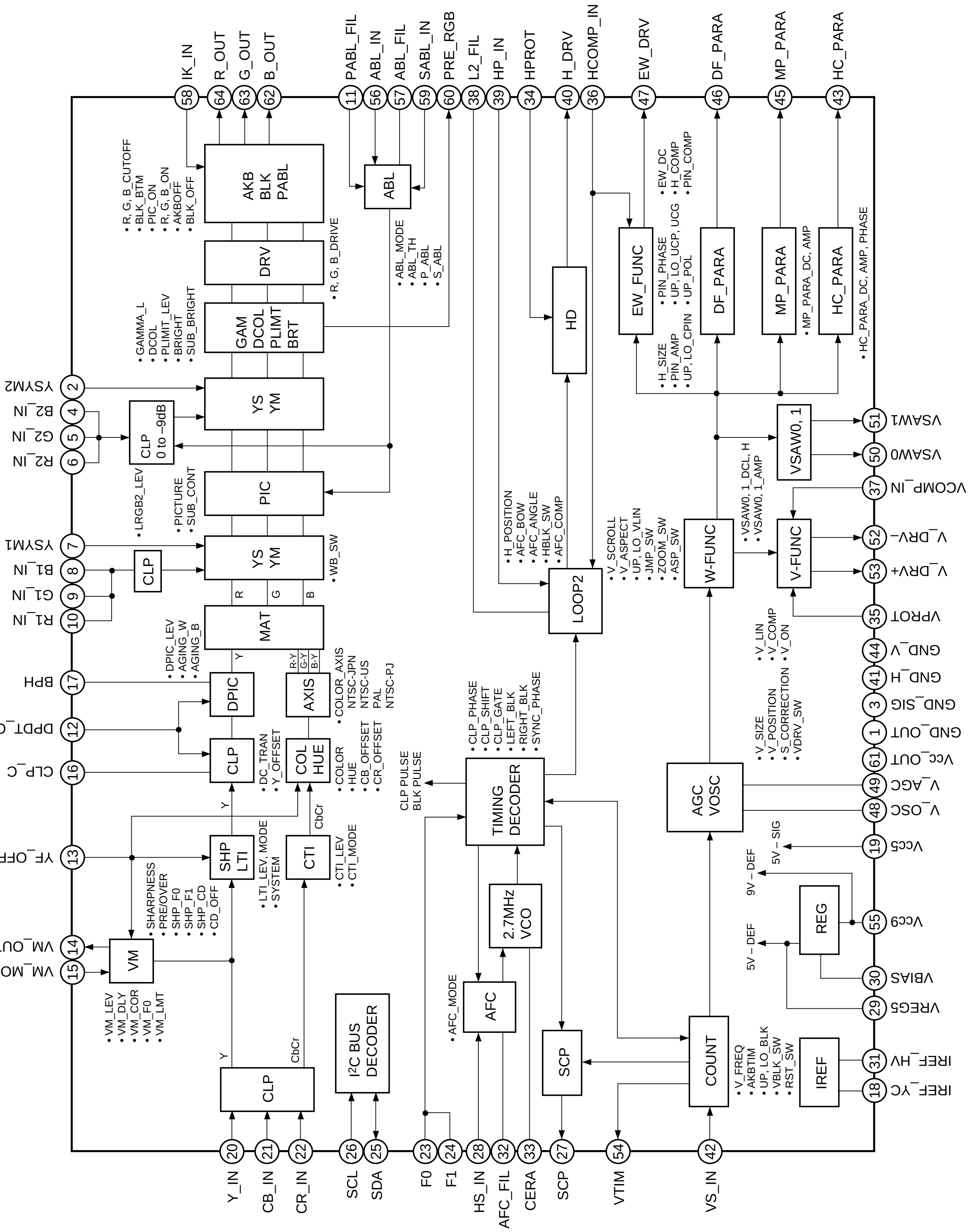
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	–0.3 to +10	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.7	W
	(when mounted on a 50mm × 50mm board)		
• Voltages at each pin		–0.3 to V_{CC}9, V_{CC}_OUT + 0.3	V

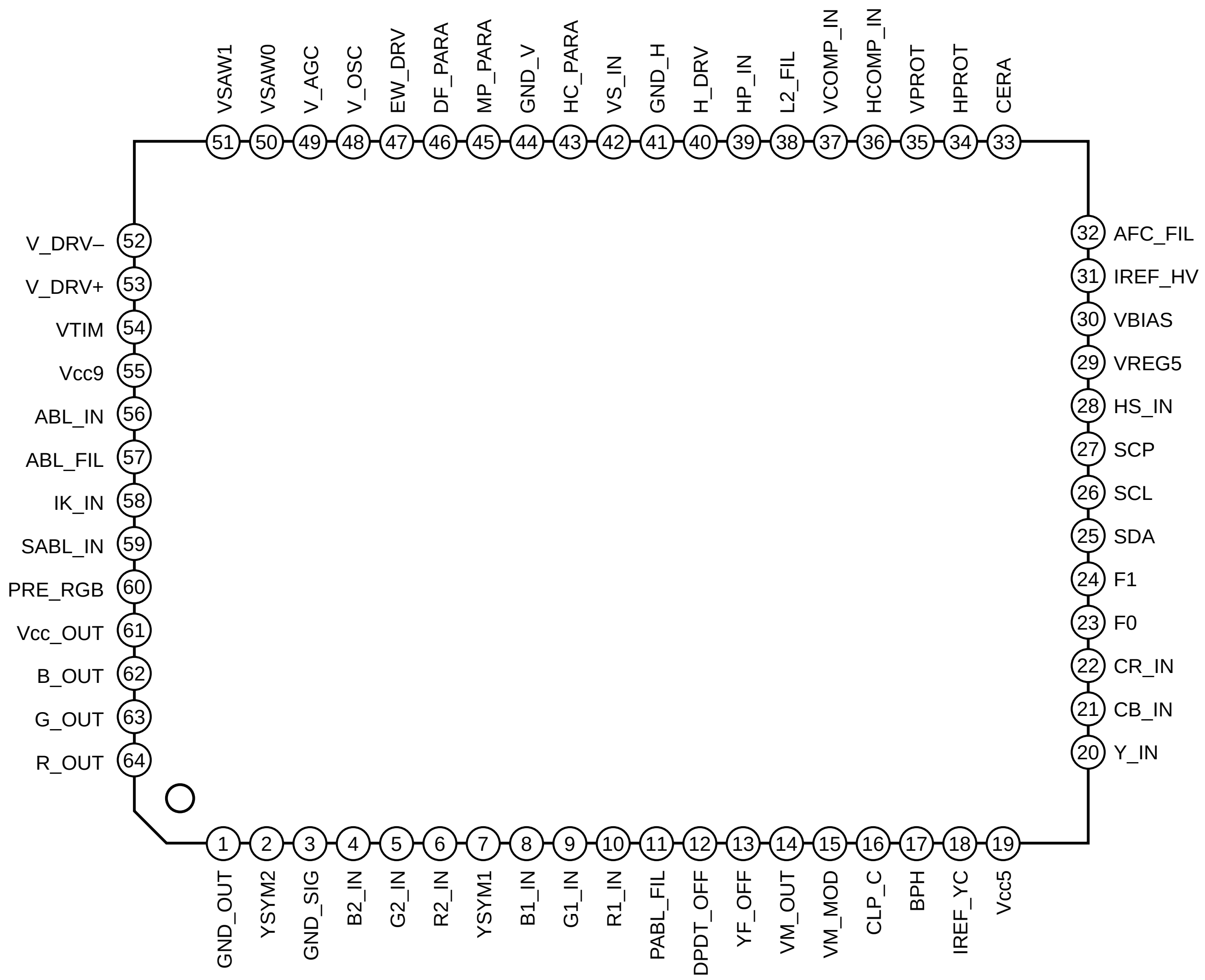
Operating Conditions

Supply voltage	V_{CC}9, V_{CC}_OUT	9.0 ± 0.5	V
	V_{CC}5	5.0 ± 0.25	V

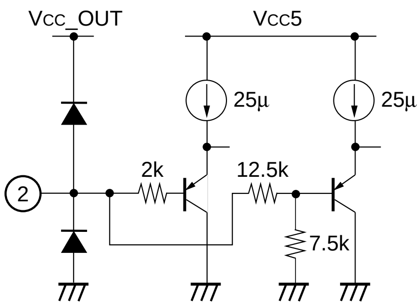
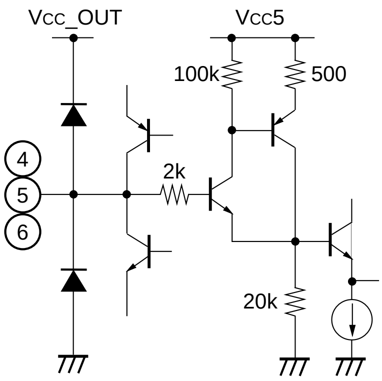
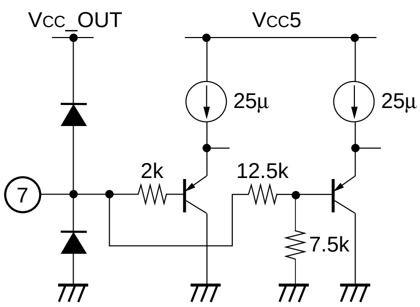
Block Diagram

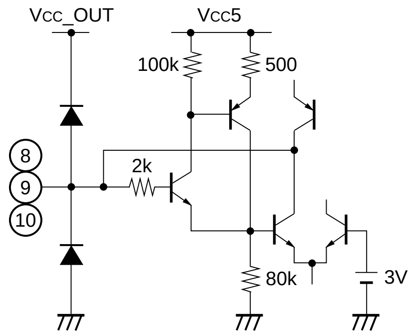
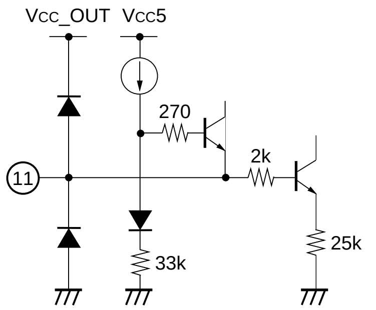
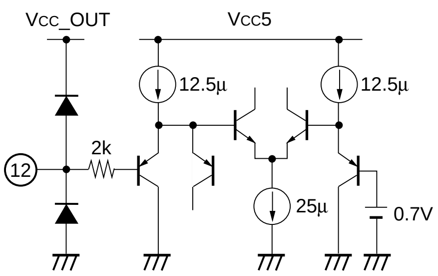
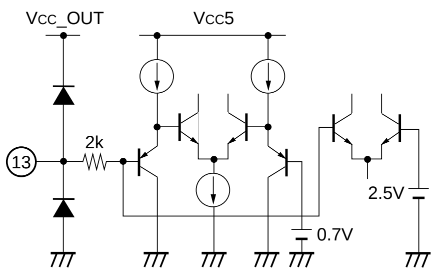
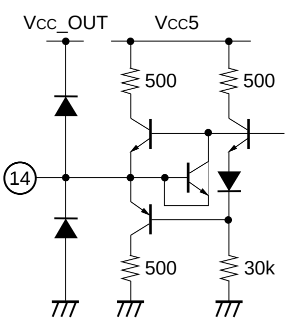


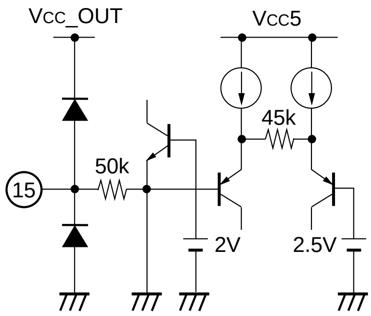
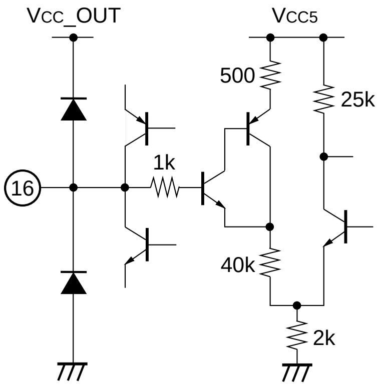
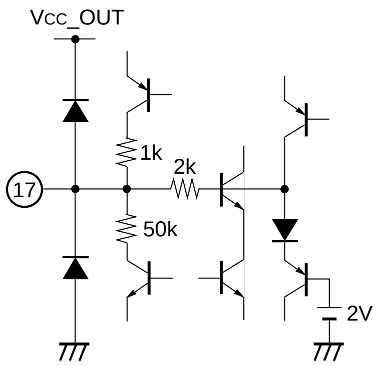
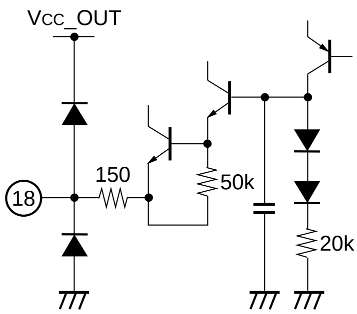
Pin Configuration

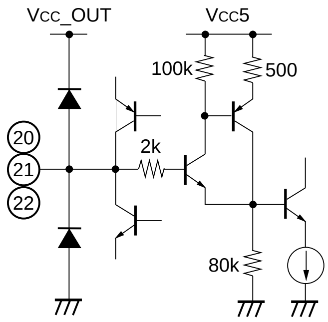
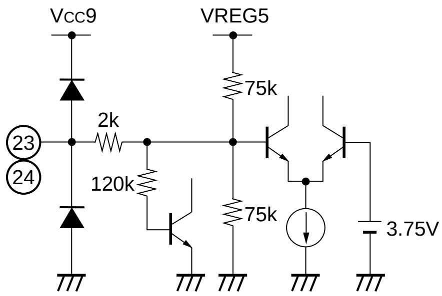
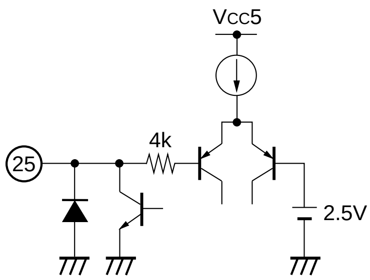
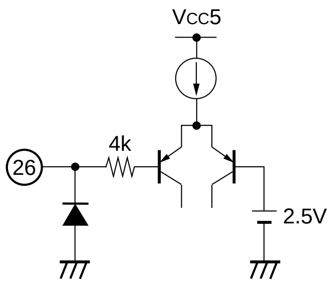
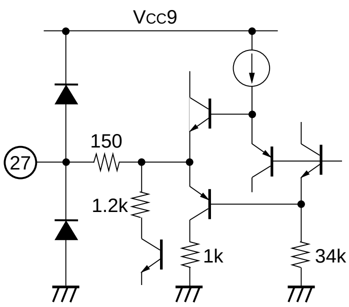


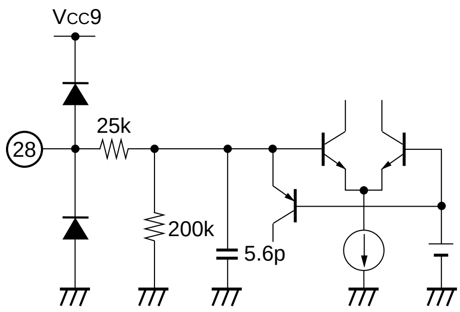
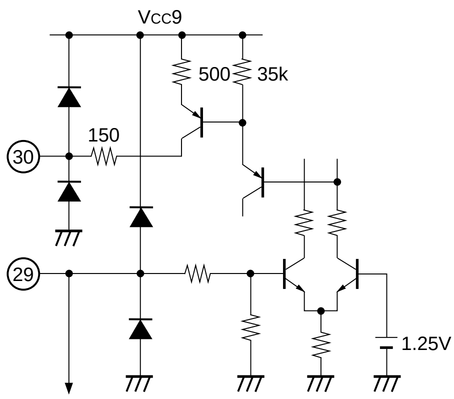
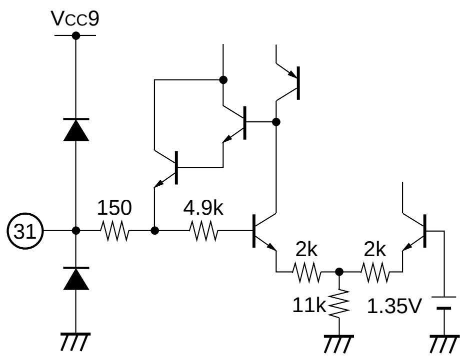
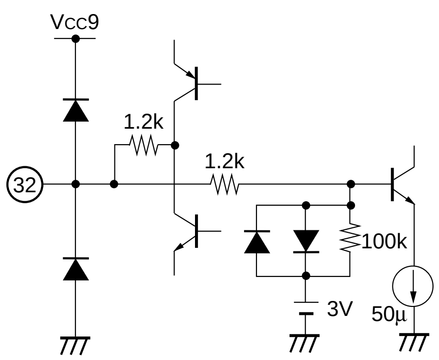
Pin Description

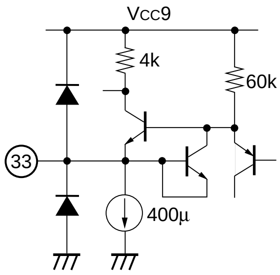
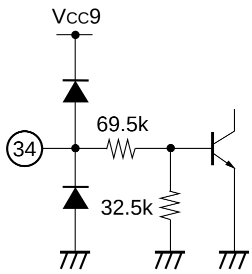
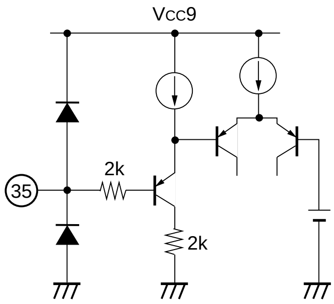
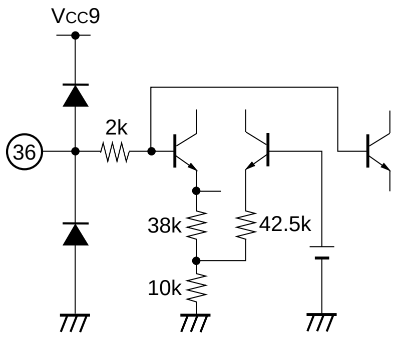
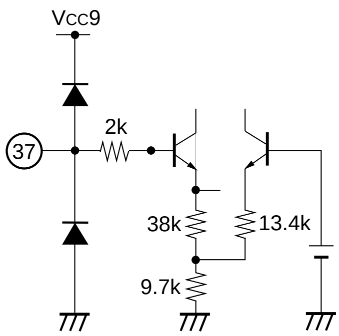
Pin No.	Symbol	Equivalent circuit	Description
1	GND_OUT		GND for RGB_OUT output stage
2	YSYM2		YS2/YM2 control input. When the input level reaches the YM level, VM is OFF. <YS2SW> YS2: ON $V_{IH} \geq 2.3V$ RGB2_IN selected YS2: OFF $V_{IL} \leq 1.5V$ Internal RGB signal selected <YM2SW> YM2: ON $V_{IH} \geq 0.9V$ Internal RGB signal set to –9.5dB YM2: OFF $V_{IL} \leq 0.5V$ Internal RGB signal passed at 0dB * Input voltage range: 0 to 5V
3	GND_SIG		GND for Y/color difference and RGB systems.
4 5 6	B2_IN G2_IN R2_IN		Analog R2, G2 and B2 signal inputs. Input a 0.7Vp-p, 100 IRE (no sync) signal via a capacitor. The pedestal is clamped to 3.2V. * Input voltage range: less than 5V
7	YSYM1		YS1/YM1 control input. When the input level reaches the YM level, VM is OFF. <YS1SW> YS1: ON $V_{IH} \geq 2.3V$ RGB1_IN selected YS1: OFF $V_{IL} \leq 1.5V$ Internal RGB signal selected <YM1SW> YM1: ON $V_{IH} \geq 0.9V$ Internal RGB signal set to –9.5dB YM1: OFF $V_{IL} \leq 0.5V$ Internal RGB signal passed at 0dB * Input voltage range: 0 to 5V

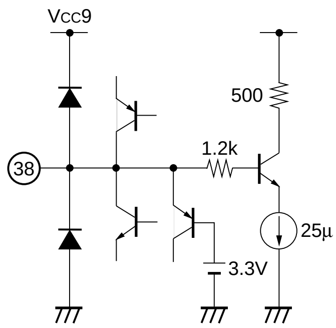
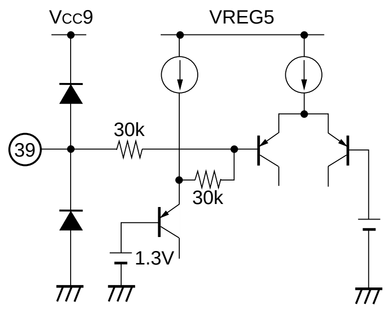
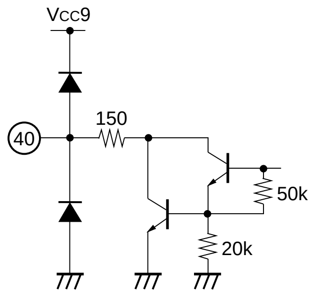
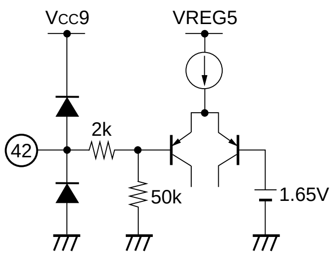
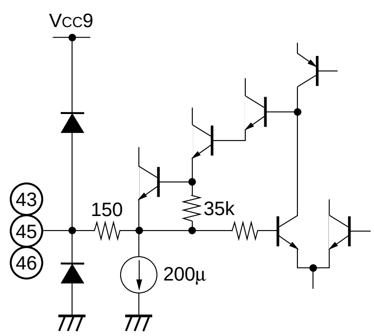
Pin No.	Symbol	Equivalent circuit	Description
8 9 10	B1_IN G1_IN R1_IN		Analog R1, G1 and B1 signal inputs. Input a 0.7Vp-p, 100 IRE (no sync) signal via a capacitor. The pedestal is clamped to 3.75V. * Input voltage range: less than 5V
11	PABL_FIL		Peak hold for peak ABL. A capacitor and resistor are connected between this pin and GND to form a LPF.
12	DPDT_OFF		Muting of the dynamic picture operation (black expansion) and DC transmission ratio signal interval detection can be controlled by this pin. MUTE: ON $V_{IH} \geq 1V$ MUTE: OFF $V_{IL} \leq 0.4V$ * Input voltage range: 0 to 5V
13	YF_OFF		For turning off the VM, sharpness and color. Ternary inputs are supported. COLOR : OFF $V_{IH} \geq 3V$: ON $V_{IL} \leq 2V$ VM, SHP : OFF $V_{IH} \geq 1.0V$: ON $V_{IL} \leq 0.4V$ * Input voltage range: 0 to 5V
14	VM_OUT		VM output. The differential waveforms of the Y signal are output with a positive polarity. The amplitude and phase of this waveform can be adjusted by the I^2C bus. * Allowable load current: –1 to +1mA

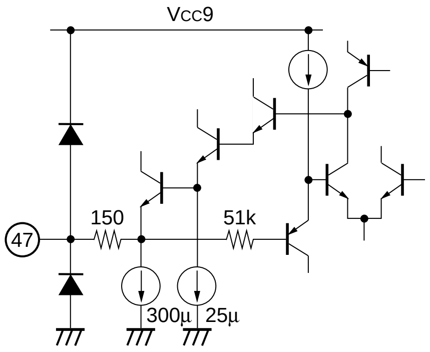
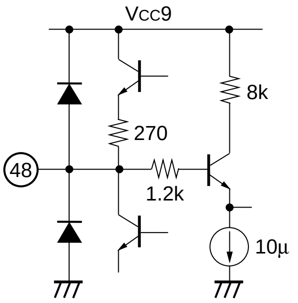
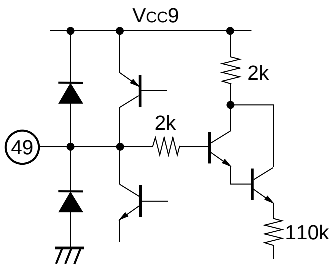
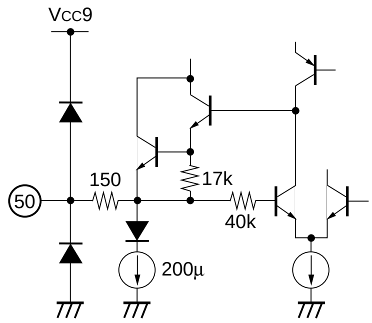
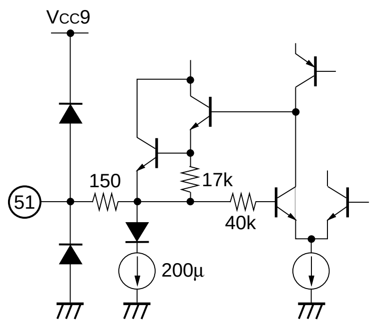
Pin No.	Symbol	Equivalent circuit	Description
15	VM_MOD		VM level modulation. Outputs are 0 at 1.5V or less, modulated from 1.5 to 3.5V, nonmodulated at 3.5V or more. At 1.5V or more output level can be adjusted by VM_LEV (I^2C bus control) * Input voltage range: 0 to 5V
16	CLP_C		Connect a capacitor for Y system clamp. This capacitor also sets the DC transmission ratio.
17	BPH		Connect a capacitor to GND for black detection of the dynamic picture (black stretch)
18	IREF_YC		Reference current setting for Y/color difference signal processing system. Connect to GND via the 4.7kΩ resistor (such as a metal film resistor) with an error of less than 1%.
19	Vcc5		Power supply for Y/color difference, RGB systems and I^2C bus block.

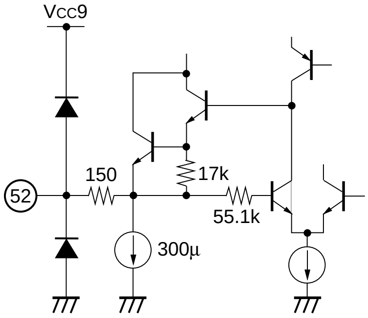
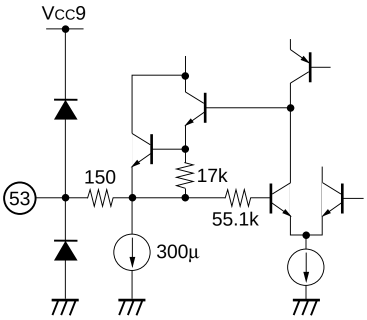
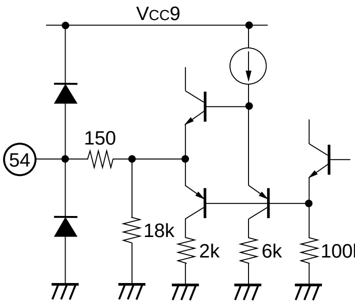
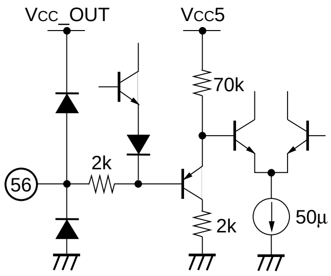
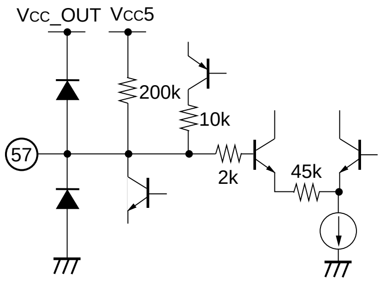
Pin No.	Symbol	Equivalent circuit	Description
20 21 22	Y_IN CB_IN CR_IN		External Y, Cb and Cr inputs Input 0.7Vp-p, 100 IRE Y, Cb and Cr signals (when Cb and Cr are at 100% color bar) via a capacitor. The pedestal is clamped to 3.5V. * Input voltage range: less than 5V
23 24	F0 F1		Horizontal free-running frequency setting (See Table 1 on page 44.)
25	SDA		I^2C bus protocol SDA (Serial Data) input $V_{IH} \geq 3V$ $V_{IL} \leq 1.5V$ $V_{OL} \leq 0.6V$
26	SCL		I^2C bus protocol SCL (Serial Clock) input $V_{IH} \geq 3V$ $V_{IL} \leq 1.5V$
27	SCP		Sand castle pulse output The approximately 0 to 5V CLP pulse is output superimposed on the approximately 0 to 2.5V HBLK and VBLK pulses. * Allowable load current: –0.5 to +2mA

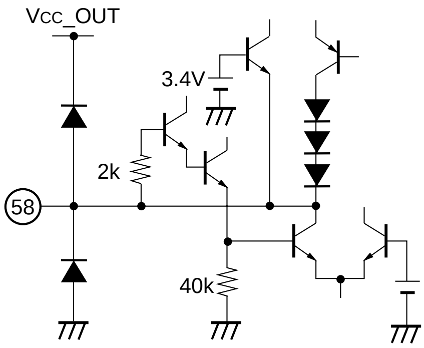
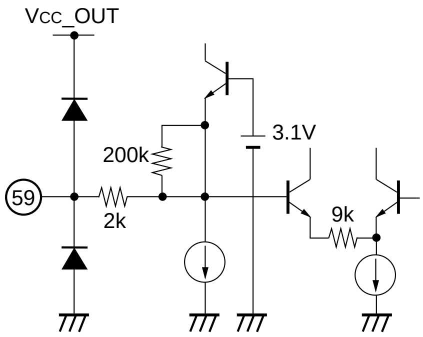
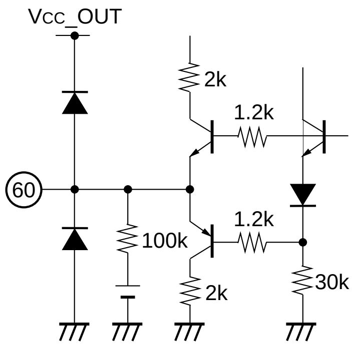
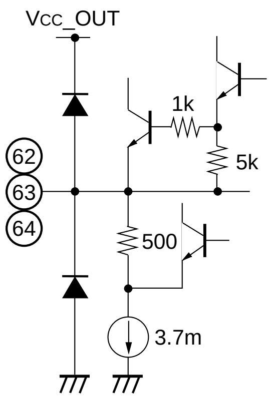
Pin No.	Symbol	Equivalent circuit	Description
28	HS_IN		HSYNC input Input at the sync phase. Positive polarity input VIH ≥ 2.6V VIL ≤ 0.6V * Input DC coupled
29 30	VREG5 VBIAS	 To Vcc for H system and the reference voltage for V system	Connect a NPN-Tr for the external feedback between Pin 30 (VBIAS) and Pin 29 (VREG5) to form 5V shunt regulator. Connect a capacitor of 100µF between Pin 29 (VREG5) and GND.
31	IREF_HV		Reference current setting for H, V deflection systems. A 10kΩ resistor with an error of less than 1% (such as a metal film resistor) is connected between this pin and GND.
32	AFC_FIL		AFC lag-lead filter Connect the RC for the lag-lead filter.

Pin No.	Symbol	Equivalent circuit	Description
33	CERA		Connect a 2.7MHz ceramic oscillator.
34	HPROT		HD output hold-down signal input When this pin is 2V or more for a 7V cycle or longer, the hold-down function operates so that the HD output is held to High Z. In addition, the R, G and B outputs are completely blanked and "1" is output to the status register HNG. To cancel this status, turn the IC power off and then on again.
35	VPROT		V protect input. When the protect function operates, the R, G and B outputs are completely blanked and "1" is output to the status register VNG. See Fig. 14 on page 59 for the input conditions.
36	HCOMP_IN		Voltage input for high voltage fluctuation compensation High voltage compensation is performed for the EW_DRV signal DC amplitude and H_DRV signal phase. The control characteristics can be varied by H_COMP, PIN_COMP and AFC_COMP, respectively. * Input voltage range: 0 to 5V
37	VCOMP_IN		Voltage input for high voltage fluctuation compensation High voltage compensation is performed for the V_DRV signal amplitude. The control characteristics can be varied by V_COMP. * Input voltage range: 0 to 5V

Pin No.	Symbol	Equivalent circuit	Description
38	L2_FIL		Filter for AFC 2nd loop Connect to GND via a capacitor. The AFC phase can also be controlled from this pin by leading current in and out of this capacitor. As the pin voltage rises, the picture shifts to the right. As the pin voltage falls, the picture shifts to the left.
39	HP_IN		H deflection pulse input for H AFC Input low level = 0V and high level = 5V pulse directly or a 5Vp-p pulse via an approximately 0.1µF capacitor.
40	H_DRV		H drive signal output This pin is output by an open collector. Set high level to 5V
41	GND_H		GND for H deflection system.
42	VS_IN		VSYNC input Input at the sync phase. Positive polarity input $V_{IH} \geq 2.6V$ $V_{IL} \leq 0.6V$ * Input DC coupled
43 45 46	HC_PARA MP_PARA DF_PARA		General-purpose V parabola wave output * Allowable load current: –0.2 to +2.6mA

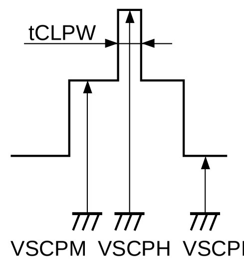
Pin No.	Symbol	Equivalent circuit	Description
44	GND_V		GND for V deflection system
47	EW_DRV		V parabola wave output This is used to compensate the horizontal amplitude and the horizontal pin distortion. * Allowable load current: –0.2 to +2.6mA
48	V_OSC		V sawtooth wave generation. Connect to GND via a 0.1µF capacitor. For the capacitor, use a PP (polypropylene) capacitor, or similar capacitor with a small tanδ.
49	V_AGC		Sample-and-hold for AGC which maintains the V sawtooth wave at a constant amplitude Connect to GND via a 0.1µF capacitor.
50	VSAW0		V sawtooth wave (VSAW0) output * Allowable load current: –0.2 to +2.6mA
51	VSAW1		V sawtooth wave (VSAW1) output * Allowable load current: –0.2 to +2.6mA

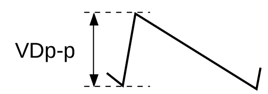
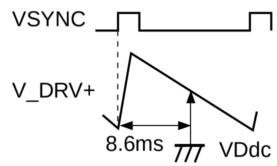
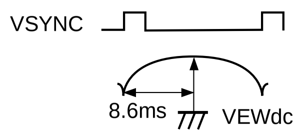
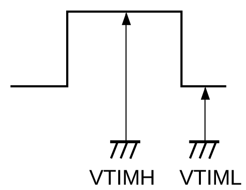
Pin No.	Symbol	Equivalent circuit	Description
52	V_DRV–		V sawtooth wave output (opposite polarity of V_DRV+) * Allowable load current: –0.3 to +1.7mA
53	V_DRV+		V sawtooth wave output (opposite polarity of V_DRV–) * Allowable load current: –0.3 to +1.7mA
54	VTIM		V timing pulse output Positive polarity pulses from 0 to 5V. This pin corresponds to VBLK position of RGB output during high period.
55	Vcc9		Power supply for V deflection system.
56	ABL_IN		ABL control signal input This pin functions as the average value. The ABL_IN threshold voltage can be varied by the I^{2}C bus ABL_TH. * Input voltage range: 0 to 5V
57	ABL_FIL		Connect a capacitor to form the LPF for the ABL_IN input signal.

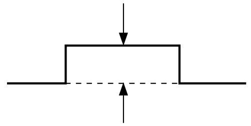
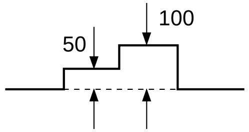
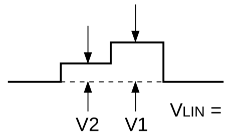
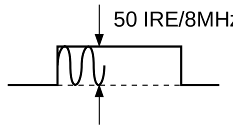
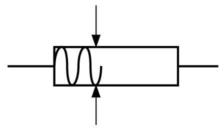
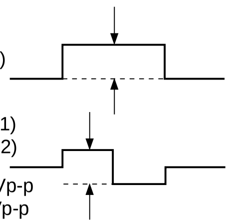
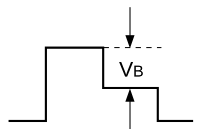
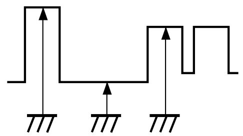
Pin No.	Symbol	Equivalent circuit	Description
58	IK_IN		The reference pulses are returned to this pin. The CRT cathode current IK is converted to a voltage and input via a capacitor. This signal is clamped to 2.8V at the V retrace timing of the V blanking. * Input voltage range: less than 5V
59	SABL_IN		SABL compensation signal input PRE_RGB output signal (Pin 60) can be input via a external filter. * Input voltage range: 0 to 5V
60	PRE_RGB		Mixed RGB signal output for high voltage fluctuation compensation and SABL compensation. * Allowable load current: –0.8 to +0.4mA
61	Vcc_OUT		Power supply for RGB system output stage.
62 63 64	B_OUT G_OUT R_OUT		R, G and B signal outputs. A 2.6Vp-p signal is output at 100 IRE. * Allowable load current: –3.7 to +5mA

Electrical Characteristics Measurement conditions: Ta = 25°C, $V_{CC}9$ = V_{CC}_OUT = 9V, $V_{CC}5$ = 5V, GND_OUT = GND_SIG = GND_H = GND_V = 0V

Measures the following after setting the I^2C bus register as shown in "I^2C bus Register Initial Settings".

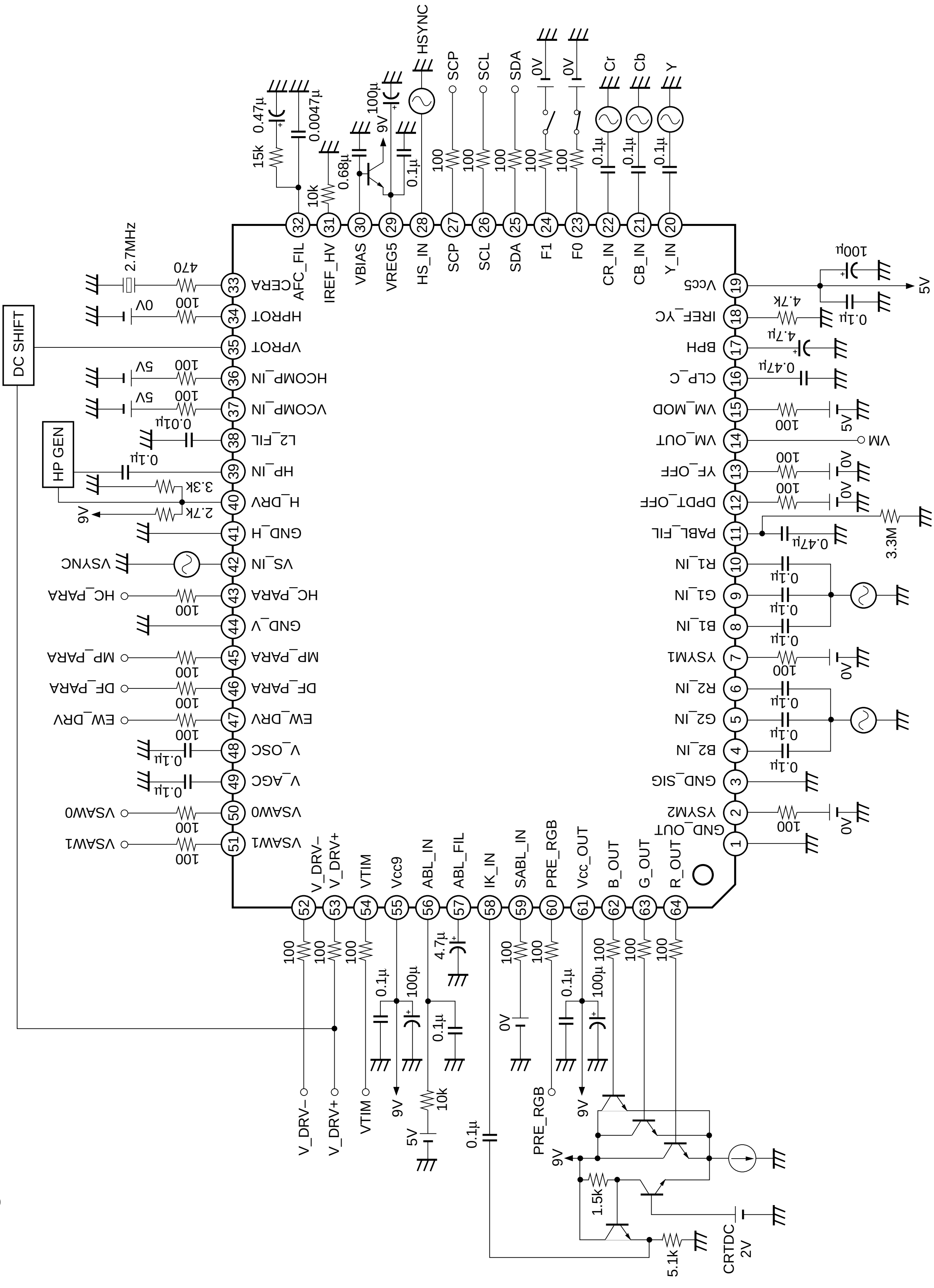
No.	Item	Symbol	Measurement conditions	Measurement pin	Measurement contents	Min.	Typ.	Max.	Unit
1	5V system current consumption	ICC5		19	Measure the pin inflow current.	55	80	115	mA
2	9V system current consumption	ICC9		55, 61	Measure the pin inflow current.	18	33	52	mA
3	5V regulator current consumption	ICCreg		*29	* Measure the collector current of the external NPN-Tr.	17	27	38	mA
4	5V regulator voltage	VREG		29	Measure the pin voltage.	4.8	5	5.2	V
Deflection system items									
5	Horizontal free-running frequency 1	fHFR1	AFC_MODE = 0, F0: 0V, F1: 0V	40	Measure the output frequency.	15.4	15.74	16.1	kHz
6	Horizontal free-running frequency 2	fHFR2	AFC_MODE = 0, F0: Open, F1: 0V			31.1	31.5	31.9	kHz
7	Horizontal free-running frequency 3	fHFR3	AFC_MODE = 0, F0: 0V, F1: Open			33.4	33.83	34.2	kHz
8	Horizontal free-running frequency 4	fHFR4	AFC_MODE = 0, F0: Open, F1: 5V			37.2	37.6	38.0	kHz
9	Horizontal free-running frequency 5	fHFR5	AFC_MODE = 0, F0: Open, F1: Open			44.7	45.1	45.5	kHz
10	Horizontal sync pull-in range	ΔfHR	Input HSYNC		Normalize the pull-in range when the HSYNC input frequency is shifted from the free-running frequency. (Confirm the HLOCK = 1.)	—	±3	—	%
11	H_DRV output pulse duty	Hdduty			Measure the pulse duty of H_DRV output.	43.4	43.74	44	%
12	SCP CLP output pulse width	tCLPW	Measure the pulse width for the section where the SCP CLP output is high level, and normalize it with the horizontal cycle.	27		3.2	3.7	4.2	%
13	SCP CLP output high level	VSCPH	Measure the SCP CLP output high level.			4.7	5	—	V
14	SCP BLK output high level	VSCPM	Measure the SCP BLK output high level.			2.35	2.5	2.65	V
15	SCP output low level	VSCPL	Measure the SCP output low level.			0.05	0.2	0.4	V

No.	Item	Symbol	Measurement conditions	Measurement pin	Measurement contents	Min.	Typ.	Max.	Unit
16	V_DRV output amplitude	VDp-p	Input VSYNC.	52, 53	Measure the V_DRV output Vp-p 	1.07	1.2	1.3	V
17	V_DRV output center potential	VDdc				3.39	3.5	3.63	V
18	EW_DRV output amplitude	VEWp-p		47	Measure the EW_DRV output Vp-p 	0.39	0.54	0.65	V
19	EW_DRV output center potential	VEWdc				3.78	4	4.16	V
20	VTIM output high level	VTIMH		54		4.65	5	5.05	V
21	VTIM output low level	VTIML				0.15	0.25	0.35	V

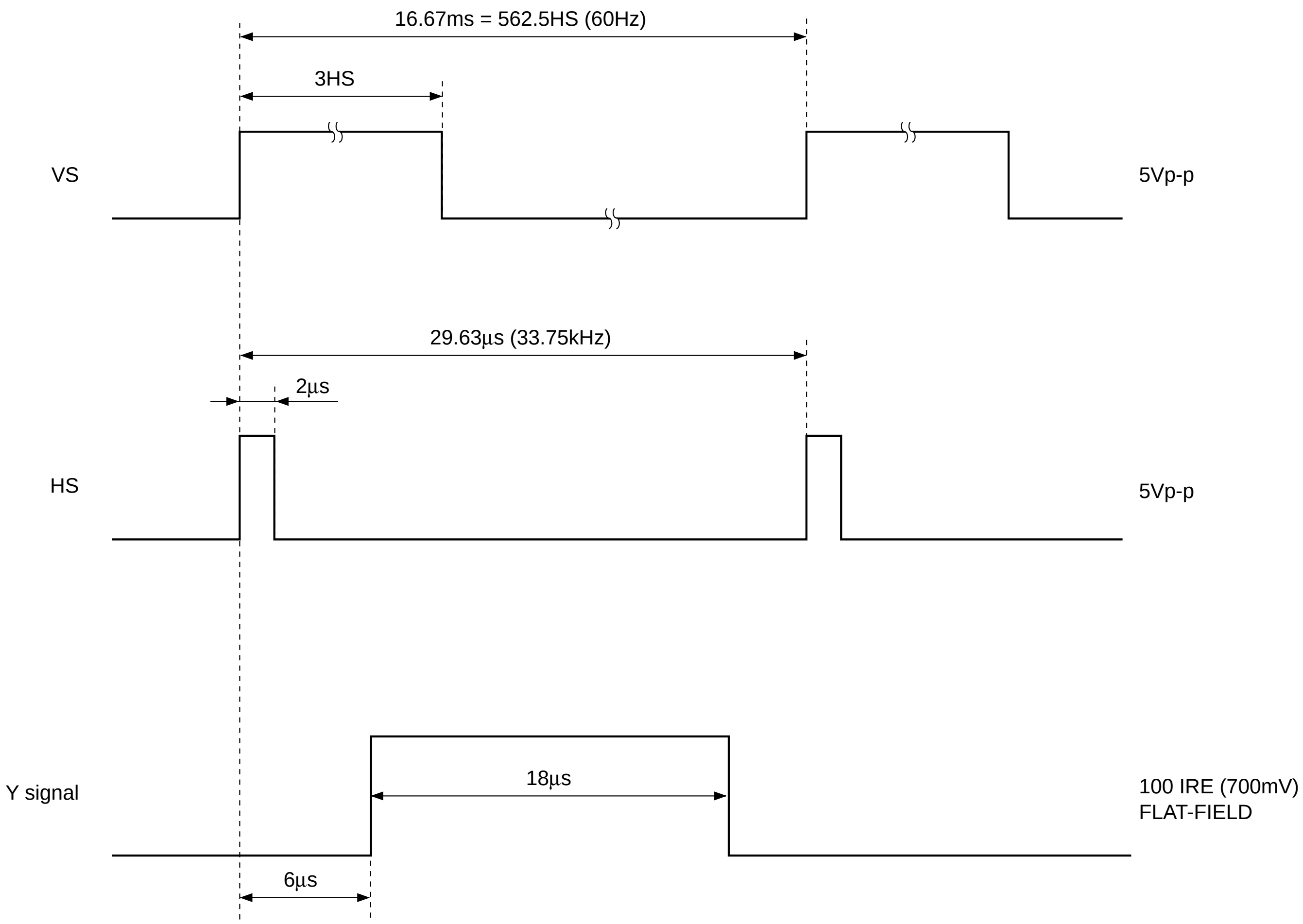
No.	Item	Symbol	Measurement conditions	Measurement pin	Measurement contents	Min.	Typ.	Max.	Unit
Signal system items									
22	RGB output	V_{RGB}	 100 IRE signal input to Y_IN (Pin 20)	62, 63, 64	Measure the output level.	2.18	2.56	2.84	V
23	RGB linearity	V_{LIN}	 Staircase wave input to Y_IN (Pin 20)		 $V_{LIN} = \frac{V1}{V2 \times 2} \times 100$	95	100	104	%
24	RGB1 gain	G_{L1}	100 IRE signal input to G1_IN (Pin 9), YSYM1 (Pin 7) = 5V	63	Compare the output level to V_{RGB}	–0.8	–0.2	0.3	dB
25	RGB2 gain	G_{L2}	100 IRE signal input to G2_IN (Pin 5), YSYM2 (Pin 2) = 5V		Compare the output level to V_{RGB}	–0.8	–0.1	0.8	dB
26	VM output	V_{VM}	 Sine wave to Y_IN (Pin 20)	14	 Measure the VM_OUT level.	1.75	2.56	3.15	V
27	HUE center	θ_B		62	 $\theta_B = \tan^{-1} \frac{\text{VB level with Cr input}}{\text{VB level with Cb input}}$	–8	–4.7	–1	deg
28	BRIGHT center Rch	V_{BRT-R}		64	 $V_{BRT} = V_{PED} - V_{REFP}$	–420	–250	–45	mV
29	BRIGHT center Gch	V_{BRT-G}		63		–420	–250	–45	mV
30	BRIGHT center Bch	V_{BRT-B}		62		–420	–250	–45	mV
31	RGB output VBLK level	V_{BLK-R}		64		200	400	550	mV

Electrical Characteristics Measurement Circuit

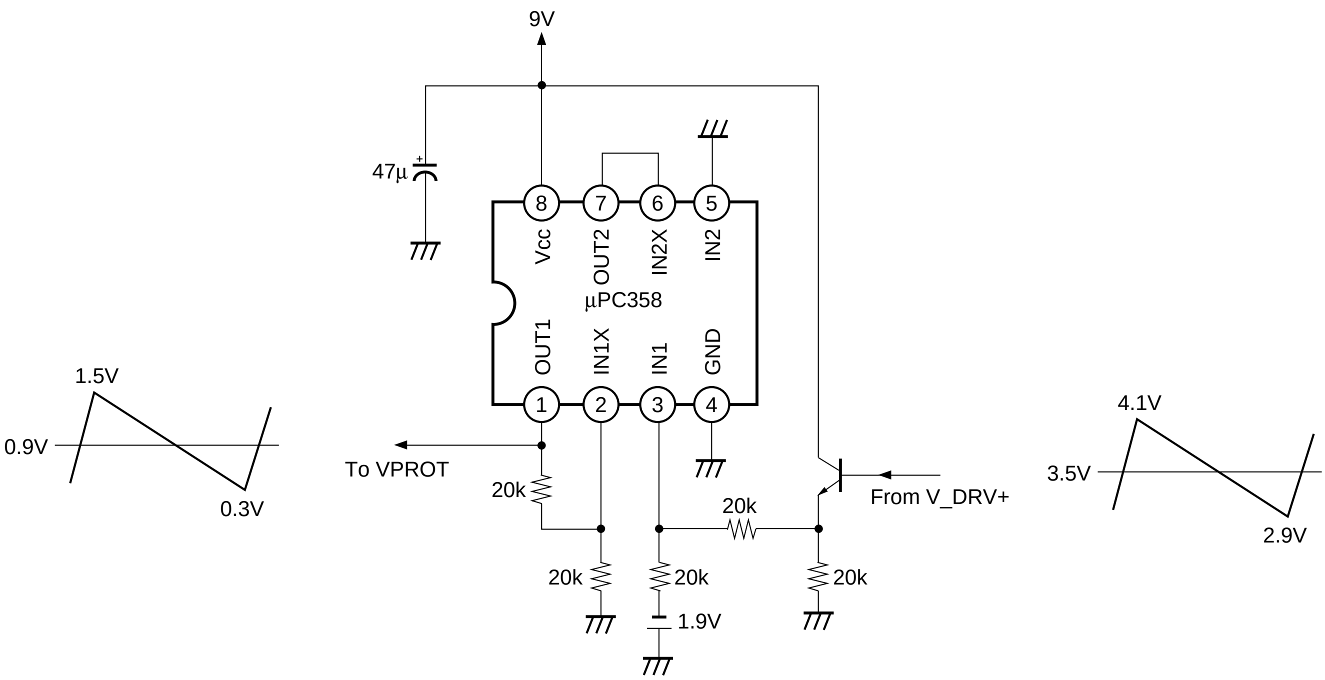
Signal sources ⊙ are all GND unless otherwise specified in the Measurement conditions column of Electrical Characteristics.



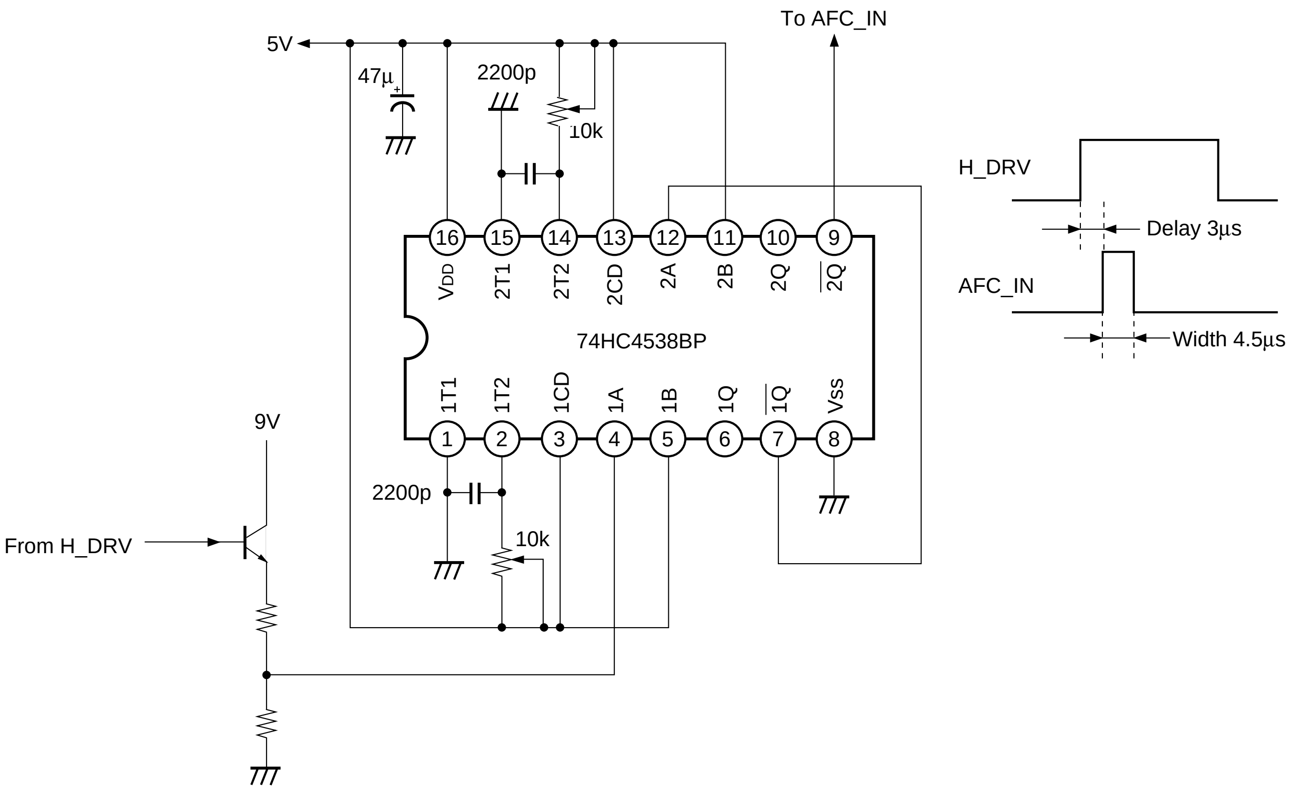
Electrical Characteristics Measurement Input Signals



DC SHIFT



HP GEN.



Electrical Characteristics Measurement Conditions "I²C bus Register Initial Settings"

Register name	No. of bits	Setting	Description
PIC_ON	1	1	R, G, B outputs on
R_ON	1	1	R output on
G_ON	1	1	G output on
B_ON	1	1	B output on
DCOL	2	0	DCOL off
WB_SW	1	0	OFF
GAMMA_L	1	0	GAMMA fine adjustment off
PICTURE	6	3Fh	Max.
BLK_BTM	2	0	Min.
HUE	6	1Fh	Center
COL_AXIS	2	3	NTSC Japan
COLOR	6	1Fh	Center
CTI_LEV	2	0	CTI off
BRIGHT	6	1Fh	Center
S_ABL	2	0	SABL off
SHARPNESS	6	1Fh	Center
LTI_LEV	2	0	LTI off
R_DRIVE	6	29h	0dB
PLIMIT_LEV	2	3	Max.
G_DRIVE	6	29h	0dB
ABL_MODE	2	0	Picture/Only
B_DRIVE	6	29h	0dB
CTI_MODE	2	0	B/W both sides improvement
SUB_BRIGHT	6	1Fh	Center
GAMMA	2	0	GAMMA off
R_CUTOFF	6	1Fh	Center
LTI_MODE	2	0	B/W both sides improvement
G_CUTOFF	6	1Fh	Center
DPIC_LEV	2	0	OFF
B_CUTOFF	6	1Fh	Center
DC_TRAN	2	0	DC transmission ratio 100%
SUB_CONT	4	7h	Center
LRGB2_LEV	4	Fh	0dB
P_ABL	4	Fh	Max.
ABL_TH	4	0	Min.

Register name	No. of bits	Setting	Description
CB_OFFSET	6	1Fh	Center
AGING_W	1	0	OFF
AGING_B	1	0	OFF
CR_OFFSET	6	1Fh	Center
SYSTEM	2	2	HD mode
Y_OFFSET	4	7h	Center
VM_LEV	2	3	Max.
SHP_F0	1	1	16MHz
CD_OFF	1	1	SHP_CD function off
SHP_CD	2	0	OFF
SHP_F1	2	0	OFF
PRE/OVER	2	1	1:1
VM_COR	2	0	OFF
VM_F0	2	0	Min.
VM_LMT	2	3	Maximum limit
VM_DLY	2	0	VM output delay Max.
AKB_TIM	5	0h	Bch REF-P 10H
BLK_OFF	1	0	Blanking on
AKBOFF	1	0	AKB mode
UP_BLK	4	0h	VBLK-end 0H after Bch REF-P
LO_BLK	4	0h	VBLK-start 0H before VSYNC
V_SIZE	6	1Fh	Center
V_ON	1	1	V_DRV output on
EW_DC	1	0	OFF
V_POSITION	6	1Fh	Center
VSAW0_DCH	2	1	Center
V_LIN	4	7h	Center
S_CORRECTION	4	0h	Min.
H_SIZE	6	1Fh	Center
UP_UCP	2	0	Most inside point compensated
PIN_AMP	6	1Fh	Center
LO_UCP	2	0	Most inside point compensated
UP_CPIN	6	1Fh	Center
UP_UCG	2	0	Min.
LO_CPIN	6	1Fh	Center
LO_UCG	2	0	Min.

Register name	No. of bits	Setting	Description
PIN_PHASE	6	1Fh	Center
UC_POL	1	0	H-size small on compensated parts
VBLK_SW	1	1	UP/LO_BLK only
H_POSITION	6	1Fh	Center
CLP_SHIFT	1	0	CLP_PHASE settings
SYNC_PHASE	2	0	HSYNC delay 0%
AFC_BOW	6	1Fh	Center
AFC_MODE	2	2	Medium gain
AFC_ANGLE	6	1Fh	Center
RST_SW	1	0	Retrace after VSYNC
LEFT_BLK	6	1Fh	Center
CLP_PHASE	2	3	Min.
RIGHT_BLK	6	1Fh	Center
CLP_GATE	1	0	Gating function off
HBLK_SW	1	1	HBLK control enable
V_ASPECT	6	0h	Min.
ZOOM_SW	1	0	ZOOM_SW off
JMP_SW	1	0	JMP_SW off
V_SCROLL	6	1Fh	Center
VFREQ	2	1	60Hz mode
UP_VLIN	4	0h	Min.
LO_VLIN	4	0h	Min.
V_COMP	4	0h	Compensation off
H_COMP	4	0h	Compensation off
VSAW0_DCL	4	Fh	Center
VSAW1_DC	4	7h	Center
VSAW0_AMP	5	Fh	Amplitude off
PIN_COMP	3	0	Compensation off
VSAW1_AMP	5	Fh	Amplitude off
AFC_COMP	3	0	Compensation off
MP_PARA_DC	4	7h	Center
MP_PARA_AMP	4	0h	Amplitude off
HC_PARA_DC	6	1Fh	Center
ASP_SW	1	0	OFF
VDRV_SW	1	0	OFF
HC_PARA_AMP	6	1Fh	Amplitude off
HC_PARA_PHASE	6	1Fh	Center

Definition of I²C bus Registers
Slave address 86H: Slave Receiver 87H: Slave Transmitter
Control Register (Register Tables *: Undefined)

Sub Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XXX00000 00h	PIC_ON	R_ON	G_ON	B_ON	DCOL		WB_SW	GAMMA_L
XXX00001 01h	PICTURE						BLK_BTM	
XXX00010 02h	HUE						COL_AXIS	
XXX00011 03h	COLOR						CTI_LEV	
XXX00100 04h	BRIGHT						S_ABL	
XXX00101 05h	SHARPNESS						LTI_LEV	
XXX00110 06h	R_DRIVE						PLIMIT_LEV	
XXX00111 07h	G_DRIVE						ABL_MODE	
XXX01000 08h	B_DRIVE						CTI_MODE	
XXX01001 09h	SUB_BRIGHT						GAMMA	
XXX01010 0Ah	R_CUTOFF						LTI_MODE	
XXX01011 0Bh	G_CUTOFF						DPIC_LEV	
XXX01100 0Ch	B_CUTOFF						DC_TRAN	
XXX01101 0Dh	SUB_CONT				LRGB2_LEV			
XXX01110 0Eh	P_ABL				ABL_TH			
XXX01111 0Fh	CB_OFFSET						AGING_W	AGING_B
XXX10000 10h	CR_OFFSET						SYSTEM	
XXX10001 11h	Y_OFFSET				VM_LEV		SHP_F0	CD_OFF
XXX10010 12h	SHP_CD		*	0	SHP_F1		PRE/OVER	
XXX10011 13h	VM_COR		VM_F0		VM_LMT		VM_DLY	
XXX10100 14h	AKBTIM					*	BLK_OFF	AKBOFF
XXX10101 15h	UP_BLK				LO_BLK			
XXX10110 16h	V_SIZE						V_ON	EW_DC
XXX10111 17h	V_POSITION						VSAW0_DCH	
XXX11000 18h	V_LIN				S_CORRECTION			
XXX11001 19h	H_SIZE						UP_UCP	
XXX11010 1Ah	PIN_AMP						LO_UCP	
XXX11011 1Bh	UP_CPIN						UP_UCG	
XXX11100 1Ch	LO_CPIN						LO_UCG	
XXX11101 1Dh	PIN_PHASE						UC_POL	VBLK_SW
XXX11110 1Eh	H_POSITION						CLP_SHIFT	SYNC_PHASE
XXX11111 1Fh	AFC_BOW						AFC_MODE	
XX100000 20h	AFC_ANGLE						0	RST_SW
XX100001 21h	LEFT_BLK						CLP_PHASE	
XX100010 22h	RIGHT_BLK						CLP_GATE	HBLK_SW
XX100011 23h	V_ASPECT						ZOOM_SW	JMP_SW
XX100100 24h	V_SCROLL						VFREQ	
XX100101 25h	UP_VLIN				LO_VLIN			
XX100110 26h	V_COMP				H_COMP			
XX100111 27h	VSAW0_DCL				VSAW1_DC			
XX101000 28h	VSAW0_AMP					PIN_COMP		
XX101001 29h	VSAW1_AMP					AFC_COMP		
XX101010 2Ah	MP_PARA_DC				MP_PARA_AMP			
XX101011 2Bh	HC_PARA_DC						ASP_SW	VDRV_SW
XX101100 2Ch	HC_PARA_AMP						0	0
XX101101 2Dh	HC_PARA_PHASE						0	0

Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	INTER	HCENT	HLOCK	IKR	HNG	VNG

Description of Registers

Register name (Number of bits) Description

1. Y Signal Block Registers

SYSTEM (2) Selects the signal band

		Sharpness f0 (SHP_F0 = 0)
	0 = NORMAL mode	3MHz
	1 = FF mode	6MHz
	2 = HD mode	12MHz
	3 = DTV mode	18MHz

SHARPNESS (6) Sharpness gain control
00h = –10dB
1Fh = +2dB
3Fh = +8dB

SHP_F0 (1) Sharpness f0 setting
0 = 3MHz@NORMAL mode
1 = 4MHz@NORMAL mode

SHP_F1 (2) High f0 (4.2/5.6MHz@NORMAL mode) sharpness gain control
0 = 0dB
3 = +3dB

SHP_CD (2) Sharpness gain control in part of high color saturation
When Cr input signal is 100% color.
0 = 0dB
3 = +6dB

CD_OFF (1) SHP_CD ON/OFF
0 = ON
1 = OFF

LTI_LEV (2) LTI (Luminance Transient Improvement) control
0 = LTI off
1 = LTI weak
2 = LTI medium
3 = LTI strong

LTI_MODE (2) LTI mode setting
0 = both of black and white side improved
1 = black side improved
2 = white side improved
3 = prohibited

VM_LEV	(2)	VM_OUT level control 0 = VM off 1 = Weak 2 = Medium 3 = Strong
VM_DLY	(2)	VM_OUT phase control; defined by difference in phase from R_OUT 0 = Short 3 = Long
VM_COR	(2)	VM_OUT coring level setting 0 = OFF 1 = ±5% coring 2 = ±10% coring 3 = ±15% coring Coring level not changed if limiter level changed.
VM_F0	(2)	VM_OUT f0 setting 0 = Low 1 = Medium 2 = High 3 = prohibited
VM_LMT	(2)	VM_OUT limiter level setting 0 = OFF 1 = ±83% 2 = ±67% 3 = ±50%
Y_OFFSET	(4)	DC_OFFSET canceling for Y signal 0h = –32mV 7h = 0mV Fh = +37mV
DPIC_LEV	(2)	Dynamic picture (black expansion) control 0 = OFF 1 = 25 IRE knee down 2 = 30 IRE knee down 3 = 35 IRE knee down
DC_TRAN	(2)	Y system DC transmission ratio setting 0 = 103% 1 = 100% 2 = 90% 3 = 80%

PRE/OVER (2) Pre-Shoot/Over-Shoot ratio setting
0 = 1:1.5
1 = 1:1
2 = 1.5:1
3 = 2:1

AGING_W (1) White (80 IRE) output aging mode ON/OFF switch
0 = OFF
1 = ON

AGING_B (1) All black (0 IRE) output aging mode ON/OFF switch
0 = OFF
1 = ON

2. Color Difference Block Registers

COL_AXIS (2) Color detection axis setting
0 = mode for NTSC Projector
1 = mode for PAL/SECAM
2 = mode for NTSC US
3 = mode for NTSC JAPAN

HUE (6) HUE control
00h = –33deg. Flesh color appears red.
1Fh = Center
3Fh = +33deg. Flesh color appears green.

COLOR (6) Color gain control
00h = Color OFF
1Fh = 0dB
3Fh = +4.8dB

CTI_LEV (2) CTI (Chrominance Transient Improvement) setting
0 = CTI off
1 = CTI weak
2 = CTI medium
3 = CTI strong

CTI_MODE (2) CTI mode setting
0 = both of black and white side improved
1 = black side improved
2 = white side improved
3 = prohibited

CB_OFFSET (6) DC_OFFSET canceling for Cb signal

00h = Bch output DC –62mV Gch output DC +10mV
1Fh = Bch output DC ±0mV Gch output DC ±0mV
3Fh = Bch output DC +64mV Gch output DC –12mV
(@PICTURE = 3F, COLOR = 1F, COL_AXIS = 3)

CR_OFFSET (6) DC_OFFSET canceling for Cr signal

00h = Rch output DC –62mV Gch output DC +20mV
1Fh = Rch output DC ±0mV Gch output DC ±0mV
3Fh = Rch output DC +66mV Gch output DC –24mV
(@PICTURE = 3F, COLOR = 1F, COL_AXIS = 3)

3. RGB Block Registers

PIC_ON (1) RGB output including AKB reference pulse ON/OFF (0 for power ON reset)

0 = RGB output OFF (complete blanking status)
1 = RGB output ON

R_ON (1) Rch video output ON/OFF (AKB reference pulse cannot be turned ON/OFF)

0 = Rch video output OFF
1 = Rch video output ON

G_ON (1) Gch video output ON/OFF (AKB reference pulse cannot be turned ON/OFF)

0 = Gch video output OFF
1 = Gch video output ON

B_ON (1) Bch video output ON/OFF (AKB reference pulse cannot be turned ON/OFF)

0 = Bch video output OFF
1 = Bch video output ON

DCOL (2) Dynamic color mode setting

0 = Dynamic Color OFF
1 = ON1 R: 98%, G: 100%, B: 102.5%
2 = ON2 R: 97%, G: 100%, B: 105%
3 = ON3 R: 96%, G: 100%, B: 106%

PICTURE (6) Picture gain control (enabled for input signal excluding LRGB2)

00h = –13dB
3Fh = 0dB

BLK_BTM (2) RGB output bottom limiter level control (for Blanking and Signal)

0 = (AKB reference pulse DC voltage) –1.25V
3 = (AKB reference pulse DC voltage) –0.65V

PLIMIT_LEV (2) RGB signal amplitude limiter level setting
0 = 115 IRE
1 = 123 IRE
2 = 130 IRE
3 = 136 IRE

ABL_MODE (2) ABL mode setting
0 = PICTURE ABL ONLY mode
1 = PICTURE/BRIGHT mode 1 (BRIGHT ABL gain min.) : weak
2 = PICTURE/BRIGHT mode 2 (BRIGHT ABL gain middle) : medium
3 = PICTURE/BRIGHT mode 3 (BRIGHT ABL gain max.) : strong

BRIGHT (6) BRIGHT control
00h = –14 IRE
1Fh = ±0 IRE
3Fh = +14 IRE

GAMMA (2) RGB output GAMMA correction amount control
0 = OFF
1 = Min. (+5 IRE for 40 IRE input)
2 = Mid. (+10 IRE for 40 IRE input)
3 = Max. (+15 IRE for 40 IRE input)

GAMMA_L (1) GAMMA differential correction ON/OFF
0 = OFF
1 = ON (+2.5 IRE for 40 IRE input)

R_DRIVE (6) Rch drive gain control
00h = –4.67dB
29h = 0dB (2.56Vp-p at PICTURE max.)
3Fh = +1.33dB

G_DRIVE (6) Gch drive gain control
00h = –4.67dB
29h = 0dB (2.56Vp-p at PICTURE max.)
3Fh = +1.33dB

B_DRIVE (6) Bch drive gain control
00h = –4.67dB
29h = 0dB (2.56Vp-p at PICTURE max.)
3Fh = +1.33dB

SUB_BRIGHT (6) SUB_BRIGHT control
00h = –14 IRE
1Fh = ±0 IRE
3Fh = +14 IRE

R_CUTOFF	(6)	Rch cut-off control (Rch reference pulse level control on IK_IN (Pin 58)) 00h = –10dB 1Fh = 0dB 3Fh = +6dB
G_CUTOFF	(6)	Gch cut-off control (Gch reference pulse level control on IK_IN (Pin 58)) 00h = –10dB 1Fh = 0dB 3Fh = +6dB
B_CUTOFF	(6)	Bch cut-off control (Bch reference pulse level control on IK_IN (Pin 58)) 00h = –10dB 1Fh = 0dB 3Fh = +6dB
SUB_CONT	(4)	Sub picture control 0h = –0.9dB 7h = 0dB Fh = +1.2dB
LRGB2_LEV	(4)	Picture level control for LRGB2 0h = –8dB Fh = 0dB
P_ABL	(4)	RGB output level detection DC setting for PEAK-ABL 0h = 4.8V DC Fh = 6.6V DC
ABL_TH	(4)	Threshold voltage adjustment for ABL_IN input 0h = Vth 0.8V Fh = Vth 1.9V
S_ABL	(2)	S_ABL gain setting 0 = S_ABL OFF 3 = S_ABL gain max.
WB_SW	(1)	White balance offset setting 0 = OFF Normal color temperature 1 = ON Low color temperature R: 100%, G: 90%, B: 70%
AKBOFF	(1)	Automatic cut-off/Manual cut-off setting 0 = Automatic cut-off (AKB ON) 1 = Manual cut-off (AKB OFF)
BLK_OFF	(1)	Blanking ON/OFF SW when AKBOFF = 1 0 = HV blanking ON 1 = HV blanking OFF (Blanking period: approximately 8 IRE)

4. Deflection Block Registers

AKBTIM	(5)	AKB Bch reference pulse timing setting (Counted from rising edge of VS_IN) 00h = 10H : 0Fh = 25H : 1Fh = 41H
UP_BLK	(4)	VBLK position control for top of picture, when VBLK_SW = 1 (Set number of lines blanked after Bch reference pulse.) (480i: every 1H / Others: every 2H) 0h = 0H : 7h = 7H/14H : Fh = 15H/30H
LO_BLK	(4)	VBLK position control for bottom of picture, when VBLK_SW = 1 (Set number of lines blanked before VSYNC.) (480i: every 1H / Others: every 2H) 0h = 0H : 7h = 7H/14H : Fh = 15H/30H
V_SIZE	(6)	Vertical amplitude adjustment (V_DRV signal gain adjustment) 00h = –15% Vertical picture size decreases 1Fh = 0% Amplitude: 1.2Vp-p, center DC = 3.5V (when V_ASPECT = 00h and ASP_SW = 0) 3Fh = +15% Vertical picture size increases
V_POSITION	(6)	Vertical position adjustment (V_DRV signal DC bias adjustment) 00h = –0.1V Picture position falls, V_DRV+ output DC down 1Fh = 0V Center DC = 3.5V 3Fh = +0.1V Picture position rises, V_DRV+ output DC up
V_LIN	(4)	Vertical linearity adjustment (Gain adjustment for V_DRV signal secondary component) 0h = 112% (Bottom/top of picture) Top of picture compressed; bottom of picture expanded 7h = 100% (Bottom/top of picture) Fh = 88% (Bottom/top of picture) Top of picture expanded; bottom of picture compressed

S_CORRECTION (4) Vertical S correction amount adjustment
(Gain adjustment for V_DRV signal S component)
0h = Tertiary component amplitude added to the V_DRV signal is 0.
Fh = Tertiary component amplitude added to the V_DRV signal is Maximum.

V_ON (1) V_DRV signal oscillation stop ON/OFF switch
0 = V_DRV Oscillation stopped
1 = V_DRV Output

EW_DC (1) EW_DRV signal DC level down
0 = Normal
1 = –1.2V

H_SIZE (6) Horizontal amplitude adjustment (EW_DRV signal DC bias adjustment)
00h = –0.5V Horizontal picture size decreases, EW_DRV signal output DC down
1Fh = 0V EW_DRV signal center DC: 4V
3Fh = +0.5V Horizontal picture size increases, EW_DRV signal output DC up

PIN_AMP (6) Horizontal pin distortion compensation amount adjustment
(EW_DRV signal gain adjustment)
00h = 190mVp-p Compensation amount min.
1Fh = 470mVp-p When V_ASPECT = 00h
3Fh = 750mVp-p Compensation amount max.

PIN_COMP (3) High voltage fluctuation compensation amount setting for horizontal pin distortion
(EW_DRV signal amplitude compensation)
0h = OFF
7h = –10% EW_DRV signal amplitude compensation amount when HCOMP_IN = 0V

UP_CPIN (6) Horizontal pin distortion compensation amount adjustment for top edge of picture
(EW_DRV signal gain adjustment for top edge of picture)
00h = –0.33V Horizontal size for top of picture decreases
(Compensation amount max.)
1Fh = 0V
3Fh = +0.33V Horizontal size for top of picture increases
(Compensation amount min.)

LO_CPIN (6) Horizontal pin distortion compensation amount adjustment for bottom edge of picture
(EW_DRV signal gain adjustment for bottom edge of picture)
00h = –0.25V Horizontal size for bottom of picture decreases
(Compensation amount max.)
1Fh = 0V
3Fh = +0.25V Horizontal size for bottom of picture increases
(Compensation amount min.)

UP_UCP (2) Horizontal pin distortion compensation position adjustment for extreme top edge of picture (EW_DRV signal compensation position for extreme top edge of picture)
- 0 = –20% Point of inflection (Position from video center, when vertical period: 100%)
- 3 = –33%

LO_UCP (2) Horizontal pin distortion compensation position adjustment for extreme bottom edge of picture (EW_DRV signal compensation position adjustment for extreme bottom edge of picture)
- 0 = +20% Point of inflection (Position from video center, when vertical period: 100%)
- 3 = +33%

UP_UCG (2) Horizontal pin distortion compensation amount adjustment for extreme top edge of picture (EW_DRV signal gain adjustment for extreme top edge of picture)
- 0 = 0V Compensation amount 0
- 3 = ±0.26V Compensation amount max. (When UP_UCP = 0, UC_POL = 0/1, V_ASPECT = 2F)

LO_UCG (2) Horizontal pin distortion compensation amount adjustment for extreme bottom edge of picture (EW_DRV signal gain adjustment for extreme bottom edge of picture)
- 0 = 0V Compensation amount 0
- 3 = ±0.26V Compensation amount max. (When LO_UCP = 0, UC_POL = 0/1, V_ASPECT = 2F)

UC_POL (1) Horizontal pin distortion compensation polarity setting for extreme top and bottom edge of picture
- 0 = Horizontal size for top and bottom edge of picture decreases
- 1 = Horizontal size for top and bottom edge of picture increases

PIN_PHASE (6) Horizontal trapezoidal distortion compensation adjustment (EW_DRV signal center timing adjustment)
- 00h = 1.1ms advance Horizontal size for top of picture increases; Horizontal size for bottom of picture decreases
- 1Fh = Compensation OFF EW_DRV center adjusted time when V_ASPECT = 00h and VFREQ is 60Hz
- 3Fh = 1.1ms delay Horizontal size for top of picture decreases; Horizontal size for bottom of picture increases

H_POSITION (6) Horizontal position adjustment (AFC phase control) (See Fig. 13 on page 58, 100%: H period)
- 00h = –0.5% Picture position compensated to right (Video delayed with respect to HD.)
- 1Fh = +2.5%
- 3Fh = +5.5% Picture position compensated to left (Video advanced with respect to HD.)

SYNC_PHASE (1) HSYNC delay amount setting with respect to video (100%: H period)
- 0 = 0%
- 1 = –3.125%

AFC_BOW (6) Vertical line slope compensation amount adjustment
(HAFC phase control by parabola wave, 100%: H period)
00h = Top and bottom of picture advanced 1.5% with respect to picture center
1Fh = No compensation
3Fh = Top and bottom of picture delayed 1.5% with respect to picture center

AFC_ANGLE (6) Vertical line slope compensation amount adjustment
(HAFC phase control by sawtooth wave, 100%: H period)
00h = Top of picture advanced 1.5%, bottom of picture delayed 1.5% with respect to picture center
1Fh = No compensation
3Fh = Top of picture delayed 1.5%, bottom of picture advanced 1.5% with respect to picture center

AFC_MODE (2) AFC loop gain control
0 = H free-running mode
1 = Small gain
2 = Medium gain
3 = Large gain

AFC_COMP (3) High voltage fluctuation compensation amount setting for horizontal position
(HCOMP_IN = 0V, 100%: H period)
0h = 0% No compensation
7h = +0.75% Picture position compensated to left

LEFT_BLK (6) HBLK width control for left side of picture when HBLK_SW = 1
(See Fig. 13 on page 58, 100%: H period)
00h = +17.8% HBLK width max.
1Fh = +12.8% Center
3Fh = +7.8% HBLK width min.

RIGHT_BLK (6) HBLK width control for right side of picture when HBLK_SW = 1
(See Fig. 13 on page 58, 100%: H period)
00h = –2.7% HBLK width min.
1Fh = –7.7% Center
3Fh = –12.7% HBLK width max.

HBLK_SW (1) HBLK width control ON/OFF switch during 4:3 software full display mode on a 16:9 CRT
0 = HBLK generated from HP_IN
1 = HBLK is made by processing the pulse generated from HP_IN and the pulse set by LEFT_BLK and RIGHT_BLK with OR logic.

CLP_PHASE (2) Internal clamp pulse phase control (See Fig. 13 on page 58, 100%: H period)
0 = +5%
3 = +2%

CLP_SHIFT (1) Internal clamp pulse start phase setting (100%: H period)
0 = CLP_PHASE settings
1 = CLP_PHASE settings – 3.125%

CLP_GATE (1) Switch for gating internal clamp pulse with input HSYNC
0 = No gated with input HSYNC
1 = Gated with input HSYNC

VFREQ (2) Vertical frequency setting
0 = 50Hz
1 = 60Hz
2 = 100Hz
3 = 120Hz

V_ASPECT (6) Aspect ratio control
00h = 75% 16:9 CRT Full
2Fh = 100% 4:3 CRT Full
3Fh = 106%

ASP_SW (1) Switch to correspond to the signal with low effective video ratio
0 = OFF
1 = ON V_DRV signal amplitude is 10% up when V_ASPECT = 0, and BLK for top and bottom for picture are 22 lines added.

ZOOM_SW (1) Zoom mode ON/OFF switch for 16:9 CRT
(V_DRV signal top and bottom squeeze mode ON/OFF)
0 = Zoom OFF
1 = Zoom ON

JMP_SW (1) Reference pulse jump mode ON/OFF switch
0 = Jump mode OFF
1 = Jump mode ON
On a 16:9 CRT, jump mode compresses the V_DRV signal amplitude to 67%
On a 4:3 CRT, jump mode compresses the V_DRV signal amplitude to 75%

V_SCROLL (6) Vertical picture scroll control
00h = –0.16V Scroll toward bottom of picture
1Fh = 0V
3Fh = +0.16V Scroll toward top of picture

UP_VLIN (4) Vertical linearity control for top of picture
0h = 100% (Bottom/top of picture)
Fh = 125% (Bottom/top of picture) Top of picture compressed

LO_VLIN (4) Vertical linearity control for bottom of picture
0h = 100% (Bottom/top of picture)
Fh = 73% (Bottom/top of picture) Bottom of picture compressed

V_COMP	(4)	High voltage fluctuation compensation amount setting for vertical picture size 0h = 0% Fh = –12% V_DRV signal amplitude compensation amount when VCOMP_IN = 0V
H_COMP	(4)	High voltage fluctuation compensation amount setting for horizontal picture size (EW_DRV signal DC bias compensation) 0h = 0V Fh = –0.3V EW_DRV signal DC compensation amount when HCOMP_IN = 0V
VSAW0_DCH	(2)	VSAW0 waveform DC component control high 2 bit
VSAW0_DCL	(4)	VSAW0 waveform DC component control low 4 bit 0h and VSAW0_DCH = 0 = –1.1V VSAW0 signal output DC down Fh and VSAW0_DCH = 1 = 0V VSAW0 signal center DC4V Fh and VSAW0_DCH = 3 = +1.1V VSAW0 signal output DC up
VSAW1_DC	(4)	VSAW1 waveform DC component 0h = –1.1V VSAW1 signal output DC down 7h = 0V VSAW1 signal center DC4V Fh = +1.1V VSAW1 signal output DC up
VSAW0_AMP	(5)	VSAW0 waveform SAW component amplitude 00h = 0.9Vp-p Right falling SAW component amplitude 0Fh = 0Vp-p No VSAW0 signal SAW component 1Fh = 0.9Vp-p Right rising SAW component amplitude
VSAW1_AMP	(5)	VSAW1 waveform SAW component amplitude 00h = 0.9Vp-p Right falling SAW component amplitude 0Fh = 0Vp-p No VSAW1 signal SAW component 1Fh = 0.9Vp-p Right rising SAW component amplitude
MP_PARA_DC	(4)	V parabola for middle pin DC bias control 0h = –1V MP_PARA signal output DC down 7h = 0V MP_PARA signal center DC 2.5V Fh = +1V MP_PARA signal output DC up
MP_PARA_AMP	(4)	V parabola for middle pin gain control 0h = 0Vp-p No parabola wave component Fh = 0.55Vp-p Downward convex parabola wave amplitude
HC_PARA_DC	(6)	V parabola for raster center DC bias control 00h = –1V HC_PARA signal output DC down 1Fh = 0V HC_PARA signal center DC 3.5V 3Fh = +1V HC_PARA signal output DC up

HC_PARA_PHASE (6) V parabola for raster center SAW component amplitude control
- 00h = 0.7Vp-p Right rising SAW component amplitude
- 1Fh = 0Vp-p No HC_PARA signal SAW component
- 3Fh = 0.7Vp-p Right falling SAW component amplitude

HC_PARA_AMP (6) V parabola for raster center amplitude control
- 00h = 0.35Vp-p Downward convex parabola wave amplitude
- 1Fh = 0Vp-p No parabola wave component
- 3Fh = 0.35Vp-p Upward convex parabola wave amplitude

VDRV_SW (1) V_DRV+, – signal jump voltage ON/OFF switch
- 0 = VDRV jump OFF
- 1 = VDRV jump ON
  Amplitude from the retrace timing to Bch reference pulse just behind increases 5%

VBLK_SW (1) VBLK width control ON/OFF switch
- 0 = VBLK is set as internal VDRV limited timing when ZOOM_SW = 1
- 1 = VBLK is set by UP_BLK and LO_BLK

RST_SW (1) VDRV retrace start setting switch
- 0 = 0.75H Retrace start after input VSYNC
- 1 = 6.25H Retrace start before input VSYNC

5. Status Registers

INTER (1) Input signal interlace/progressive identification
- 0 = Input signal: Progressive
- 1 = Input signal: Interlace

HCENT (1) High-low comparison between the input HSYNC frequency and the HVCO frequency (Valid when HVCO is locked.)
- 0 = HVCO free-running frequency is lower than input HSYNC frequency.
- 1 = HVCO free-running frequency is higher than input HSYNC frequency.

HLOCK (1) Lock status between HSYNC and HVCO
- 0 = IC free-running status
- 1 = Locked to HSYNC

IKR (1) AKB operation status
- 0 = Unstable AKB loop
- 1 = Stable AKB loop

HNG (1) Signal input status to HPROT pin
- 0 = Normal status
- 1 = Abnormal signal input to HPROT pin

VNG (1) Signal input status to VPROT pin (See Fig. 14 on page 59.)
- 0 = Normal status
- 1 = Abnormal signal input to VPROT pin

Description of Operation

1. Power-on Sequence

The CXA2150AQ does not have an internal power-on sequence. Therefore, the entire power-on sequence is controlled by the set microcomputer (I^2C bus controller).

1) Power-on reset

The IC is reset during power-on and the RGB output are all blanked.
Horizontal deflection output H_DRV starts to oscillate, but is free-running so that oscillation is not synchronized even if an unstable signal is input to HS_IN during power-on.
In vertical deflection system, VTIM starts to output, but V_DRV is DC output.
Bus registers which are set by the power-on reset are as follows.

PIC_ON	= 0:	RGB all blanking ON
R_ON	= 0:	Rch video blanking ON
G_ON	= 0:	Gch video blanking ON
B_ON	= 0:	Bch video blanking ON
GAMMA_L	= 0:	GAMMA fine adjustment OFF
CD_OFF	= 0:	SHP_CD function ON
BLK_OFF	= 0:	In AKB OFF-mode, blanking function is ON.
AKBOFF	= 0:	AKB function ON (Auto-cut-off mode)
V_ON	= 0:	V_DRV oscillation stopped mode
EW_DC	= 1:	EW_DRV signal DC level down
VBLK_SW	= 0:	In ZOOM, the blanking slicing internal VSAW is used.
SYNC_PHASE	= 0:	The delay amount compensation between video and HSYNC is 0.
CLP_SHIFT	= 0:	CLP_PHASE settings
AFC_MODE	= 0:	H_DRV oscillation free-running mode
RST_SW	= 0:	V_DRV signal starts to retrace after VSYNC
VFREQ	= 1:	60Hz mode
VSAW0_DCH	= 1:	VSAW0 DC level center
VSAW0_DCL	= Fh:	
VSAW1_DC	= 7h:	VSAW1 DC level center
VSAW0_AMP	= Fh:	No VSAW0 signal SAW component
VSAW1_AMP	= Fh:	No VSAW1 signal SAW component

2) Bus register data transfer

The register setting sequence differs according to the TV-set sequence. Register settings for the following sequence are shown as an example.

Set sequence	CXA2150AQ register settings
Power-on	Reset status in 1) above.
↓	↓
Degauss	Reset status in 1) above. The CRT is degaussed in the completely darkened condition.
↓	↓
V_DRV oscillation	The IC is set to the power-on initial settings. A sawtooth wave is output to V_DRV and the IC waits for the vertical deflection to stabilize.
↓	↓
AKB operation start	"R, G, B_ON" are set to 0, "PIC_ON" is set to 1 and reference pulse is output from R, G, B_OUT. Then, the IC waits for the cathode to warm up and the beam current to start flowing.
↓	↓
AKB loop stable	Status register "IKR" is monitored. IKR = 0: Unstable IKR = 1: Stable Note that the time until "IKR" returns to 1 differs according to the initial status of the cathode.
↓	↓
Video output	R, G, B_ON are set to 1 and the video signal is output from R, G, B_OUT.

3) Power-on initial settings

The initial settings listed here for power-on when V_DRV starts to oscillate are reference value; the actual settings may be determined as needed according to the conditions under which the set is to be used.

PIC_ON	=	0	RGB all blanked
R_ON	=	0	Rch video output blanked
G_ON	=	0	Gch video output blanked
B_ON	=	0	Bch video output blanked
DCOL	=	0	Dynamic Color OFF
WB_SW	=	0	OFF
GAMMA_L	=	0	GAMMA fine adjustment OFF
PICTURE	=	0	Max. (User control)
BLK_BTM	=	0	Min.
HUE	=	1Fh	Center (User control)
COL_AXIS	=	3	NTSC Japan
COLOR	=	1Fh	Center (User control)

CTI_LEV	=	0	CTI OFF
BRIGHT	=	1Fh	Center (User control)
S_ABL	=	0	SABL OFF
SHARPNESS	=	1Fh	Center (User control)
LTI_LEV	=	0	LTI OFF
R_DRIVE	=	29h	0dB (Adjust)
PLIMIT_LEV	=	3	Max.
G_DRIVE	=	29h	0dB (Adjust)
ABL_MODE	=	1	Picture/Bright ABL mode (Bright ABL Gain min.)
B_DRIVE	=	29h	0dB (Adjust)
CTI_MODE	=	0	B/W both sides improvement
SUB_BRIGHT	=	1Fh	Center (Adjust)
GAMMA	=	0	GAMMA OFF
R_CUTOFF	=	1Fh	Center (Adjust)
LTI_MODE	=	0	B/W both sides improvement
G_CUTOFF	=	1Fh	Center (Adjust)
DPIC_LEV	=	0	Black expansion OFF
B_CUTOFF	=	1Fh	Center (Adjust)
DC_TRAN	=	0	DC transmission ratio 100%
SUB_CONT	=	7h	Center (Adjust)
LRGB2_LEV	=	Fh	0dB
P_ABL	=	Fh	Max.
ABL_TH	=	0	Min.
CB_OFFSET	=	1Fh	Center (Adjust)
AGING_W	=	0	OFF
AGING_B	=	0	OFF
CR_OFFSET	=	1Fh	Center (Adjust)
SYSTEM	=	2	HD mode
Y_OFFSET	=	7h	Center (Adjust)
VM_LEV	=	3	Max.
SHP_F0	=	0	12MHz
CD_OFF	=	0	SHP_CD function ON
SHP_CD	=	0	OFF
SHP_F1	=	0	OFF
PRE/OVER	=	0	1:1
VM_COR	=	0	OFF
VM_F0	=	0	Min.
VM_LMT	=	3	Max, limit
VM_DLY	=	0	VM_OUT delay Max.
AKB_TIM	=	0h	Bch REF-P 10H
BLK_OFF	=	0	Blanking ON
AKBOFF	=	0	AKB mode
UP_BLK	=	0h	VBLK-end 0H after Bch REF-P
LO_BLK	=	0h	VBLK-start 0H before VSYNC
V_SIZE	=	1Fh	Center (Adjust)
V_ON	=	1	V_DRV output ON
EW_DC	=	0	OFF

V_POSITION	=	1Fh	Center (Adjust)
VSAW0_DCH	=	1	Center
V_LIN	=	7h	Center (Adjust)
S_CORRECTION	=	7h	Center (Adjust)
H_SIZE	=	1Fh	Center (Adjust)
UP_UCP	=	0	Most inside compensation point
PIN_AMP	=	1Fh	Center (Adjust)
LO_UCP	=	0	Most inside compensation point
UP_CPIN	=	1Fh	Center (Adjust)
UP_UCG	=	0	Min.
LO_CPIN	=	1Fh	Center (Adjust)
LO_UCG	=	0	Min.
PIN_PHASE	=	1Fh	Center (Adjust)
UC_POL	=	0	H-size small on compensation parts
VBLK_SW	=	1	UP/LO_BLK only
H_POSITION	=	1Fh	Center (Adjust)
SYNC_PHASE	=	0	HSYNC delay 0%
CLP_SHIFT	=	0	CLP_PHASE settings
AFC_BOW	=	1Fh	Center (Adjust)
AFC_MODE	=	2	Medium gain
AFC_ANGLE	=	1Fh	Center (Adjust)
RST_SW	=	0	Retrace after VSYNC
LEFT_BLK	=	1Fh	Center (Adjust)
CLP_PHASE	=	3	Min.
RIGHT_BLK	=	1Fh	Center (Adjust)
CLP_GATE	=	0	Gate function OFF
HBLK_SW	=	1	HBLK control enable
V_ASPECT	=	0h	16:9 CRT (Min.)
ZOOM_SW	=	0	ZOOM_SW OFF
JMP_SW	=	0	JUMP_SW OFF
V_SCROLL	=	1Fh	Center (User Control)
VFREQ	=	1	60Hz mode
UP_VLIN	=	0h	Compensation OFF
LO_VLIN	=	0h	Compensation OFF
V_COMP	=	0h	Compensation OFF
H_COMP	=	0h	Compensation OFF
VSAW0_DCL	=	Fh	Center
VSAW1_DC	=	7h	Center
VSAW0_AMP	=	Fh	Amplitude OFF
PIN_COMP	=	0	Compensation OFF
VSAW1_AMP	=	Fh	Amplitude OFF
AFC_COMP	=	0	Compensation OFF
MP_PARA_DC	=	7h	Center
MP_PARA_AMP	=	0h	Amplitude OFF
HC_PARA_DC	=	1Fh	Center
ASP_SW	=	0	OFF
VDRV_SW	=	0	OFF
HC_PARA_AMP	=	0	Amplitude OFF
HC_PARA_PHASE	=	0	Center

2. Various Mode Settings

The CXA2150AQ contains I2C bus registers for deflection compensation which can be set for various wide modes. Wide mode setting registers can be used separately from registers for normal picture distortion adjustment, and once picture distortion adjustment has been performed in full mode, wide mode settings can be made simply by changing the corresponding register data.

- Vertical picture distortion adjustment registers (V_DRV)
  V_SIZE, V_POSITION, S_CORRECTION, V_LIN
- Horizontal picture distortion adjustment registers (EW_DRV)
  H_SIZE, EW_DC, PIN_AMP, UP_CPIN, LO_CPIN, PIN_PHASE
- Wide mode setting registers
  V_ASPECT, ZOOM_SW, HBLK_SW, V_SCROLL, JUMP_SW, VBLK_SW, UP_VLIN, LO_VLIN, LEFT/RIGHT_BLK, UP/LO_BLK

Examples of various modes are listed below. These modes are described using 480 lines as essential number of display scanning lines. Wide mode setting register data is also listed, but adjustment values may differ slightly due to IC variation. The standard setting data differs for 16:9 CRTs and 4:3 CRTs.

Register	16:9 CRT	4:3 CRT
V_ASPECT	0h	2Fh
V_SCROLL	1Fh	1Fh
ZOOM_SW	1	0
UP_VLIN	0h	0h
LO_VLIN	0h	0h
JUM_SW	0	0
VBLK_SW	1	1
HBLK_SW	1	1
LEFT_BLK	1Fh	1Fh
RIGHT_BLK	1Fh	1Fh

1) 16:9 CRT full mode

This mode reproduces the full 480 lines on a 16:9 CRT. 4:3 images are reproduced by vertical compression. Normal images are compressed vertically, but 16:9 images can be reproduced in their original 16:9 aspect ratio with a video source which compress (squeezes) 16:9 images to 4:3 images.
The register settings are the 16:9 CRT standard values.

2) 16:9 CRT normal mode

In this mode, 4:3 images are reproduced without modification. A black border appears at the left and right of the picture. In this mode, the H deflection size must be compressed by 25% compared to full mode. The CXA2150AQ performs compression with a register "EW_DC" that compresses the H size. Because excessive current flows to the horizontal deflection coil in this case, adequate consideration must be given to allowable power dissipation, etc., of the horizontal deflection coil in the design of the set. In addition, this concern can also be addressed through measures taken external to the IC, such as switching the horizontal deflection coil. Full mode should be used when performing memory processing and attaching a black border to the video signal.

H blanking of the image normally uses the H-pulse input from HP_IN (Pin 39). However, the blanking width can be varied according to the control register setting when blanking is insufficient for the right and left black borders.

The following three settings are added to the 16:9 CRT standard values for the register settings.

HBLK_SW = 1
LEFT_BLK = Adjustment value
RIGHT_BLK = Adjustment value

The H angle of deflection also decreases, causing it to differ from the PIN compensation amount during H size full status. Therefore, in addition to the wide mode registers, "PIN_AMP" must also be readjusted only for this mode.

3) 16:9 CRT zoom mode

In this mode, 4:3 images are reproduced by enlarging the picture without other modification. The top and bottom of normal 4:3 images are lost, but almost the entire picture can be reproduced for vista size video software, etc. which already has back borders at the top and bottom. The enlargement ratio can be controlled by the "V_ASPECT" register, and enlarging the picture by 33% compared to full mode allows zooming to be performed for 4:3 images without distortion. In this case, the number of scanning lines is reduced to 360 Iines compared to 480 Iines for full mode. The zooming position can be shifted vertically by the "V_SCROLL" register. V blanking of the image is performed by setting VBLK_SW = 0, and the top and bottom parts which are lost are also blanked during this mode.

Adjust the following two registers with respect to the 16:9 CRT standard values for the register settings.

V_ASPECT = 2Fh
V_SCROLL = 1Fh or user control

4) 16:9 CRT subtitle-in mode

When Cinema Scope Size images which have black borders at the top and bottom of the picture are merely enlarged with the zoom mode in 3) above, subtitles present in the black borders may be lost. Therefore, this mode is used to super-compress only the subtitle part and reproduce it on the display.

Add the "LO_VLIN" adjustment to the zoom mode settings for the register settings.

V_ASPECT = 2Fh
V_SCROLL = 1Fh or user control
LO_VLIN = Adjustment value

5) 16:9 CRT two-picture mode

This mode is used to reproduce two 4:3 video displays on a 16:9 CRT such as for P and P.
The V size must be compressed to 67% in order to reproduce two displays on a 16:9 CRT without distortion using 480 scanning lines, and this can be set by "JMP_SW".
By setting JMP_SW = 1, the V size is compressed except the period from the retrace of V_DRV signal to putting the reference pulses on R, G, B signal, and the AKB reference pulses remain in the over-scan position.
The following timings can be adjusted with each register.

The reference pulses: "AKBTIM"
The end of the vertical blanking: "UP_BLK"
The start of the vertical blanking: "LO_BLK"

Adjust the following five registers with respect to the 16:9 CRT standard values for the register settings.

JMP_SW = 1
AKBTIM = Adjustment value
VBLK_SW = 1
UP_BLK = Adjustment value
LO_BLK = Adjustment value

6) 16:9 CRT wide zoom mode

This mode reproduces 4:3 video software on wide displays by enlarging 4:3 images without other modification and compressing the parts of the image which protrude from the picture into the top and bottom parts of the picture. The display enlargement ratio is controlled by V_ASPECT, and the compression ratios at the top and bottom of the picture are controlled by UP/LO_VLIN.
Adjust the following three registers with respect to the 16:9 CRT standard values for the register settings.

V_ASPECT = Adjustment value
UP_VLIN = Adjustment value
LO_VLIN = Adjustment value

7) 4:3 CRT normal mode

This is the standard mode for 4:3 CRTs.
The register settings are with respect to the 4:3 CRT standard values.

8) 4:3 CRT V compression mode

This mode is used to reproduce M-N converter output consisting of 16:9 images expanded to 4:3 aspect ratio and other squeezed signals without distortion on a 4:3 CRT. In this case, the V size must be compressed to 75%. This is done using JMP_SW in 5) above. Fine adjustment of the V size is possible by adding the V_ASPECT adjustment.
Adjust the following two registers with respect to the 4:3 CRT standard values for the register settings.

V_ASPECT = Adjustment value
JMP_SW = 1

9) 4:3 CRT V compression mode for 100Hz TV (Flicker Free)

The V deflection frequency for 100Hz TV sets is twice that 50Hz TV sets, so scanning may become rougher at the top of the picture when using the mode in 8) above.
In this case, V compression is performed with V_ASPECT not using JMP_SW, and if necessary, the timings adding the reference pulse and the blanking period can be adjusted with AKBTIM and UP/LO_BLK in the same way as 5) above.
Adjust the following five registers with respect to the 4:3 CRT standard values for the register settings.

V_ASPECT = Adjustment value
AKBTIM = Adjustment value
VBLK_SW = 1
UP_BLK = Adjustment value
LO_BLK = Adjustment value

Settings for Horizontal Deflection Frequency

As regards horizontal deflection frequency, this IC corresponds to the following four point-scan modes.

PS15K: Normal scan for NTSC/PAL/SECAM etc.
PS31K: Double scan for NTSC etc., and VGA
PS33K: HDTV 1080i and MUSE 1035i
PS37K: SVGA
PS45K: HDTV 720p

See Table 1 for settings.

1) Settings for Pin 23 F0 and Pin 24 F1

L: Connect to GND
M: Open the pin
H: Connect to Pin 29 VREG5

2) Horizontal deflection (H_DRV) free-running frequency f0

PS15K: Point Scan 15.74kHz
PS31K: Point Scan 31.5kHz
PS33K: Point Scan 33.83kHz
PS37K: Point Scan 37.9kHz
PS45K: Point Scan 45kHz

F1	F0	H_DRV f0	Storage
L	L	PS15K	Normal
L	M	PS31K	Normal
L	H	PS31K	Long
M	L	PS33K	Normal
M	M	PS45K	Normal
M	H	*	*
H	L	PS33K	Long
H	M	PS37K	Normal
H	H	PS45K	Long

*: Prohibited settings

Table 1. Settings for Pin F0 and Pin F1

While switched by Pins F0 and F1, this IC changes horizontal deflection frequency of H_DRV output signal while H_DRV is high level, but doesn't have any other special sequences. Therefore it is recommended that a microcomputer be used in the TV set side for sequence control in the case of dynamic switching.

3) Supported HOUT storage times

The H_DRV signal output from Pin 40 is input to the horizontal deflection circuit of TV set to generate an H-pulse.
This IC provides Normal mode and Long mode to support storage times from the rising edge of HD signal to the rising edge of H-pulse input to Pin 39 HP_IN.
See Table 1 for settings Pins F0 and F1.

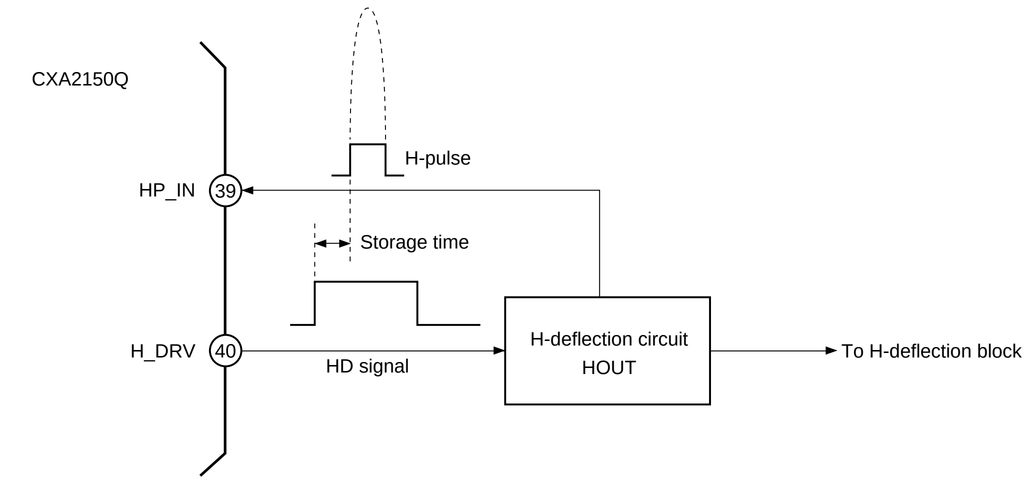


Fig. 1. Storage Time from HD to H-pulse

The storage time differs slightly depending on the drive conditions of a TV set, etc.
Fig. 2 shows examples of the range of the storage time covered for each mode.
Conditions: "H_POSITION" and "AFC_BOW, ANGLE" etc. are center value, and the input H-pulse width is 4.5µs.

Assuming that an H-pulse width on a TV set is Tw [µs], a converted value on Fig. 2, ΔST [µs] is;

$\Delta ST = (4.5 - Tw) / 2$,

$\Delta ST < 0$ (negative) : Shift to left, $\Delta ST > 0$ (positive) : Shift to right.

In additions, the variable range for "H_POSITION" and "AFC_BOW, ANGLE" etc. are in Fig. 2.

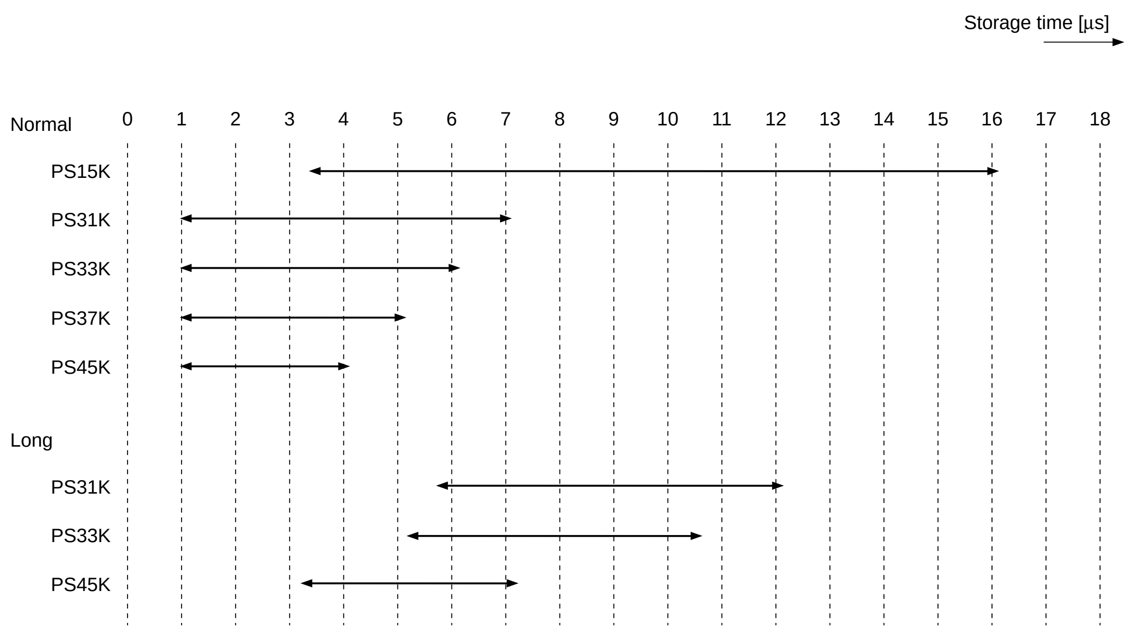


Fig. 2. Reference Example of Supported Storage Times for Each Mode (H-pulse Width: 4.5µs)

Settings for Vertical Deflection Frequency

The vertical deflection frequency is determined by combinations with settings made using pins F0 and F1 for horizontal deflection frequency and "VFREQ register" settings. See Table 2.
In additions, Table 2 shows the regular number of lines for each set vertical frequency.

Horizontal mode	"VFREQ" register			
	0: 50Hz	1: 60Hz	2: 100Hz	3: 120Hz
PS15K	312.5	262.5	×	×
PS31K	625	525	312.5	262.5
PS33K	675	562.5	×	×
PS45K	×	750	×	×

×: Prohibited settings

Table 2. Settings for Vertical Deflection Frequency (Regular Number of Lines) for Each Horizontal Mode

VSYNC signal input in the range from –50% to +12.5% of the regular number of lines is accepted. Therefore, when VSYNC is not input, the CXA2150AQ is free-running as the regular number of lines +12.5%.
However, when input VSYNC frequency changes, the vertical picture size also changes because V_DRV output amplitude is Auto-Gain-Controlled depending on the regular number of lines.
In addition, V_DRV output operates as interlaced or non interlaced mode depending on VSYNC input.

SVGA Mode

The CXA2150AQ can support the SVGA deflection frequencies (horizontal: 37.9kHz, vertical: 60Hz).
The setting method is as follows: (See Table 1 PS37K.)

Pin 23 (F0): Connected to Pin 29 (VREG5) (H)
Pin 24 (F1): Open (M)
"VFREQ" register: 1

The V_DRV output AGC operation in SVGA mode differs from other modes, so the "Settings for Vertical Deflection Frequency" above do not apply.
Therefore, the vertical deflection free-running frequency fv is approximately 35Hz.
In addition, VSYNC input up to fv (approximately 35Hz) is accepted, and even if the input VSYNC frequency changes within the AGC operating range, the vertical picture size does not change.

Vertical Timing Charts

Figs. 3 to 12 show the vertical timing charts.

Fig. 3: Relationship between "AKBTIM" and "UP/LO_BLK" variable ranges and various effective video line inputs

Figs. 4 to 12 show each mode at 1125i (1080i).

Fig. 4: Standard settings
(VBLK_SW = 1, ZOOM_SW = 0, JUMP_SW = 0, V_ASPECT = 00h, ASP_SW = 0, RST_SW = 0, VDRV_SW = 0)
Fig. 5: Zoom mode (VBLK_SW = 0, ZOOM_SW = 1, V_ASPECT = 2Fh)
Fig. 6: JUMP (V compression) mode (JUMP_SW = 1)
Fig. 7: Effective video ratio conversion mode (ASP_SW = 1)
Fig. 8: (VDRV_SW = 1)
Fig. 9: (RST_SW = 1)
Fig. 10: When a faster VSYNC than the regular cycle is input such as when switching channels
Fig. 11: When VSYNC input stops or when VSYNC is input suddenly
Fig. 12: When VSYNC input stops or when VSYNC is input suddenly (RST_SW = 1)

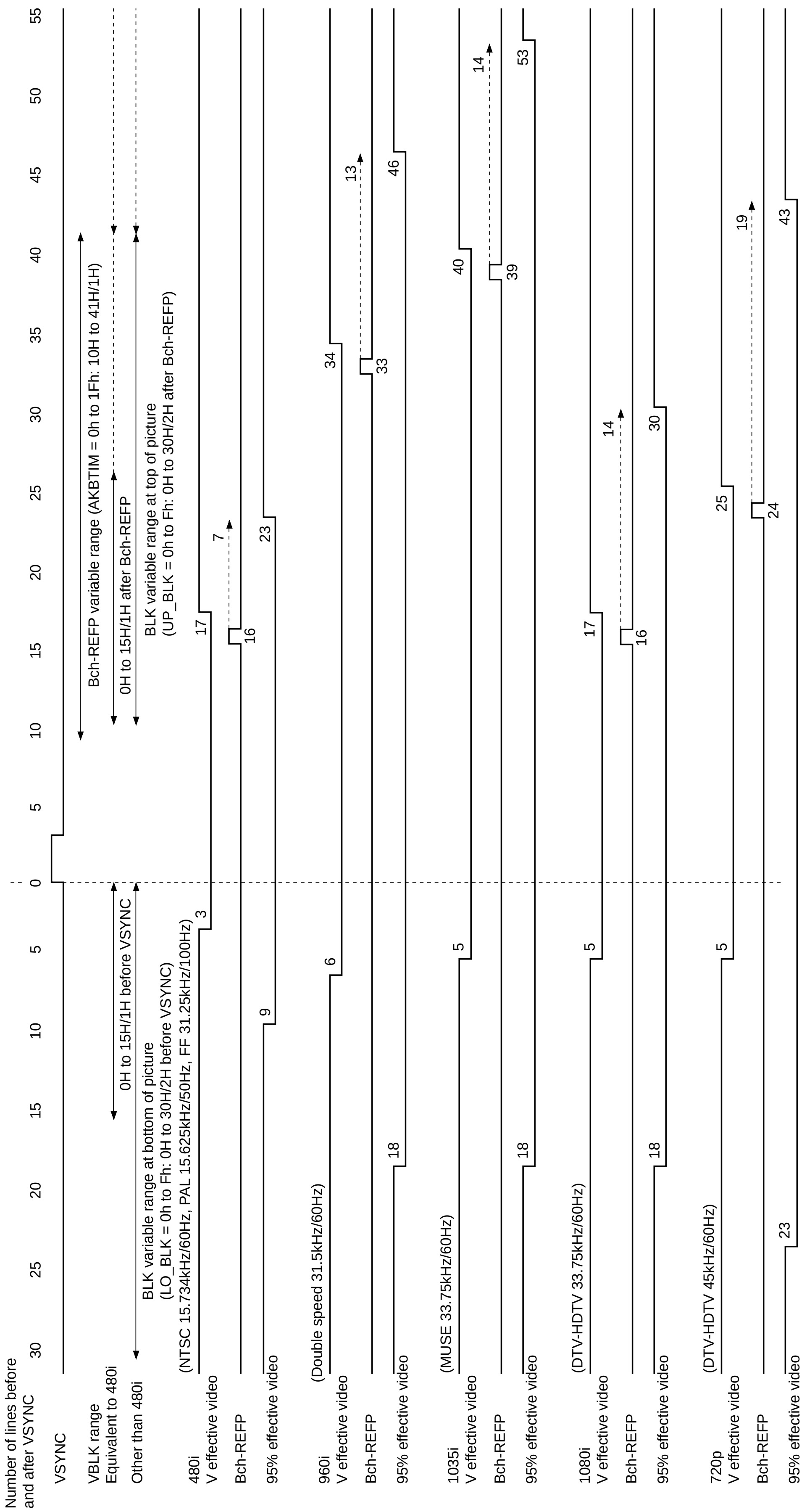


Fig. 3. Relationship between "AKBTIM" and "UP/LO_BLK" Variable Ranges and Various Effective Video Line Inputs

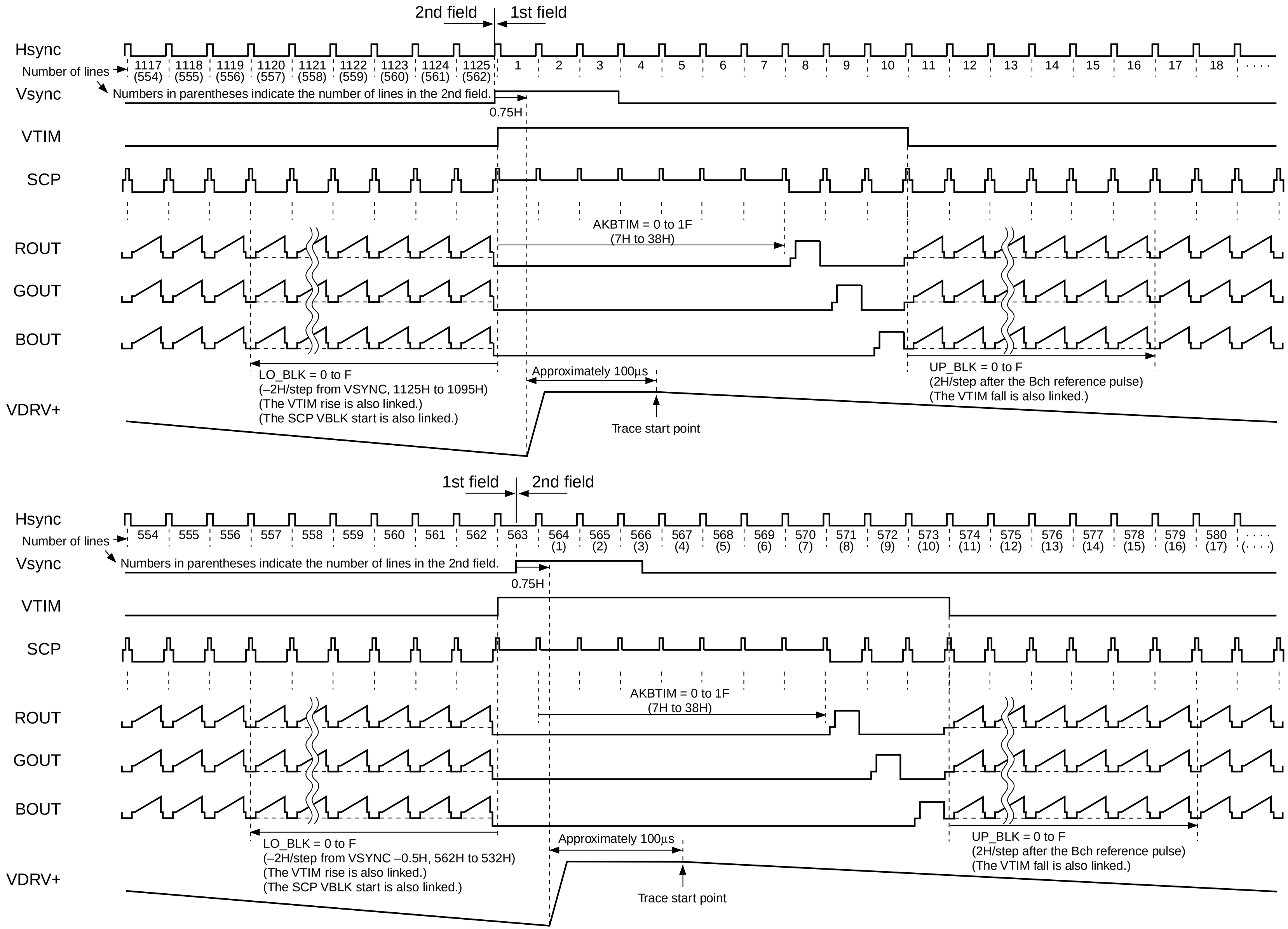


Fig. 4. V Timing Chart 1 – 1125i (1080i) Standard Settings

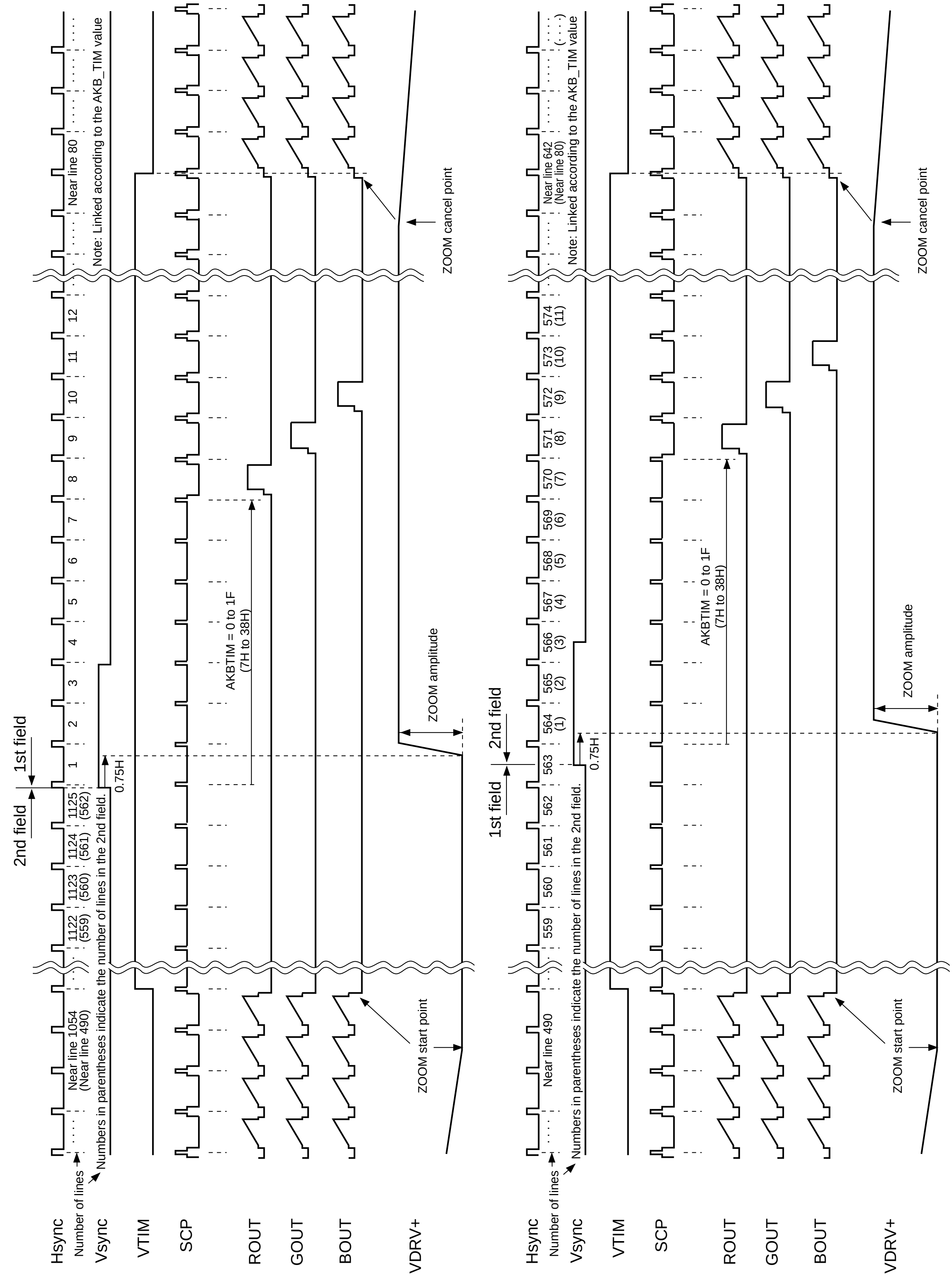


Fig. 5. V Timing Chart 2 – Zoom Mode (VBLK_SW = 0, ZOOM_SW = 1, V_ASPECT = 2Fh)

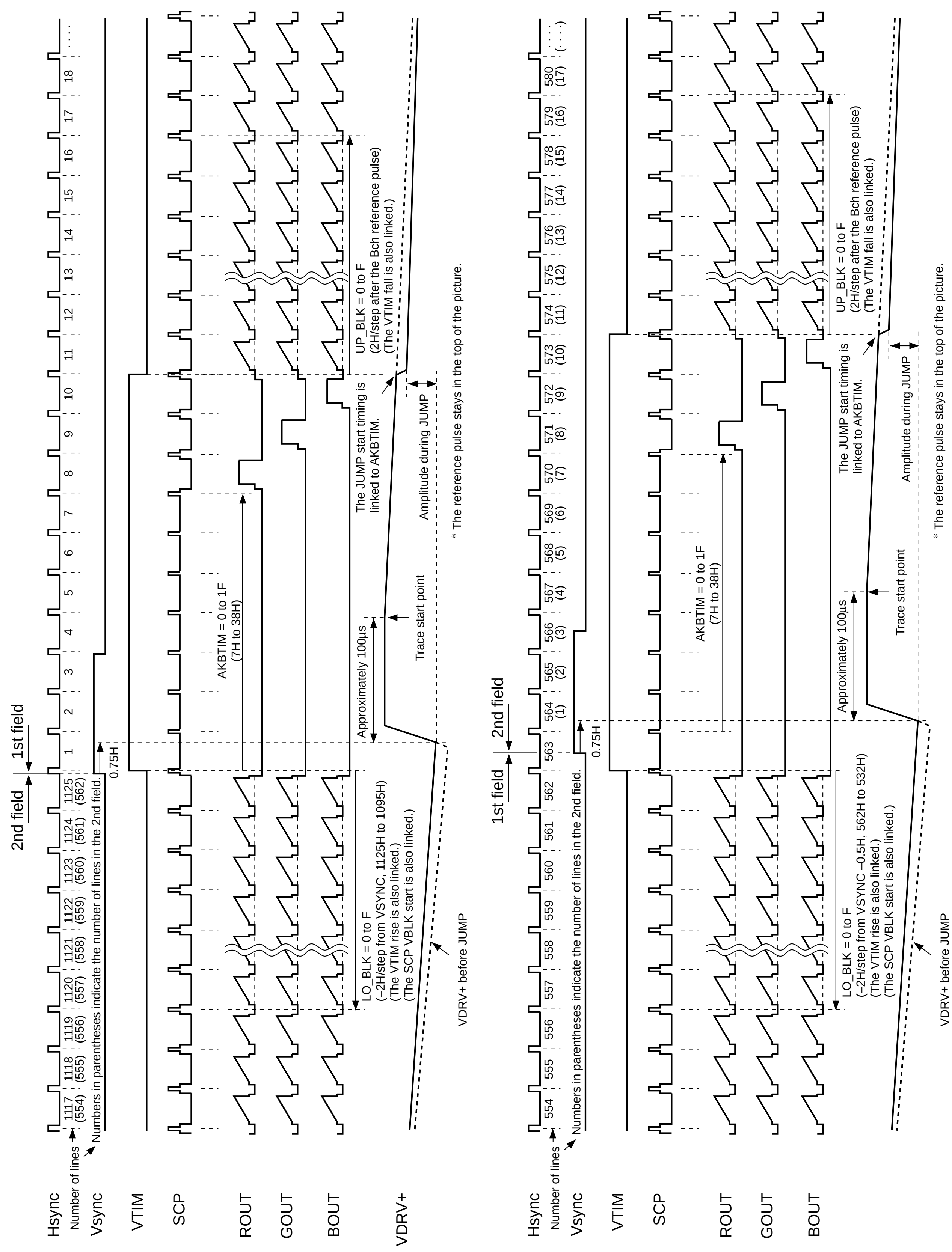


Fig. 6. V Timing Chart 3 – JUMP (V Compression) Mode (JUMP_SW = 1)

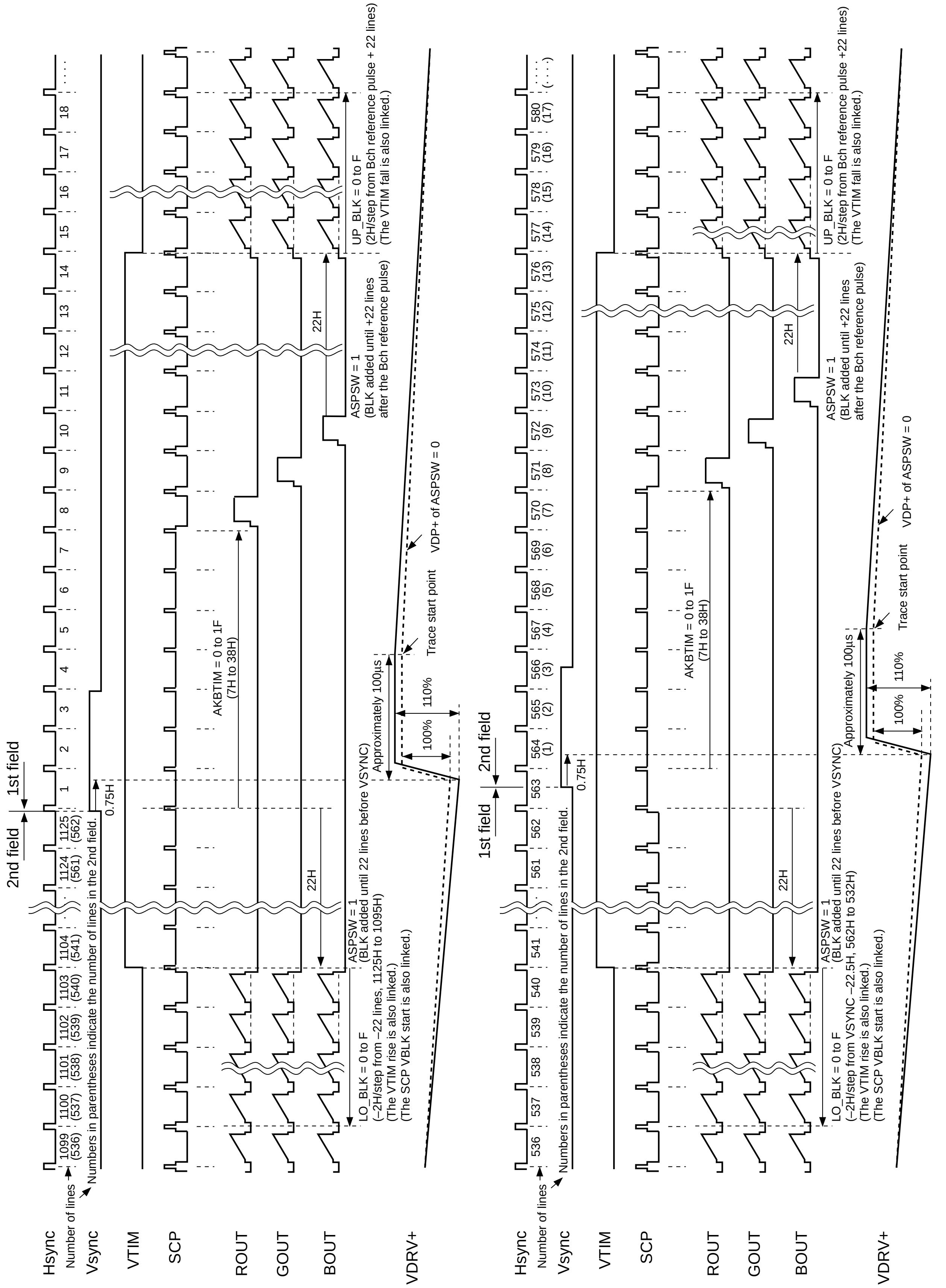


Fig. 7. V Timing Chart 4 – Effective Video Ratio Conversion Mode (ASP_SW = 1)

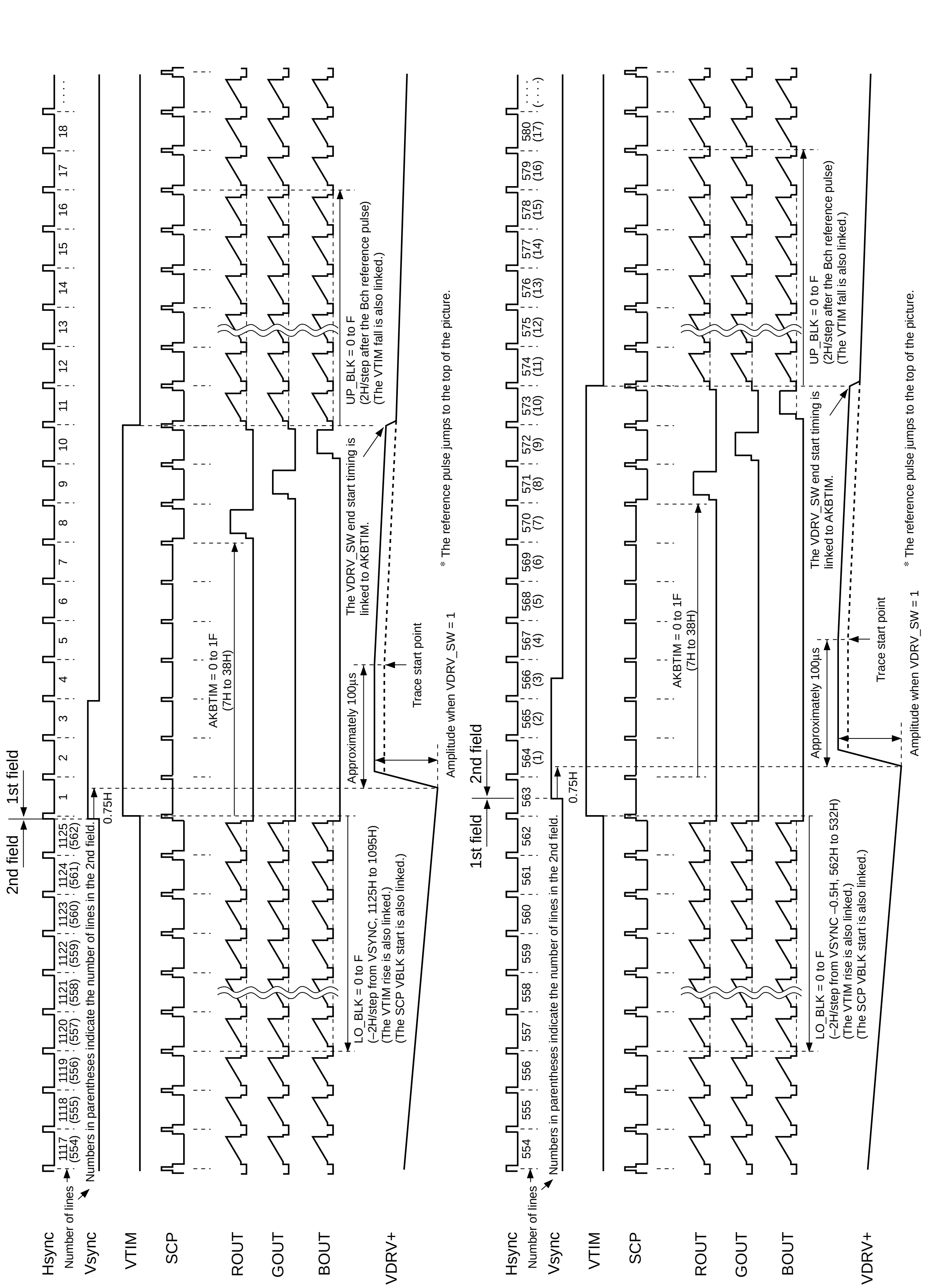


Fig. 8. V Timing Chart 5 – VDRV_SW = 1

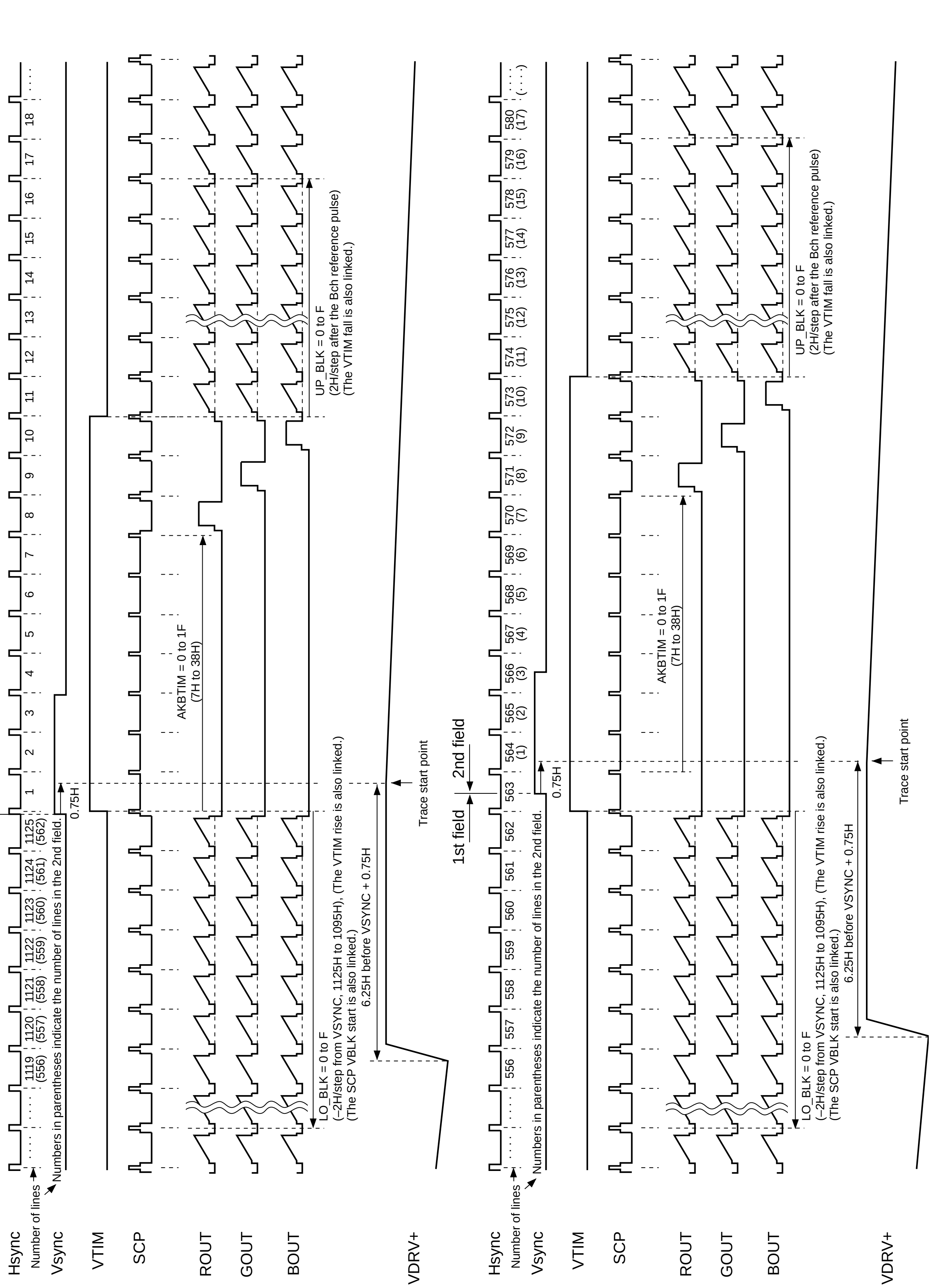
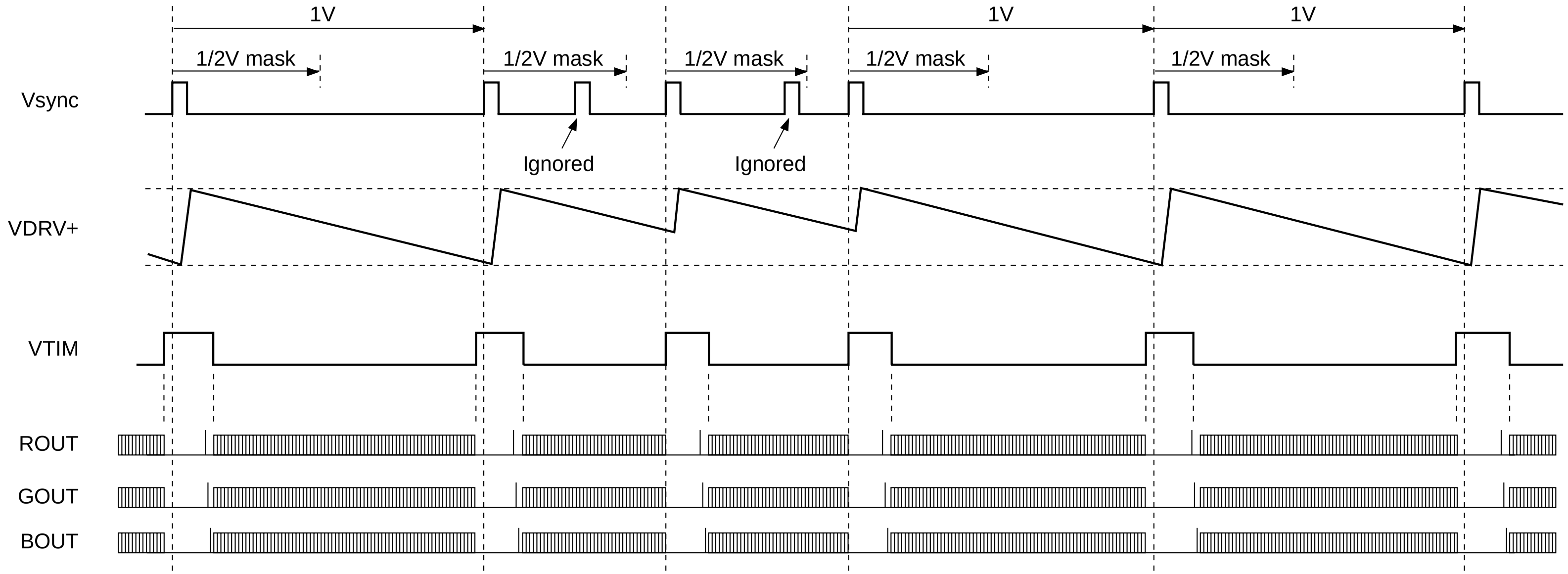
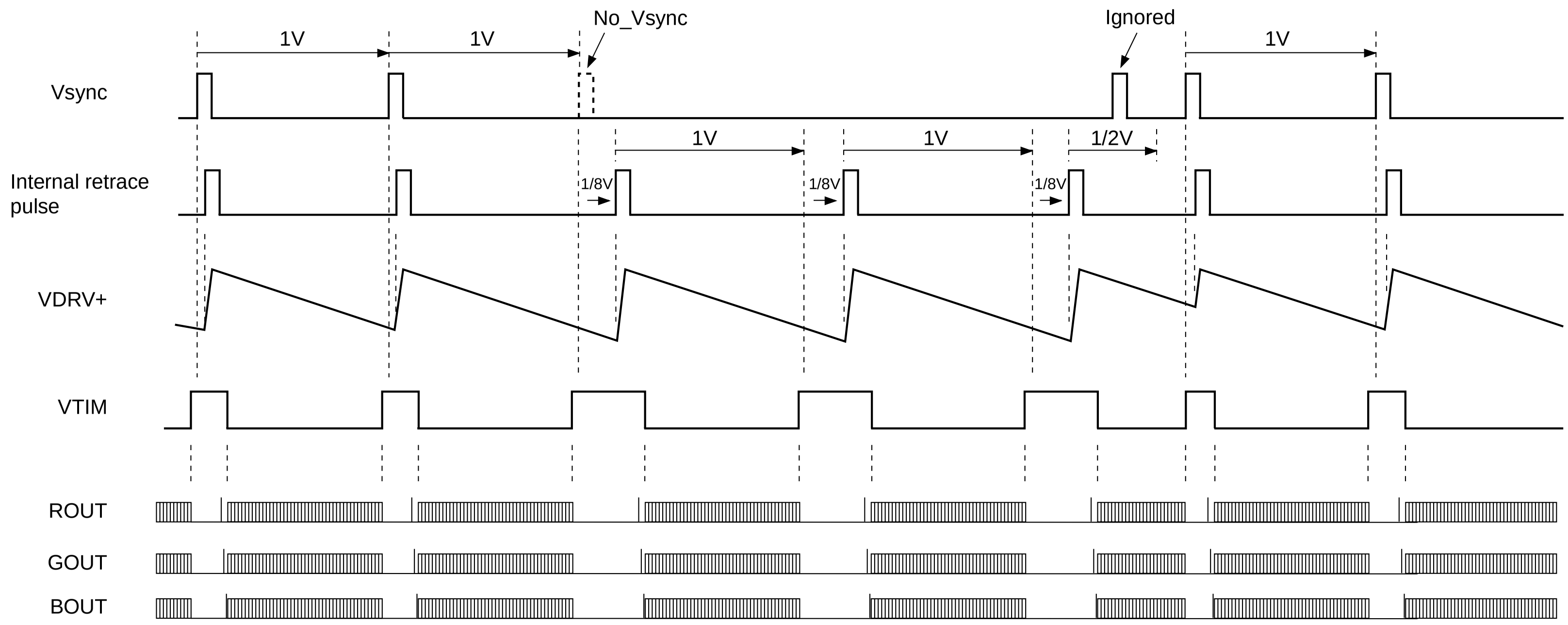


Fig. 9. V Timing Chart 6 – RST_SW = 1



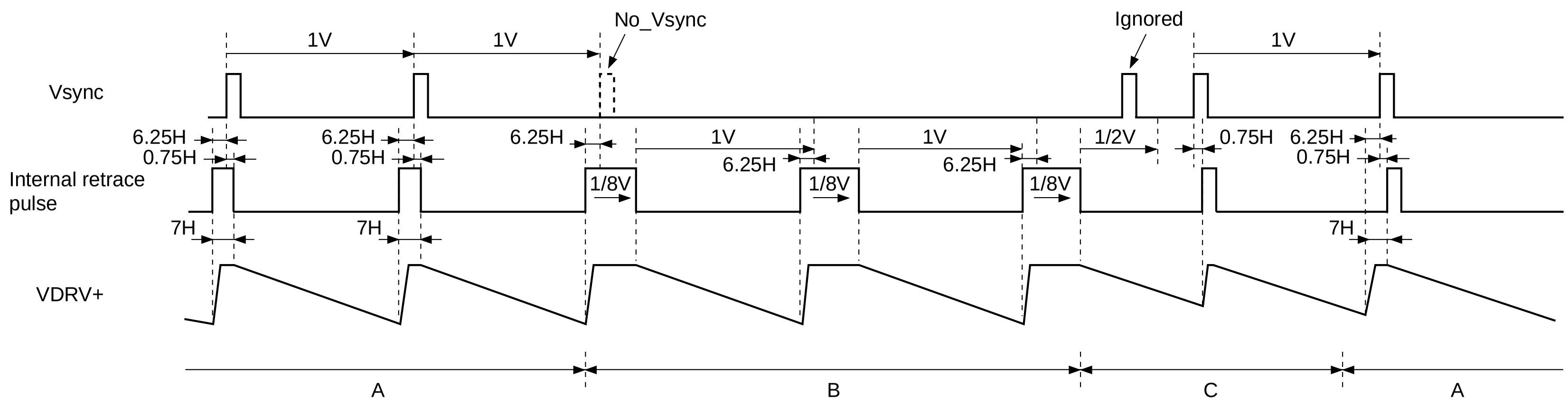
* VSYNC is not accepted within a 1/2V period from the start of the VDRV+ retrace. (1/2V mask)
* When a shorter V than the normal V frequency is input, the RGBOUT V blanking starts at approximately the same time as VSYNC, regardless of the LO_BLK data.

Fig. 10. V Timing Chart 7 – When a faster VSYNC than the regular cycle is input such as when switching channels



* When VSYNC input stops, free-running at a 1V + 1/8V cycle results.

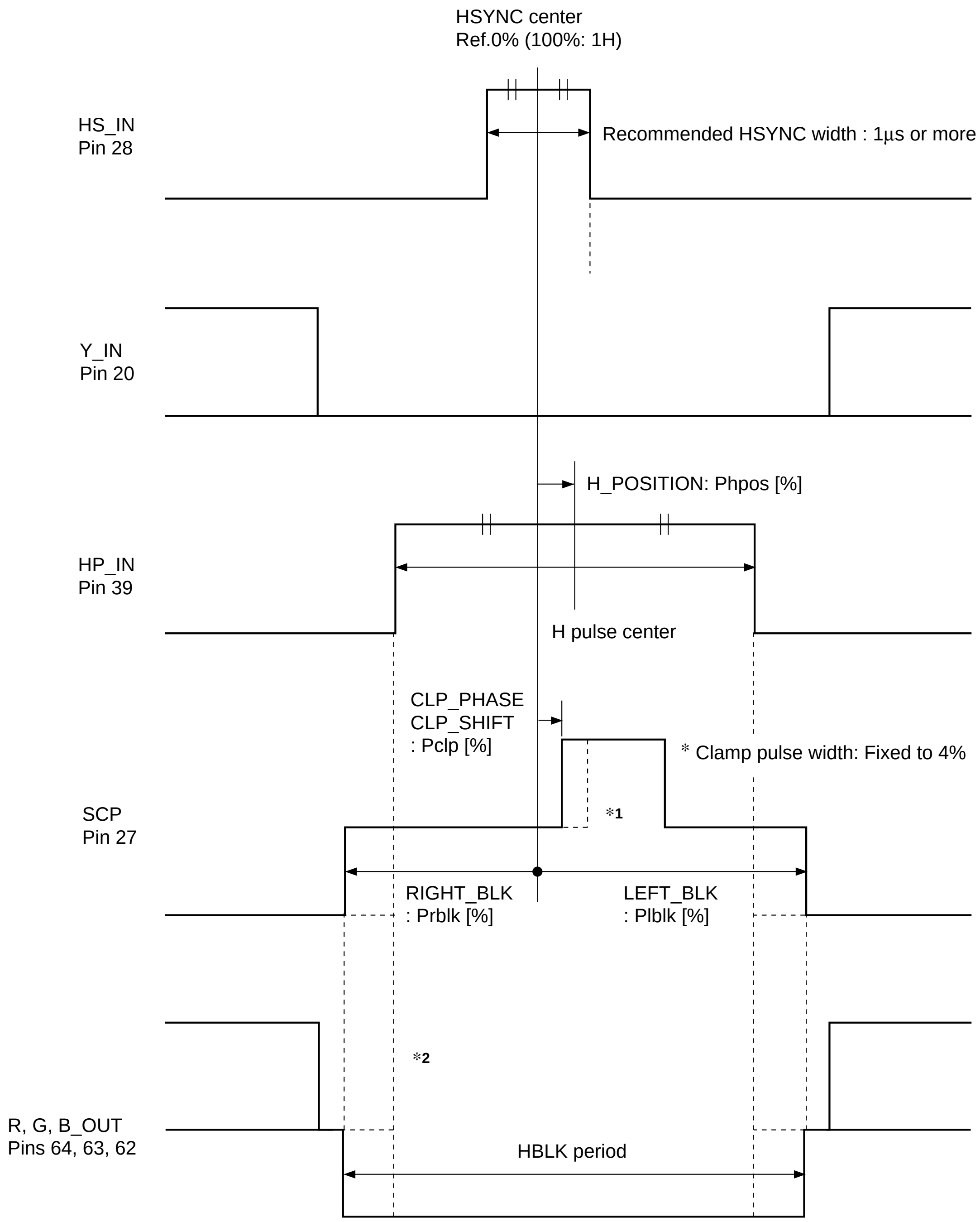
Fig. 11. V Timing Chart 8 – When VSYNC input stops or when VSYNC is input suddenly



A) When VSYNC is input: VDP+ retrace starts from 6.25H before VSYNC.
B) When VSYNC input stops: Free-running at a 1/8V + 1V cycle results.
C) When VSYNC is input suddenly: VDRV+ retrace starts with precedence on the VSYNC 1/2V or more after the trace start or the internal retrace pulse 6.25H before 1V is reached, whichever is input first.

Fig. 12. Timing Chart 9 – When VSYNC input stops or when VSYNC is input suddenly (RST_SW = 1)

Horizontal System Timing Chart



*1 When "CLP_GATE" =1, the Clamp pulse is masked in the period that input HSYNC is high level.
The internal clamp pulse is same, so set to a suitable clamped phase using "CLP_PHASE" and "CLP_SHIFT".

*2 When "HBLK_SW" =1, the HBLK period on R, G, B_OUT and SCP is made by processing the pulse set by "RIGHT, LEFT_BLK" and the period that H-pulse is high level with OR logic.
When "HBLK_SW" = 0, the HBLK is the period that H-pulse is high level.

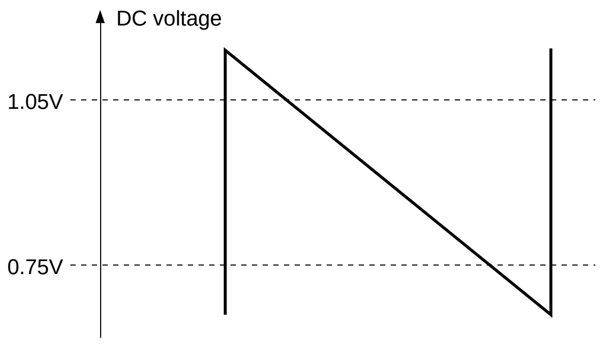
Fig. 13

V Protect

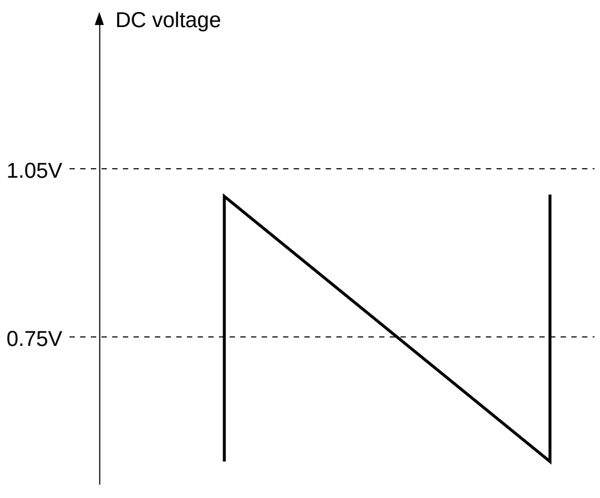
Pin 35 (VPROT) is used to completely blanks the R, G, B_OUT output during abnormal signal input by feeding back the vertical deflection drive signal using V_DRV output.
(Reference pulses are also blanked.)
The conditions for determining whether the VPROT input is "normal input" are as follows.

(1) The input signal should rise to 1.05V or more after VSYNC
(2) The bottom edge of the input signal should fall to 0.75V or less after (1) above

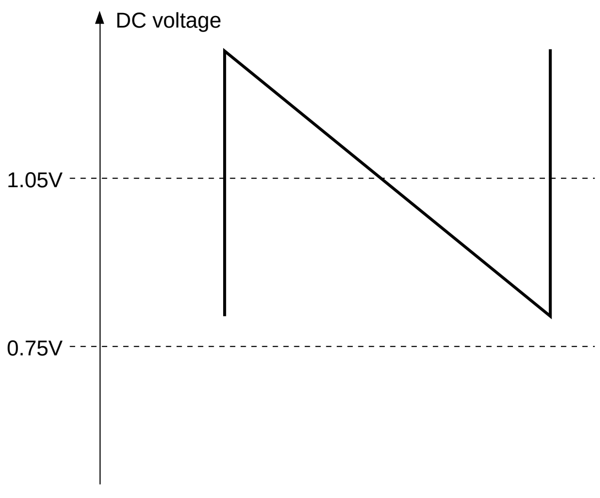
If a signal that do not satisfy both (1) and (2) above continues for more than 3 V cycles,
it is considered "abnormal input" and R, G, B_OUT are completely blanked.
If the input returns to "normal input", the blanking will be cancelled from the next V cycle.
In addition R, G, B_OUT are also completely blanked during power-on and when "V_ON" = 0 (V_DRV signal is just DC with no amplitude.).



Normal input to VPROT input pin



Abnormal input to VPROT input pin example 1
(The top edge of the input signal does not rise to 1.05V or more.)



Abnormal input to VPROT input pin example 2
(The bottom edge of the input signal does not fall to 0.75V or less.)

Fig. 14. Signal Input Status to VPROT

Frequency Response Related Settings

Table 3 shows the center frequency f0 setting value reference data for each control register related to frequency response.

Function	Corresponding register	"SHP_F0"	"VM_F0"	Center frequency f0 [MHz] by mode ("SYSTEM")			
				NORMAL (0)	FF (1)	HD (2)	DTV (3)
Main sharpness	"SHARPNESS"	0		3.0	6.0	11.9	17.9
		1		4.0	8.1	16.1	24.2
High f0 sharpness	"SHP_F1"	0		4.0	7.9	23.8	35.7
		1		5.4	10.8	32.3	48.4
Color dependent sharpness	"SHP_CD"	0		1.7	3.4	4.8	7.1
		1		2.3	4.6	6.5	9.7
LTI	"LTI_LEV"	0		2.0	4.0	6.0	8.9
		1		2.7	5.4	8.1	12.1
CTI	"CTI_LEV"	0		0.9	1.7	3.4	5.1
		1		1.2	2.3	4.6	6.9
VM output	"VM_LEV"	0	0	2.0	4.0	6.0	8.9
		1	0	2.7	5.4	8.1	12.1
		0	1	2.4	4.8	7.9	11.9
		1	1	3.2	6.5	10.8	16.1
		0	2	3.0	6.0	11.9	17.9
		1	2	4.0	8.1	16.1	24.2

Table 3. Center Frequency f0 Reference Values by Function

LTI/CTI Mode

The LTI/CTI function improves the input Y/CbCr signal slew rate. The center frequency f0 changes according to registers "SYSTEM" and "SHP_F0". (See Table 3 on page 60.)
In addition, this f0 determines the optimum input slew rate t0 for LTI/CTI.
t0 = 1/(2f0)

The LTI/CTI improvement mode can be changed by "LTI_MODE" and "CTI_MODE".
When a signal with the optimum input slew rate t0 for LTI/CTI is input:

0 = Normal mode (Black/white both-side improvement)
  The edges are corrected centering on a slew rate of 50%.
1 = Black side improvement mode
  The minus side from 50% is improved, and the slew rate is half from the original waveform.
2 = White side improvement mode
  The plus side from 50% is improved, and the slew rate is half from the original waveform.

See Fig. 15 for a description of the principle.

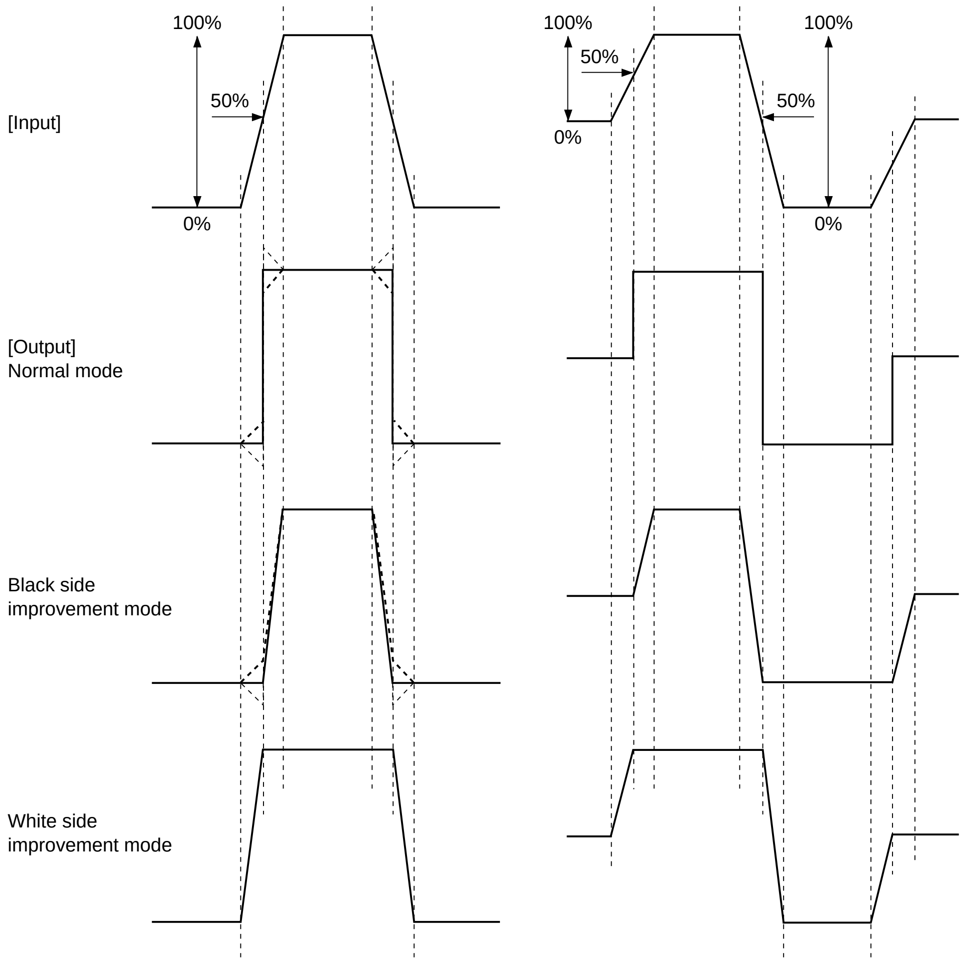


Fig. 15. Description of LTI/CTI Mode Principle

PRE_RGB Output

The PRE_RGB signal with the three R, G and B channels which have passed through the gamma circuit added is output to Pin 60 (PRE_RGB). (See Fig. 16.)

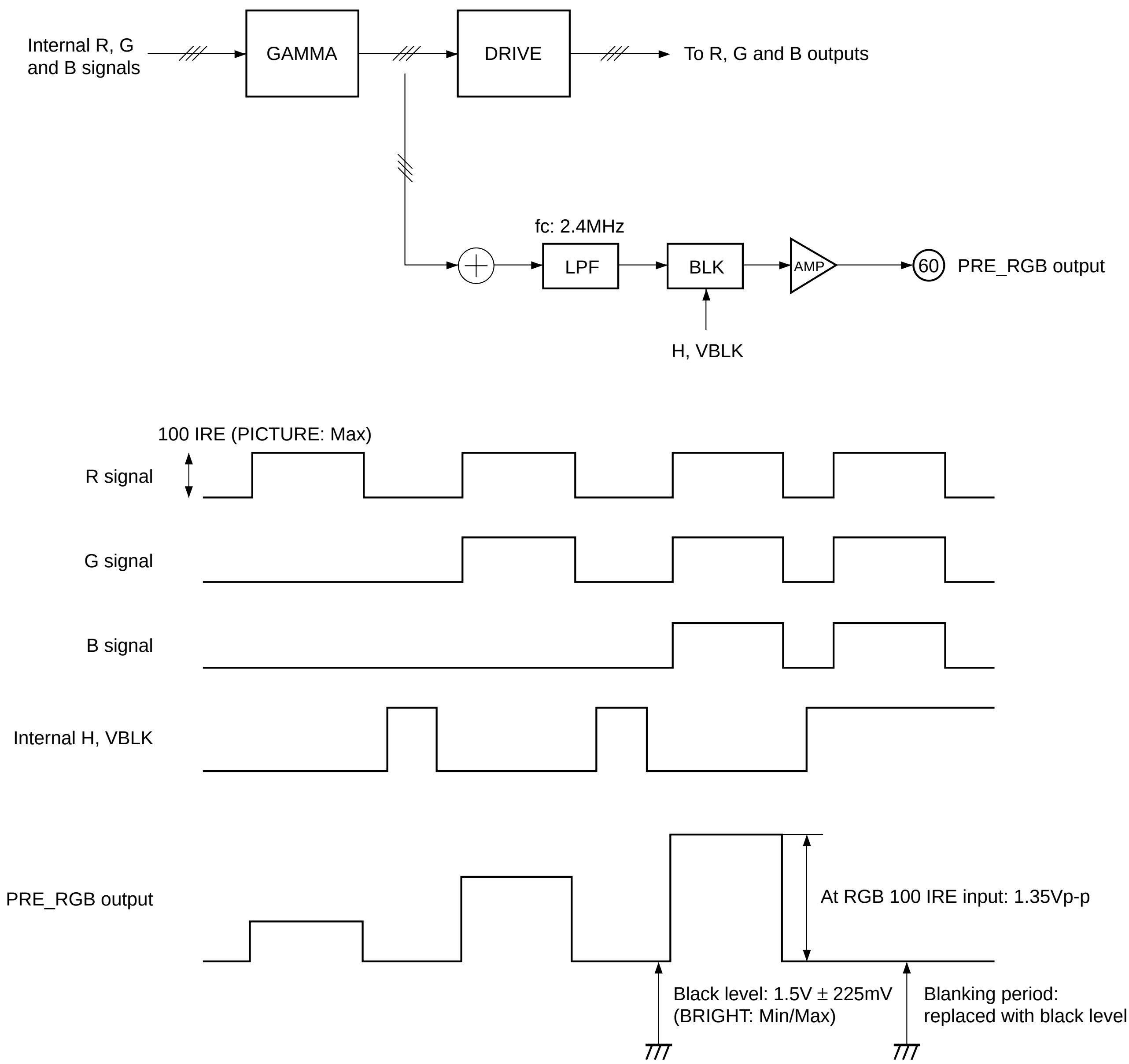


Fig. 16. Overview of PRE_RGB Output

The horizontal and vertical blanking periods are replaced with the black level(when there is no RGB input.). Also, the output DC level is linked to "BRIGHT" and "SUB_BRIGHT".

Passing the PRE_RGB output through an appropriate external LPF and inputting it to Pin 59 (SABL_IN) is effective for the short-loop RGB gain correction. Returning the PRE_RGB output to Pin 38 (L2_FIL) is also effective for AFC compensation using the RGB signal.

AKBOFF Mode

The CXA2150AQ also supports sets that do not use the AKB system. (AKBOFF mode)
AKBOFF mode is established by setting the register "AKBOFF" to 1.

- The R, G and B output DC levels are adjusted by "R, G, B_CUTOFF", respectively.
- The AKB reference pulse (REF-P) is not added to the R, G and B outputs.
- Connect Pin 58 (IK_IN) to GND via a capacitor.
- Two different DC levels can be selected for the R, G and B output horizontal and vertical blanking periods by "BLK_OFF".
- Like AKB mode, the HBLK period is set by "L/R_BLK" and the VBLK period is set by "AKBTIM" and "UP/LO_BLK".

Fig. 17 shows the RGB blanking in AKBOFF mode.

1) BLK_OFF = 0
- VBLK period level: Fixed at approximately 0.4 V
- HBLK period level: R, G and B are controlled together by "BLK_BTM".
- "BRIGHT" and "SUB_BRIGHT": Control only the effective video (non-blanking) period together for R, G and B.
- "R, G, B_CUTOFF": Control only the effective video period independently for R, G and B, respectively.

2) BLK_OFF = 1
- VBLK and HBLK period levels: Approximately 8 IRE (reference pulse level) when "BRIGHT" and "SUB_BRIGHT" are set to center.
- "BRIGHT" and "SUB_BRIGHT": Control only the effective video (non-blanking) period together for R, G and B.
- "R, G, B_CUTOFF": Control the entire period independently for R, G and B, respectively

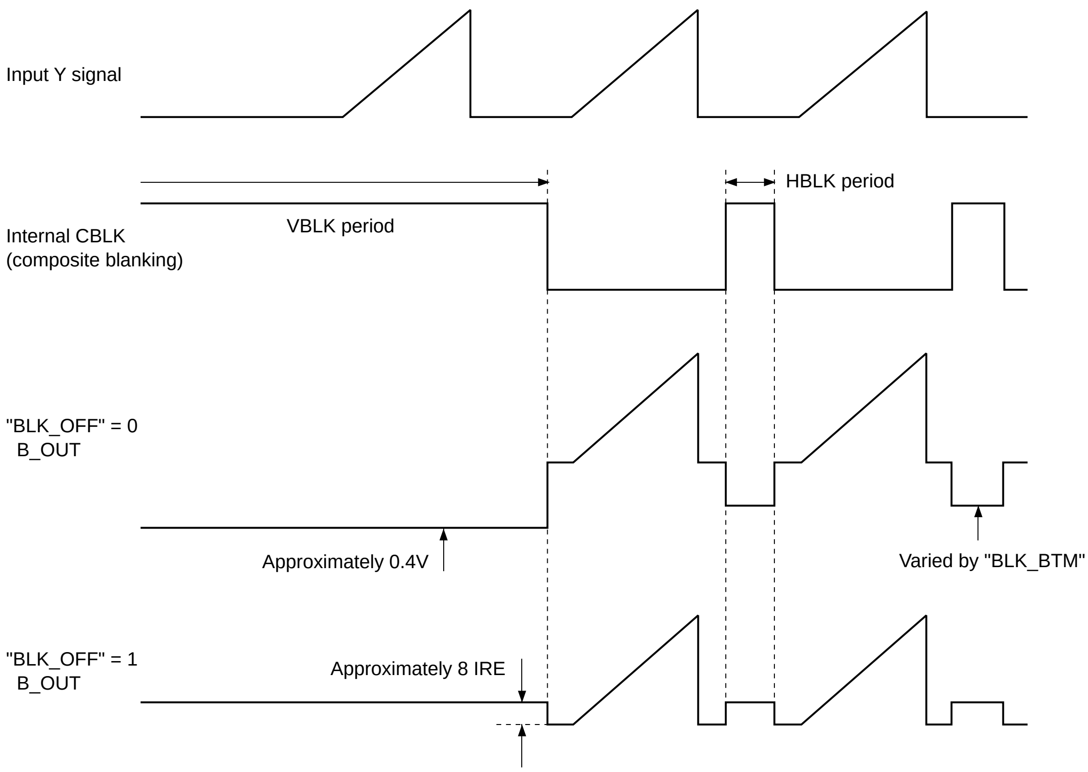


Fig. 17. RGB Blanking Period in AKBOFF Mode

Signal Processing

The CXA2150AQ consists of Y, color difference (Cb/Cr), RGB, horizontal deflection, and vertical deflection signal processing. All these types of signal processing are controlled by I^2C bus.

1. Y signal processing

A 0.7Vp-p (100 IRE) Y signal is input to Pin 20 (Y_IN) via a capacitor. This Y signal is input-clamped and passed through sharpness control, luminance transient improvement (LTI), DC transmission rate correction, and the auto pedestal circuits. It is then output to the MATRIX circuit. The Y signal's differential wave (VM signal) is output to Pin 14 (VM_OUT) with positive polarity.

The center frequency for sharpness (f0), LTI, and VM, along with the Y signal frequency response, change according to the "SYSTEM" and "SHP_F0" registers. (See Table 3 on page 60.)

The CXA2150AQ provides the following three types of sharpness features:

a) Main sharpness
The "SHARPNESS" register can be used to control the sharpness gain, while the "PRE/OVER" register can be used to control the pre-shoot/over-shoot ratio.

b) High f0 sharpness
"SHP_F1" can be used to control the sharpness gain at the higher center frequency level f1. This is useful for improving the high-frequency attenuation of a digital IC at the previous stage.

c) Color-dependent (CD) sharpness
The Y signal's low frequency is enhanced according to the Cr signal level only while the Cr input signal is positive. "SHP_CD" can be used to control the enhancement gain. "CD_OFF" can be used to turn off this feature. This feature is useful for enhancing the brightness change of the red elements on the screen.

The LTI generates contour correction signals at the Y signal's rising and falling edges and achieves contour enhancement by adding the correction signal to the original signal. "LTI_LEV" can be used to change the enhancement gain, and "LTI_MODE" can be used to change the improvement mode.

Pin 13 (YF_OFF) can achieve high-speed MUTE on the VM signal, sharpness feature, and color signal. See the pin description. The VM signal's output amplitude can be modulated by applying voltage to Pin 15 (VM_MOD). Both pins can be used as parameters for image-quality control.
There are five control registers for the VM signal:

"VM_LEV" : VM output gain control
"VM_F0" : The VM signal's center frequency control during differentiation
"VM_DLY" : Control of the phase difference between the VM signal and the output RGB signal
"VM_COR" : Coring level control for improving the VM signal's S/N
"VM_LMT" : The VM signal's dynamic range control based on the internal limiter level

The "DC_TRAN" register can be used to adjust the DC transmission rate between 103% and 80% by detecting the input signal's APL. A change of brightness caused by the input Y signal's DC offset can be reduced by "Y_OFFSET". Auto pedestal is a black-level correction circuit that detects the black elements in an input signal and automatically pulls any part below the specified level to the pedestal level. The point of inflection can be adjusted using the "DPIC_LEV" register. In addition, Pin 12 (DPDT_OFF) stops the operation of the automatic pedestal circuit and the signal interval detection that is used to control the DC transmission rate. For details, see the pin description.

This IC is equipped with two registers that can be used for aging on the production line:
"AGING_W": Full white output
"AGING_B": Full black output

2. Color difference (CbCr) signal processing

Cb/Cr color difference signals with 0.7Vp-p (100 IRE) are input to Pins 21 (CB_IN) and 22 (CR_IN) via a capacitor. The Cb/Cr signal is input-clamped and passed through chrominance transient improvement (CTI), HUE control, color control, and the detection axis setting circuit. It is then output to the MATRIX circuit.

Similar to the LTI, the CTI generates contour-correction signals at the color difference signal's rising and falling edges and achieves contour enhancement by adding the correction signal to the original signal. "CTI_LEV" can be used to change the enhancement gain, while "CTI_MODE" can be used to change the improvement mode. The central frequency for CTI changes according to "SYSTEM" and "SHP_F0". (See Table 3 on page 60.)

With the color gain control amplifier, setting "COLOR" data to "00h" results in color-off mode. Pin 13 (YF_OFF) can also be used to turn the color off. See the pin description.

The detection axis setting circuit sets the angles of the R-Y and G-Y axes and their weighting factor with the B-Y axis fixed. "COL_AXIS" can set four angles and weighting factors, so that an appropriate setting can be selected according to the destination.
The signal is converted to three different color signals (R-Y, G-Y, and B-Y) by the AXIS circuit, and then input to the MATRIX circuit along with the Y signal to obtain the RGB primary colors.

3. RGB signal processing

The RGB signals are output after passing through YSYM1, white balance switching, picture control, sub-contrast control, bright/sub-bright control, YSYM2, amplitude limiter, dynamic color, gamma correction, drive control, cut-off control, and H and V blanking circuits.

Pin 7 (YSYM1) either tones down the main signal to about 1/3 (YM) or switches it to the RGB1 analog input signal, (YS). Apply a control signal to this pin. See the pin description. The signal output from the YSYM1 circuit enters the white balance SW, where the R-G-B balance can be changed by "WB_SW".

The picture control has a variable range of about 13dB. The sub-contrast control has a variable range of about –0.9 to +1.2 dB. The bright/sub-bright control has a variable range of ±14 IRE.

Pin 2 (YSYM2) either tones down the main signal or the RGB1 analog signal to about 1/3 (YM) or switches it to the RGB2 analog input signal, (YS). Apply a control signal to this pin. See the pin description. The RGB2 analog signal can be controlled by brightness including ABL, but picture control and white balance SW have no effect. "LRGB2_LEV" can be used to independently adjust the amplitude. The amplitude limiter is activated when the input signal's amplitude is too high. "PLIMIT_LEV" is used to select the desired input amplitude level at which the limiter is to be activated. This can be used to protect TV sets against excessive input.

The signal obtained is then passed through dynamic color, gamma correction, and drive control (RGB independently adjustable), placed under the AKB system's cut-off control, and then output via a buffer.

If 75% of the R-signal level is less than G or B, the dynamic color controls the gain of R and B to increase the picture's color density. "DCOL" can be used to change this effect.
Furthermore, this IC is equipped with a built-in peak ABL. It limits the peak video signal by detecting the RGB output signal's peak level and then reducing the picture gain. The detection voltage can be changed by "P_ABL". Select an appropriate feedback time constant by forming an external LPF using Pin 11 (PABL_FIL).

To Pin 56 (ABL_IN), input a voltage, which represents the anode current via an external LPF with a range of 0 to 5V. The voltage applied to ABL_IN is compared with three internal reference voltage values and then is charged/discharged by the capacitor connected to Pin 57 (ABL_FIL). "ABL_TH" can be used to change the internal reference voltage. The effect of ABL on the RGB signal corresponds to the voltage on the ABL_FIL pin. (See the curve data.) The ABL feature includes picture ABL for suppressing the RGB signal's amplitude and brightness ABL for reducing the DC level; the desired mode can be set using "ABL_MODE".

At Pin 60 (PRE_RGB), a PRE_RGB signal, which is obtained by mixing the signals from three channels (R, G and B) after the gamma correction circuit, is output via LPF (fc: 2.4MHz). This PRE_RGB signal is useful for AFC correction by the RGB signal if it is fed back to Pin 38 (L2_FIL) via an appropriate external LPF. The ABL feature is also applicable to the voltage that is applied to Pin 59 (SABL_IN), in which case its effects can be adjusted using "S_ABL". This is useful for ABL correction with a short loop, if the PRE_RGB signal is input to SABL_IN via an appropriate external LPF. At the output stage, "BLK_BTM" can be used to set the voltage at the H blanking section. This voltage is defined as the voltage difference from AKB's reference-pulse DC. Therefore, the absolute voltage value varies from R to G to B according to the status of AKB, but is not affected by the setting of DC level controls such as brightness.

The AKB system (auto cut-off feature) automatically adjusts bias on the cut-off side by forming a loop between the CRT and this IC. This loop can also compensate for the CRT's change over its lifetime. This system adjusts color density using "R, G, B_DRV" for adjusting gain between RGB outputs with the I^2C bus and "R, G, B_CUTOFF" for adjusting the DC level while AKB is active.

AKB operation is described as follows. (For the timing chart of reference-pulse output, see Fig. 3 on page 48.)

- On the upper part of the screen (overscan section), the reference pulses for AKB are output in the order of RGB by shifting one line at a level of 8 IRE.
- Detects the cathode current generated by each reference pulse that was output, converts it to a voltage, then inputs it as IK to Pin 58 (IK_IN) via a capacitor. Because this IK signal is input-clamped, be sure to input the signal at a stable level during V blanking, immediately before the reference pulse.
- Compares the IK_IN input voltage with the IC's internal reference voltage and samples the signal by charging/discharging it, using an internal capacitor, at each reference pulse interval for R, G and B. This process is inhibited beyond the reference pulse interval.
- Changes the DC level of R, G, B_OUT according to the internal capacitor's voltage. This is repeated for each field until the clamped IK signal's voltage at each reference pulse interval for R, G and B becomes equal to the IC's internal reference voltage. The reference voltage is provided for each instance of R, G and B and can be changed by "R, G, B_CUTOFF".

When the set's power is turned on, the IK signal's reference pulse voltage remains low until the cathode is warmed up. Therefore, the internal capacitor's voltage is set to the maximum level, and R, G, B_OUT's DC level is set to the maximum value. When the cathode is warmed up and the IK signal's level rises, the internal capacitor's voltage starts falling from its maximum level, and R, G, B_OUT's DC level also starts falling. The AKB loop then becomes stable and converges.

The CXA2150AQ returns a value of "1" to the "IKR" status register when the levels of all R, G and B internal capacitors drop below the specified maximum level. When the CXA2150AQ's power is turned on, the internal capacitors' voltage starts from the GND level; therefore, "1" may be returned to IKR before the AKB loop converges. Mask reading of the "IKR" status register for an appropriate length of time after powering up this IC.

This IC provides an AKBOFF (manual cut-off) mode. When the "AKBOFF" register is set to 1, R, G, B_OUT's DC level is controlled by "R, G, B_CUTOFF". In this case, drop Pin 58 (IK_IN) to GND with a capacitor. The "BLK_OFF" register takes effect only in the AKBOFF mode. When BLK_OFF = 0, H and V blanking are applied to the RGB signals. When BLK_OFF = 1, the H and V blanking intervals for the RGB signal are output at a level of +8 IRE.

4. Horizontal deflection signal processing

1) H sync input

A positive polarity horizontal synchronizing signal with about 5Vp-p is input to Pin 26 (HS_IN) using DC coupling or AC coupling with a capacitor. For the phase and width of input H sync, see Fig. 13 on page 58. For the CXA2150AQ, inputting continuous H sync is recommended during V intervals, so it is also recommended that PLL exists at the previous stage.

2) AFC 1st loop

The CXA2150AQ employs a VCO that uses a ceramic oscillator in the horizontal oscillator circuit (fc: 2.696874MHz). Its division value is determined by the settings of Pins 23 (F0) and 24 (F1) to support five different horizontal deflection frequencies fH. (fH: 15.7, 31.5, 33.75, 37.9, or 45kHz; see Table 1 on page 44.)

The AFC 1st loop is obtained by comparing the phase of the input H sync with the phase of the internal H reference pulse (HREF1), which is obtained by dividing the 2.7MHz-VCO output. The "SYNC_PHASE" register can be used to shift to the phase of HREF1. This is useful when a Y signal's phase is delayed compared to the H sync signal at the previous stage.

The 1st loop's response characteristics are set using the lag lead filter constant at Pin 32 (AFC_FIL) and the "AFC_MODE" register. If AFC is locked with input H sync, a value of "1" is output to the "HLOCK" status register, and the result of the comparison of internal free-running frequency and input frequency is output to "HCENT". This status is useful for detecting an input signal.
"CLP_PHASE" and "CLP_SHIFT" can be used to control the phases of CXA2150AQ's internal clamp pulse and the clamp pulse superimposed on SCP output at Pin 27. "CLP_GATE" can be used to set whether or not to gate the clamp pulse during the input H sync's High period.

3) AFC 2nd loop
The AFC 2nd loop is obtained by comparing the phase of the reference H pulse derived from the 1st loop (HREF2) with the phase of the horizontal deflection pulse input to Pin 39 (HP_IN) (H pulse) to control the phase of H_DRV output (Pin 40). "H_POSITION" can be used to adjust the phase of HREF2. In other words, it is used to control the horizontal position of the video image that is displayed on the CRT. Additionally, "AFC_BOW, ANGLE" are used to correct the distortion of vertical lines by superimposing a correction signal derived from the V-shaped saw-tooth wave. The high voltage fluctuations correction signal that is input to Pin 35 (HCOMP_IN) can be used to correct high voltage fluctuations in the horizontal direction. The amount of correction can be changed by using "AFC_COMP".

For the delay between the H_DRV signal and H pulse generation, that is, the HOUT storage time, this IC provides two different modes that can be set using pins 23 (F0) and 24 (F1). (See Table 1 on page 44.)

The H pulse input to Pin 39 (HP_IN) is used for horizontal blanking, which is superimposed on the R, G, B and SCP output. When HBLK_SW = 1, "L, R_BLK" can be used to control horizontal blanking on the screen for R, G, B outputs and the horizontal blanking pulse that is superimposed on SCP output.

Since H_DRV output is an open collector connect a resistor of about 2.7kΩ to $V_{CC}9$. Additionally, limit the high voltage to 5V by connecting a 3.3kΩ resistor to GND to protect the H_DRV output from over voltage. H_DRV output is equipped with start/stop features at the time of power ON/OFF. These features are activated automatically. When Pin 29's VREG5 terminal voltage is about 4V or lower, H_DRV is off and its output is fixed at the High level.
Furthermore, to protect the TV set, the input pin HPROT (Pin 34) is provided to stop horizontal deflection. If a voltage of about 2V is applied to Pin 34 (HPROT) for more than seven V cycles, H_DRV output is set to off (High level) and RGB output is totally blanked. In this case, a value of "1" is output to the "HNG" status register. To reset this status, power down the IC once and then start it up again.

5. Vertical deflection signal processing

1) V sync input
A positive polarity vertical synchronizing signal with about 5Vp-p is input to Pin 42 (VS_IN). (The High period must be at least 3H.) An internal V sync is generated from input V sync using its rising edge as a trigger. Therefore, the input V sync's rising phase is important. There must be no H sync, equivalent pulse, or instability, because sync separation is assumed to be completed on the input V sync at the previous stage of this IC.

2) Vertical synchronization processing

The mode of the interval V countdown system is determined by the horizontal deflection frequency (fH) settings at pins F0 and F1 and the "VFREQ" register. (See Table 2 on page 46.) The number of lines defined by fH setting are loaded to operate the UP & DOWN counter. The counter is reset at the rising edge of the input V sync. Note that V sync detection is masked for a period equivalent to approximately 1/2 the regular lines in order to reject continuous noise during channel change. When V sync input doesn't exist, internal V sync becomes free running at about +12.5% more lines than regular. In other words the V countdown system's pulling range is about –50% to +12.5% of regular lines.

Synchronized to internal V sync, various timing pulses are generated:

- VOSC reset pulse
  The vertical deflection retracing timing can be changed with respect to the video signal by switching the VOSC reset timing before or after V sync using "RST_SW".
- Sampling pulse for the VAGC circuit
- R, G and B references pulse for AKB
  "AKBTIM" is used to set the reference pulse timing. The pulse generated is sent to the RGB signal processing section, where it is superimposed on the RGB signals.
- V blanking pulse
  The time from internal VSYNC to the Bch reference pulse is the reference V blanking interval. "UP, LO_BLK" can be used to increase the vertical blanking interval on the screen. The V blanking pulse is not only sent to the RGB signal processing section but also output as a VTIM signal at Pin 54 (VTIM).
- Clamp pulse for IK input and V blanking pulse for SCP
  The pulse from the beginning of V blanking up to the Rch reference pulse is used as the clamp pulse for the IK input signal and as the V blanking pulse that is superimposed on SCP output.

3) VOSC (oscillator) section

This IC employs an AGC circuit for VOSC. The AGC circuit suppresses unnecessary transient responses that may occur during channel change.
The reference SAW waveform is derived by charge/discharge of the capacitance connected to Pin 48 (V_OSC). This reference SAW signal is compared with the internal reference voltage at the time of the sampling pulse, and AGC is activated by controlling the voltage of the capacitance connected to Pin 49 (V_AGC). To prevent sag on the V retrace rising edge, the V_OSC (Pin 48) capacitor should use a material (such as polypropylene) with low internal resistance.

4) Wide-mode support block

The reference SAW signal generated at VOSC is input to the wide-mode block. In this block, control is provided for the wide modes "V_ASPECT", "V_SCROLL", "UP, LO_VLIN", "JMP_SW", and "ZOOM_SW". When ZOOM_SW = 1, the SAW signal adjusted by "V_ASPECT", etc., is limited vertically, in which case the setting VBLK_SW = 0 adds the limited interval to V blanking. During zoom mode, the OSD display position should be controlled by the microcomputer without using the VTIM signal.

When ASP_SW = 1, the amplitude of the V_DRV output signal increases by about 10%, and 22 lines of V blanking are added at the top and bottom of the screen. This feature is useful for stretching the source when there are not enough valid video lines.

The SAW signal output from the wide-mode block is input to the block that forms each V output signal. Therefore, all V system output signals are handled in wide mode.

5) Various V system output signals

The V_DRV– and V_DRV+ signals are output to Pins 52 and 53, respectively. These signals are used as the vertical deflection signal. At first power on, "V_ON" is preset to "0"; so V_DRV+ and V_DRV– are DC output. The VSAW waveform is not output until "1" is written to the control register. It is recommended to write "1" after degaussing is complete. Adjustments available for the V_DRV signal include: "V_SIZE", "V_POSITION", "V_LIN", and "S_CORRECTION". "VDRV_SW" increases the V_DRV signal level by about 5% in the interval up to the Bch reference pulse. Its purpose is to physically separate the reference pulse away from the video signal. The high voltage fluctuation correction signal that is input to Pin 37 (VCOMP_IN) can be used to correct high voltage fluctuation of the vertical picture size. The amount of correction can be changed using "V_COMP".

At Pin 47 (EW_DRV), a parabolic wave with a cycle of V is output. This is used to correct the horizontal picture size and pin distortion. Available adjustments are: "H_SIZE", "PIN_AMP", "PIN_PHASE", "UP, LO_CPIN", and "UP, LO_UCG, UCP".

The high voltage fluctuation correction signal input to Pin 36 (HCOMP_IN) can be used to correct high voltage fluctuation of the horizontal picture size and pin distortion. The amount of correction can be changed using "H_COMP" and "PIN_COMP".

VSAW0 and VSAW1 at Pins 50 and 51 are the V-shaped, saw-tooth waves that allow DC level and amplitude to be controlled independently. They are useful for vertical pin distortion correction circuits, picture rotation (horizontal trapezoidal distortion) correction circuits, etc.

At Pin 46 (DF_PARA), a parabolic wave with a cycle of V is output. This can be used to modulate the amplitude of the dynamic focus voltage at a vertical cycle. At Pin 43 (HC_PARA), a parabolic wave with a cycle of V is output. This can control DC level and the SAW element's amplitude and parabolic amplitude. It is useful for correcting the asynchronous element of the raster position and raster distortion.

At Pin 45 (MP_PARA), a parabolic wave with a cycle of V is output. This can control the DC level and parabolic amplitude. It is useful for a PWM circuit that switches an S-shaped capacitor during a trace interval to control horizontal linearity.

Furthermore, a VPROT input pin (Pin 35) is provided to forcibly turn off RGB output in the event of a V deflection error on the TV set. If input to Pin 35 (VPROT) remains erroneous for more than three V cycles, RGB output is totally blanked. In this case, a value of "1" is written in the "VNG" status register. For the input conditions, see Fig. 14 on page 59.

Notes on Operation

- Because the R, G and B signals output from the CXA2150AQ are DC direct connected, the pattern (set board) must be designed with consideration given to minimizing interface from around the power supply and GND. Do not separate the GND patterns for each pin. A solid earth is ideal. Design the power supply as low impedance as possible. Locate the by-pass capacitor which is inserted between the power supply and GND as near to the pin as possible.
  Also, it is recommended that buffers be connected to R, G and B_OUT as close to the IC as possible.

- Input the Y/Cb/Cr and R/G/B signals at a sufficiently low impedance, as these inputs are clamped by the capacitors connected to the pins.

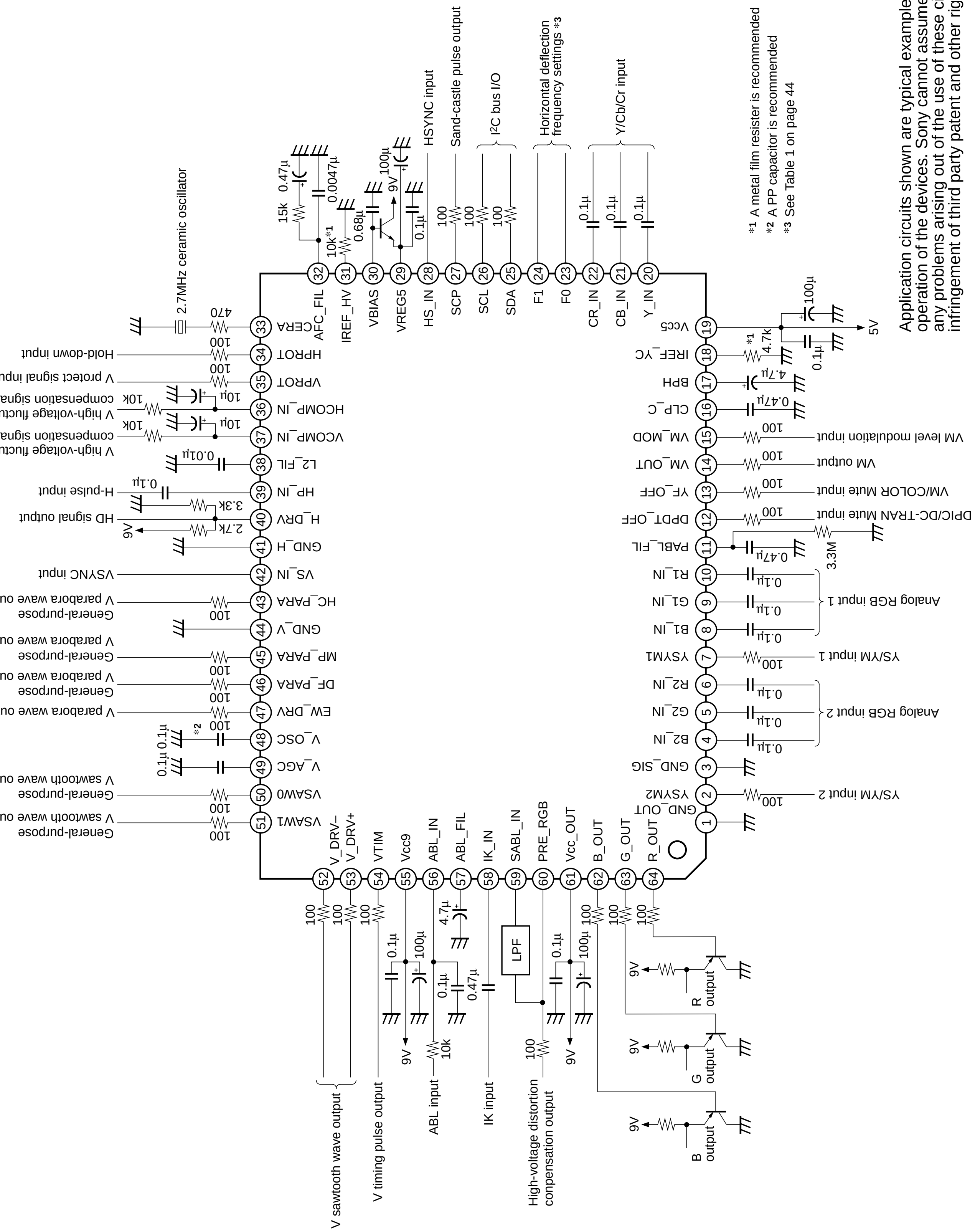
- The 5V regulator is formed by connecting a NPN-Tr between Pin 29 (VREG5) and Pin 30 (VBIAS). The regulator is for controlling the relation between rising and falling of $V_{CC}9$ supply and of VREG5 voltage that is a CXA2150AQ's horizontal supply. Locate the NPN-Tr and by-pass capacitors as close to the pins as possible. When 5V is supplied to the VREG5 pin from an external source, separate from the signal system power supply $V_{CC}5$ and open Pin 30 (VBIAS).

Notes for each pin are shown in Table 4.

Pin No.	Pin name	Notes on operation and processing when unused
1	GND_OUT	Design as solid a pattern as possible, and be common to Pin 3 (GND_SIG).
2	YSYM2	Unused, connect to GND.
3	GND_SIG	Design as solid a pattern as possible, and be common to Pin 1 (GND_OUT).
4	B2_IN	Unused, connect to GND via a 0.1µF capacitor.
5	G2_IN	Unused, connect to GND via a 0.1µF capacitor.
6	R2_IN	Unused, connect to GND via a 0.1µF capacitor.
7	YSYM1	Unused, connect to GND.
8	B1_IN	Unused, connect to GND via a 0.1µF capacitor.
9	G1_IN	Unused, connect to GND via a 0.1µF capacitor.
10	R1_IN	Unused, connect to GND via a 0.1µF capacitor.
11	PABL_FIL	
12	DPDT_OFF	Unused, connect to GND.
13	YF_OFF	Unused, connect to GND.
14	VM_OUT	Connect a buffer as close as possible.
15	VM_MOD	Unused, connect to Vcc5.
16	CLP_C	
17	BPH	
18	IREF_YC	Connect to GND via a 4.7kΩ resistor with an error of 1% or less with a short pattern.
19	Vcc5	Connect a by-pass capacitor nearby with thick pattern to flow approximately 80mA current.
20	Y_IN	
21	CB_IN	
22	CR_IN	
23	F0	As horizontal deflection frequency is 33.75kHz, connect to GND.
24	F1	As horizontal deflection frequency is 33.75kHz, connect to Pin 29 (VREG5).
25	SDA	
26	SCL	
27	SCP	
28	HS_IN	Input DC coupled.
29	VREG5	Connect a by-pass capacitor nearby with thick pattern.
30	VBIAS	Locate a NPN-Tr for feed-back and by-pass capacitors as close as possible.
31	IREF_HV	Connect to GND via a 10kΩ resistor with an error of 1% or less with short pattern.
32	AFC_FIL	Locate external parts as near as possible.
33	CERA	Locate external parts as near as possible.
34	HPROT	Unused, connect to GND.
35	VPROT	Input with the condition of Fig. 14 on page 59.
36	HCOMP_IN	Unused, connect to VREG5.
37	VCOMP_IN	Unused, connect to VREG5.
38	L2_FIL	Locate external parts as close as possible.
39	HP_IN	
40	H_DRV	Locates the register for pull-up as close as possible.
41	GND_H	Design as solid a pattern as possible.
42	VS_IN	Input DC coupled.
43	HC_PARA	
44	GND_V	Design as solid a pattern as possible.
45	MP_PARA	
46	DF_PARA	
47	EW_DRV	
48	V_OSC	Use a capacitor, such as polypropylene, with a small tanδ.
49	V_AGC	Locate external parts as close as possible.
50	VSAW0	
51	VSAW1	
52	V_DRV–	
53	V_DRV+	
54	VTIM	
55	Vcc9	Connect a by-pass capacitor nearby with thick pattern.
56	ABL_IN	Unused, connect to Vcc5.
57	ABL_FIL	
58	IK_IN	Unused, connect to GND via a 0.1µF capacitor.
59	SABL_IN	Unused, connect to GND.
60	PRE_RGB	
61	Vcc_OUT	Connect a by-pass capacitor nearby with thick pattern.
62	B_OUT	Connect a buffer as nearby as possible.
63	G_OUT	Connect a buffer as nearby as possible.
64	R_OUT	Connect a buffer as nearby as possible.

Table 4. Notes on The Operation of Each Pin

Application Circuit



*1 A metal film resister is recommended
*2 A PP capacitor is recommended
*3 See Table 1 on page 44

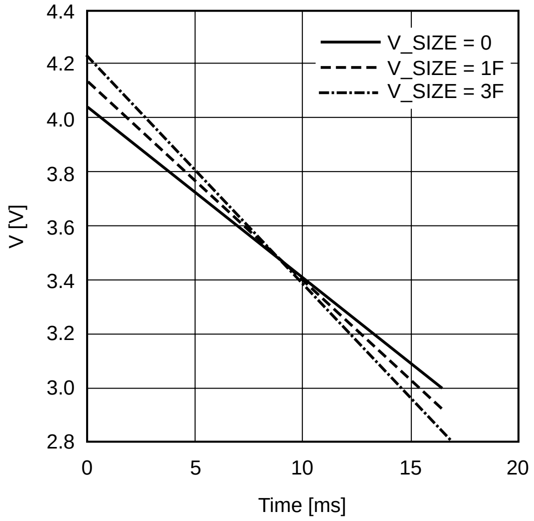
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Curve Data

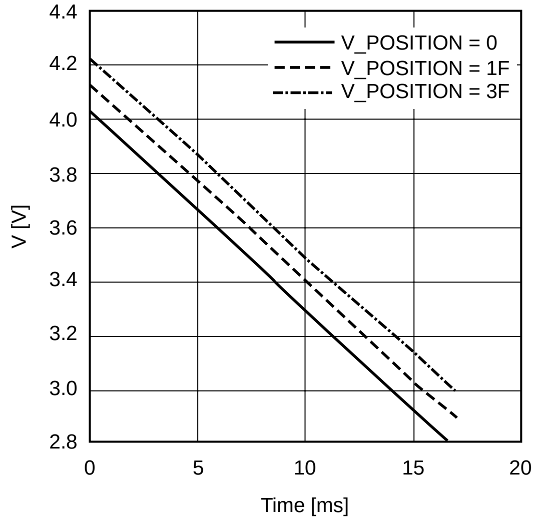
(I^2C bus data conforms to the "I^2C bus Register Initial Setting" of the Electrical Characteristics Measurement Conditions (P. 20).)

1) V_DRV+

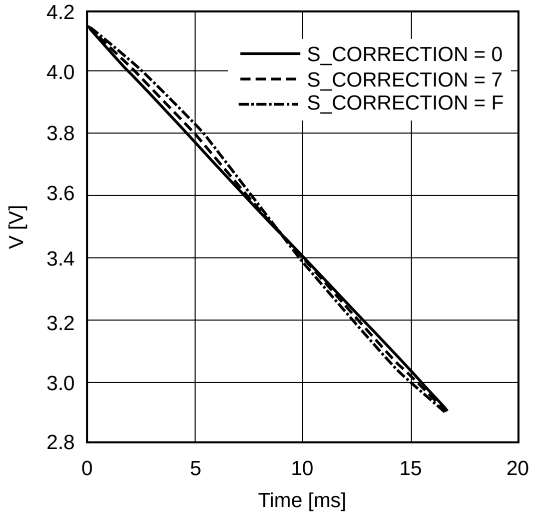
V_SIZE



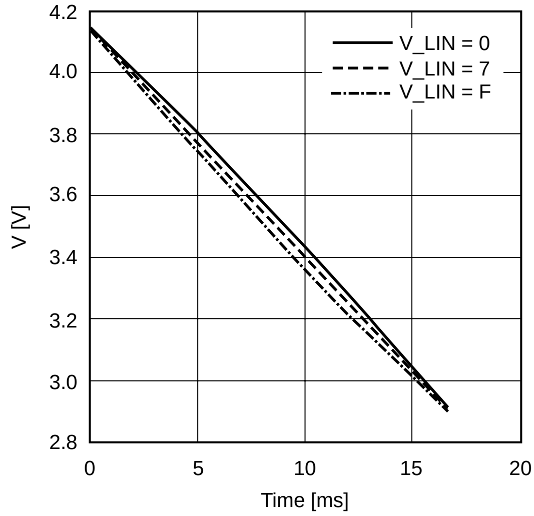
V_POSITION



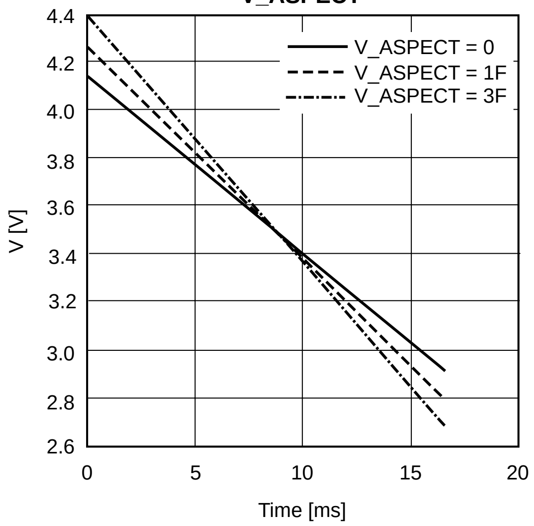
S_CORRECTION



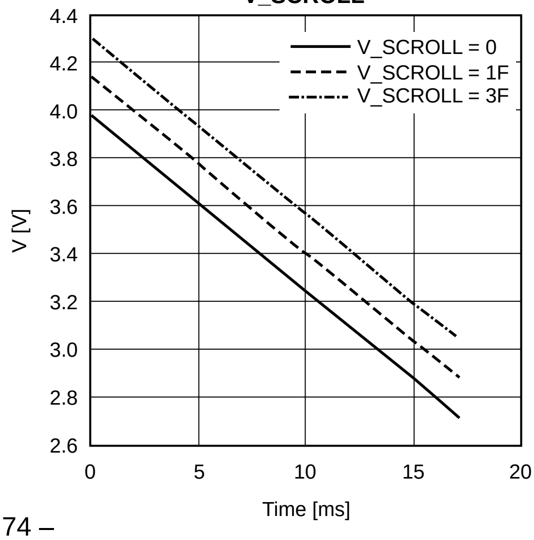
V_LIN

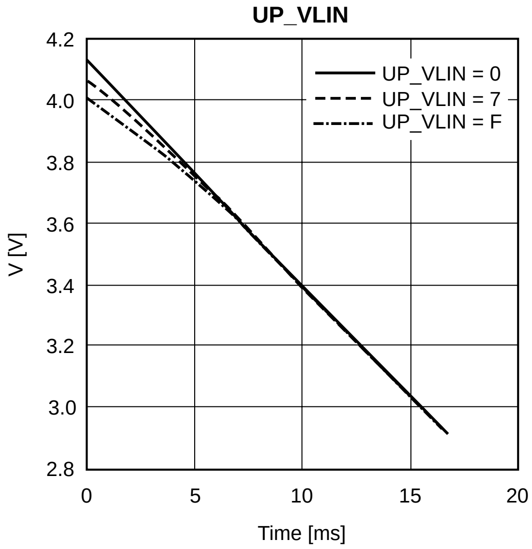


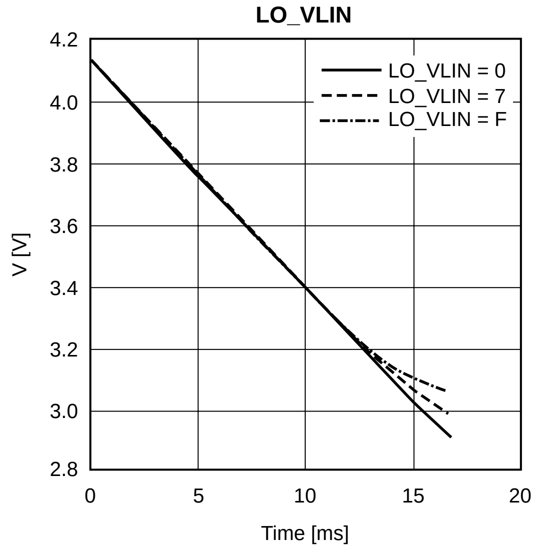
V_ASPECT

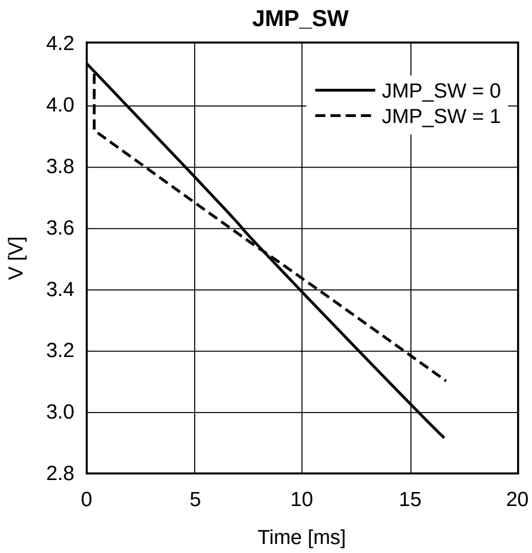


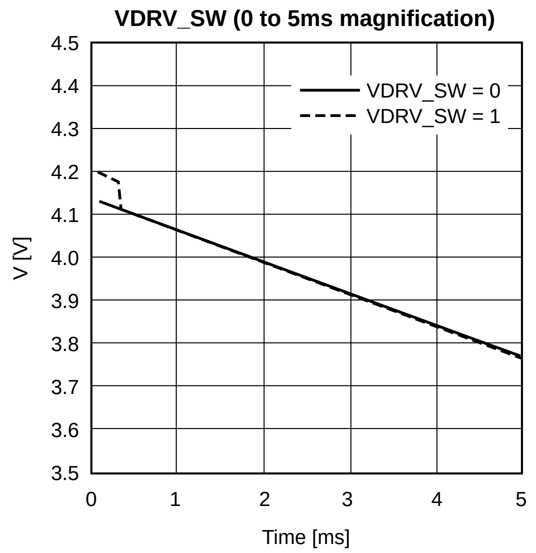
V_SCROLL

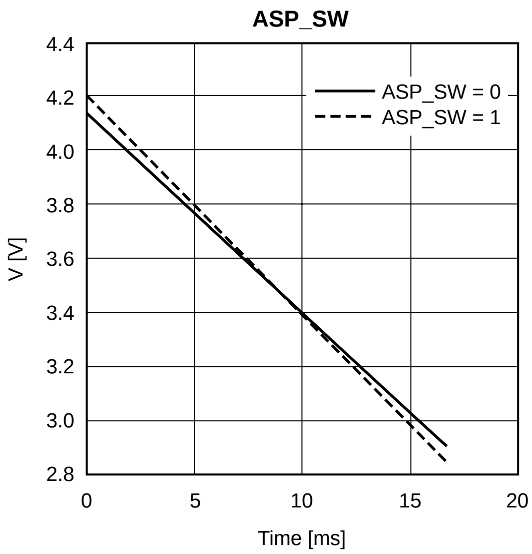



UP_VLIN
UP_VLIN = 0
UP_VLIN = 7
UP_VLIN = F
V [V]
4.2
4.0
3.8
3.6
3.4
3.2
3.0
2.8
0
5
10
15
20
Time [ms]

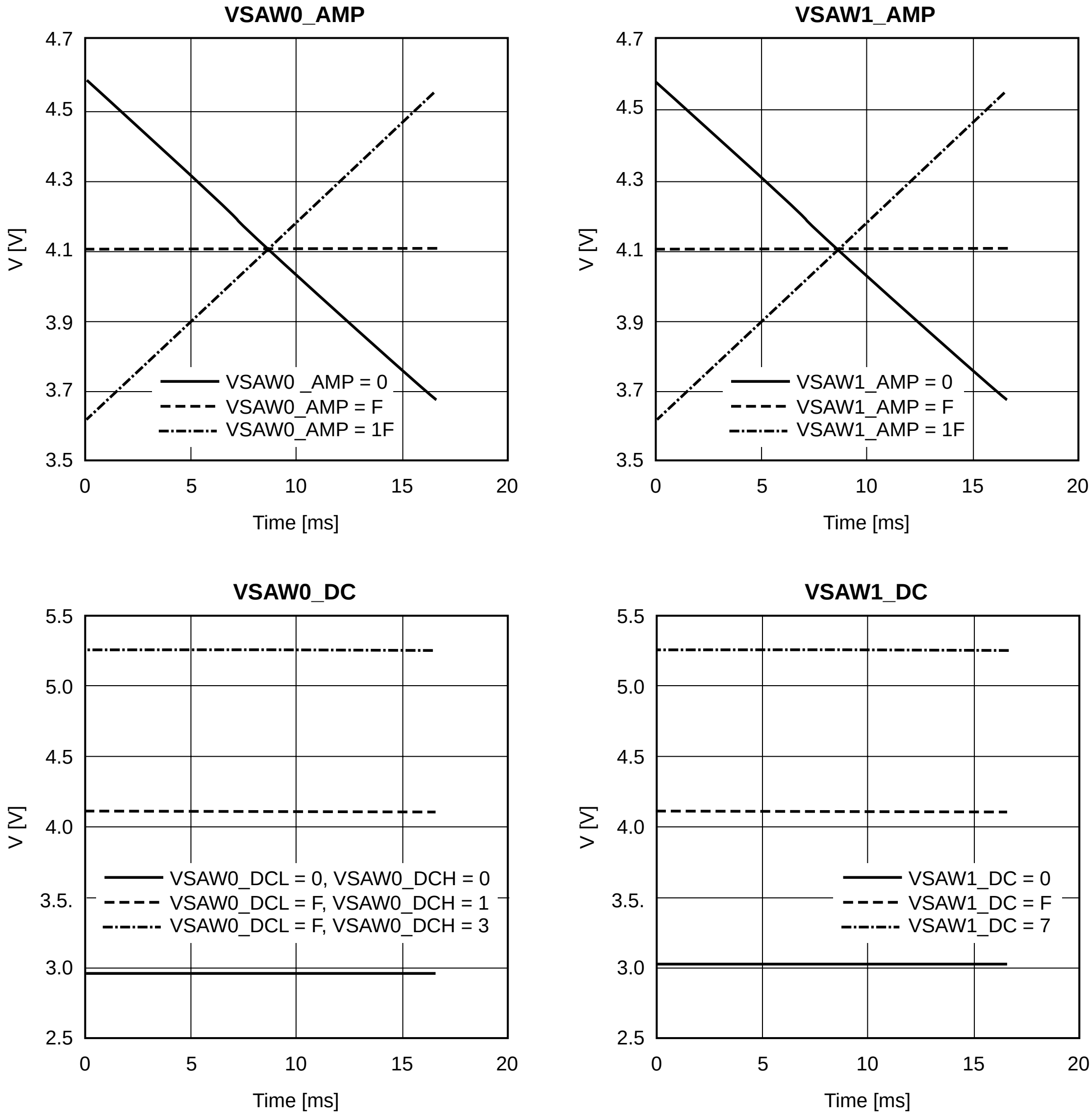

LO_VLIN
LO_VLIN = 0
LO_VLIN = 7
LO_VLIN = F
V [V]
4.2
4.0
3.8
3.6
3.4
3.2
3.0
2.8
0
5
10
15
20
Time [ms]


JMP_SW
JMP_SW = 0
JMP_SW = 1
V [V]
4.2
4.0
3.8
3.6
3.4
3.2
3.0
2.8
0
5
10
15
20
Time [ms]

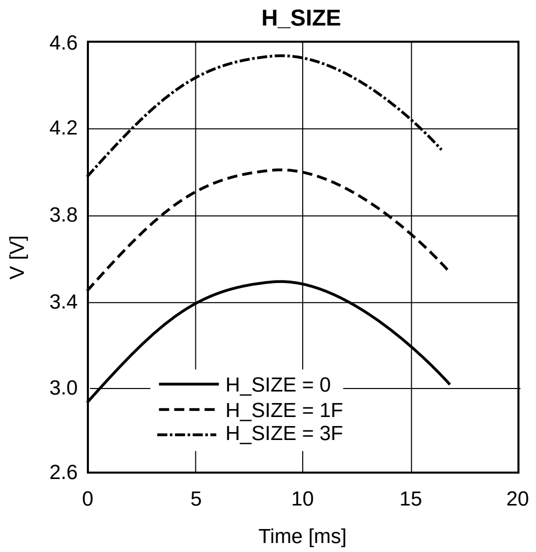

VDRV_SW (0 to 5ms magnification)
VDRV_SW = 0
VDRV_SW = 1
V [V]
4.5
4.4
4.3
4.2
4.1
4.0
3.9
3.8
3.7
3.6
3.5
0
1
2
3
4
5
Time [ms]

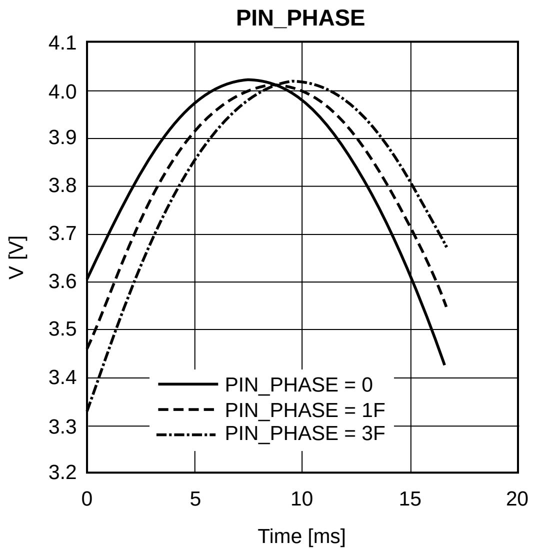

ASP_SW
ASP_SW = 0
ASP_SW = 1
V [V]
4.4
4.2
4.0
3.8
3.6
3.4
3.2
3.0
2.8
0
5
10
15
20
Time [ms]

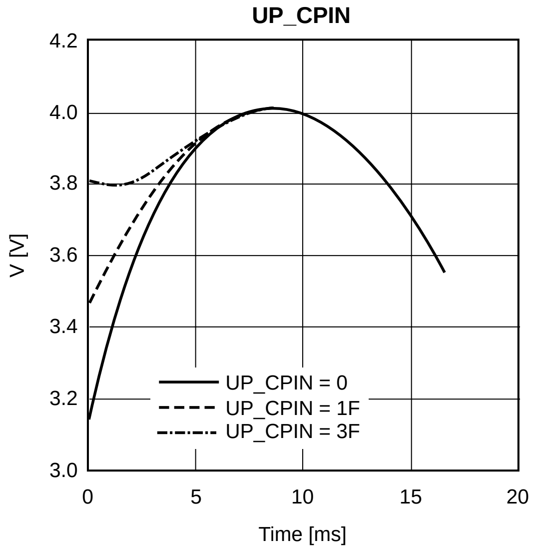
2) V_SAW0, 1

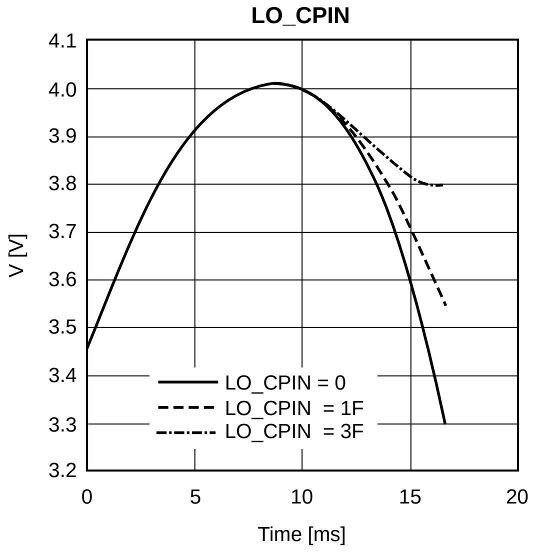

VSAW0_AMP
V [V]
4.7
4.5
4.3
4.1
3.9
3.7
3.5
0
5
10
15
20
Time [ms]
VSAW0 _AMP = 0
VSAW0_AMP = F
VSAW0_AMP = 1F
VSAW1_AMP
V [V]
Time [ms]
VSAW1_AMP = 0
VSAW1_AMP = F
VSAW1_AMP = 1F
VSAW0_DC
V [V]
5.5
5.0
4.5
4.0
3.5.
3.0
2.5
Time [ms]
VSAW0_DCL = 0, VSAW0_DCH = 0
VSAW0_DCL = F, VSAW0_DCH = 1
VSAW0_DCL = F, VSAW0_DCH = 3
VSAW1_DC
V [V]
Time [ms]
VSAW1_DC = 0
VSAW1_DC = F
VSAW1_DC = 7

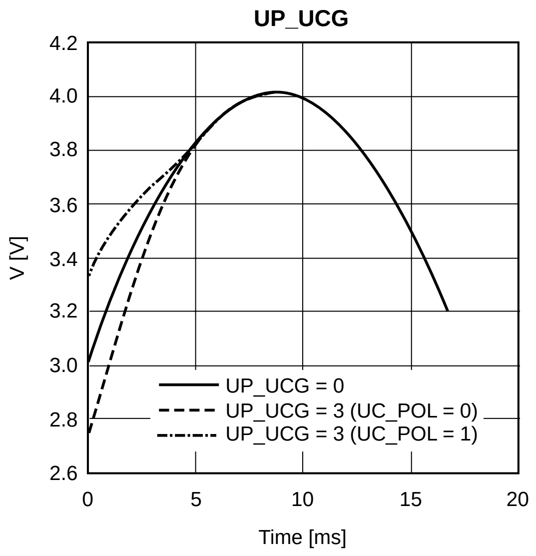
3) EW_DRV

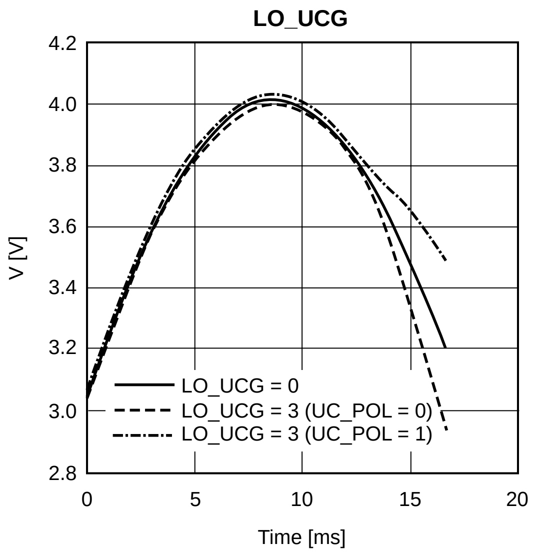

H_SIZE
V [V]
Time [ms]
H_SIZE = 0
H_SIZE = 1F
H_SIZE = 3F


PIN_PHASE
V [V]
Time [ms]
PIN_PHASE = 0
PIN_PHASE = 1F
PIN_PHASE = 3F

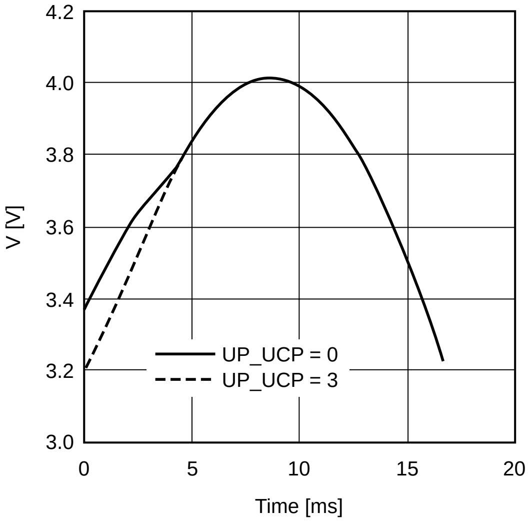

UP_CPIN
V [V]
Time [ms]
UP_CPIN = 0
UP_CPIN = 1F
UP_CPIN = 3F


LO_CPIN
V [V]
Time [ms]
LO_CPIN = 0
LO_CPIN = 1F
LO_CPIN = 3F

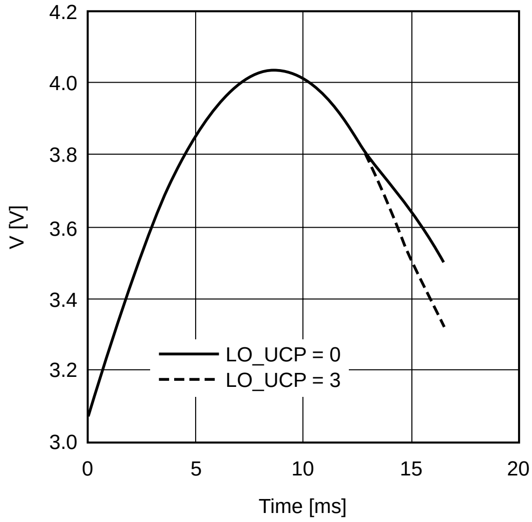

UP_UCG
V [V]
Time [ms]
UP_UCG = 0
UP_UCG = 3 (UC_POL = 0)
UP_UCG = 3 (UC_POL = 1)


LO_UCG
V [V]
Time [ms]
LO_UCG = 0
LO_UCG = 3 (UC_POL = 0)
LO_UCG = 3 (UC_POL = 1)

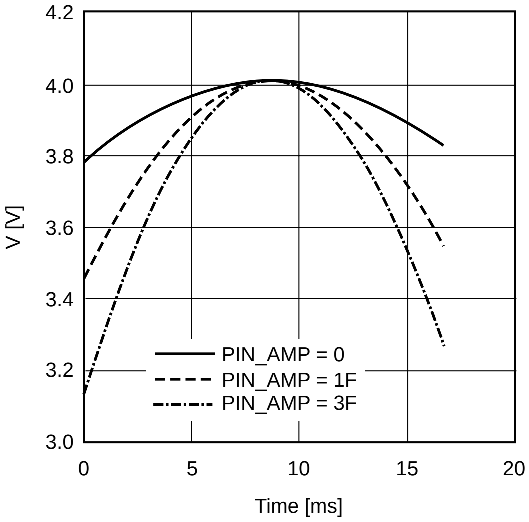
UP_UCP



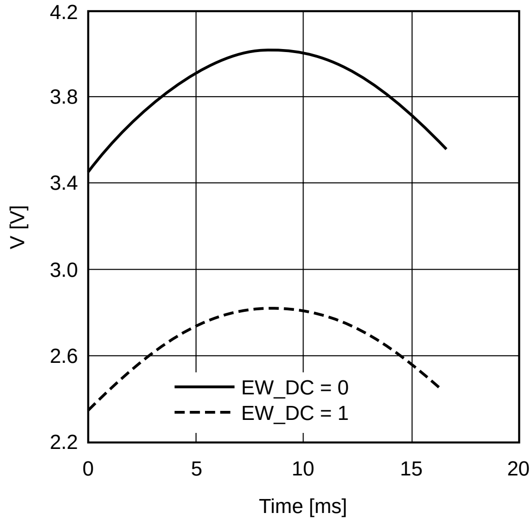
LO_UCP



PIN_AMP

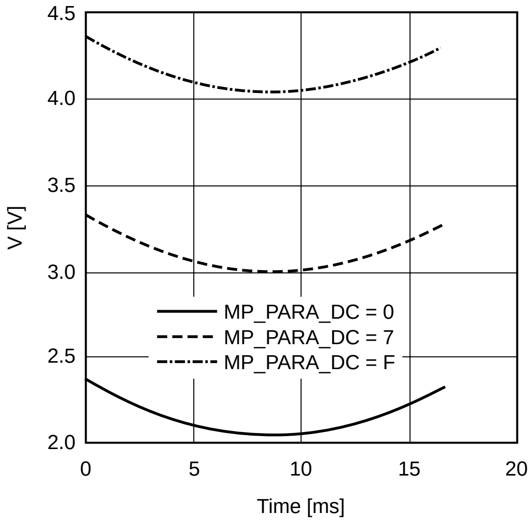


EW_DC

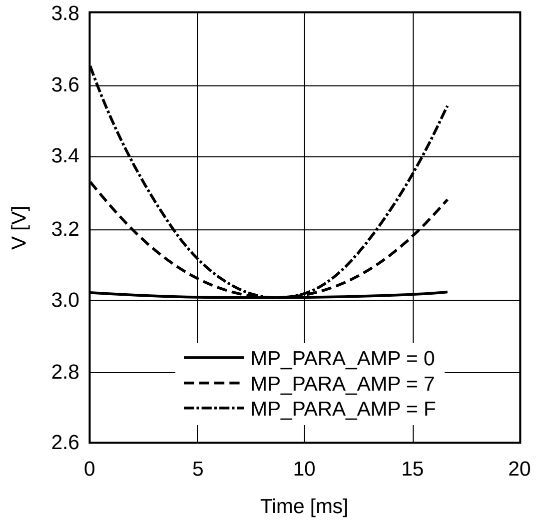


4) MP_PARA, HC_PARA, DF_PARA

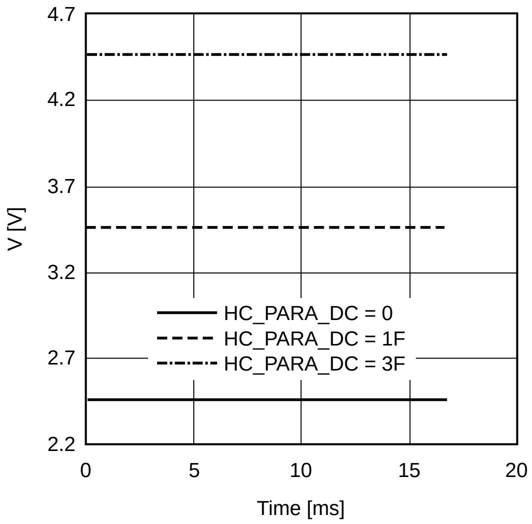
MP_PARA_DC



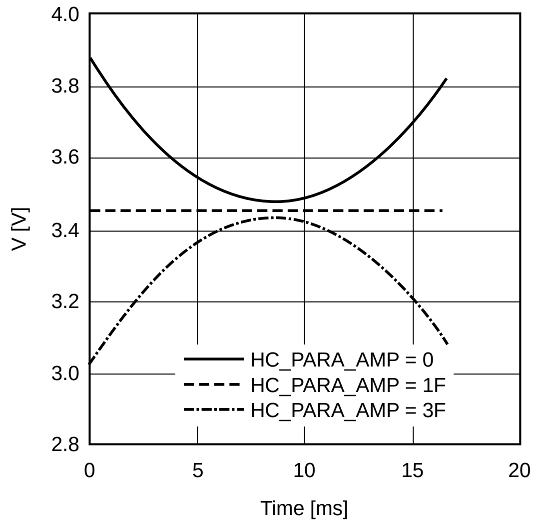
MP_PARA_AMP



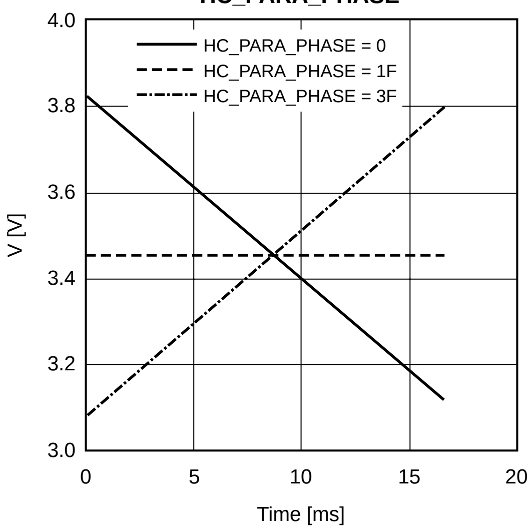
HC_PARA_DC



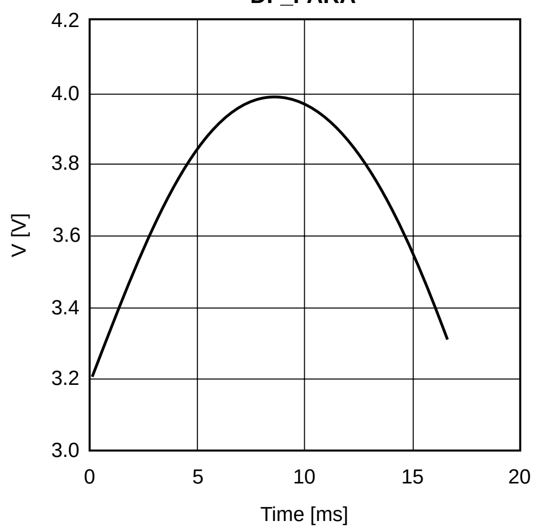
HC_PARA_AMP



HC_PARA_PHASE

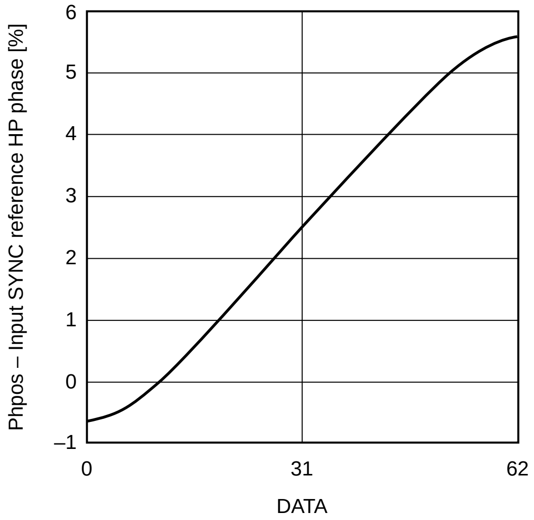


DF_PARA

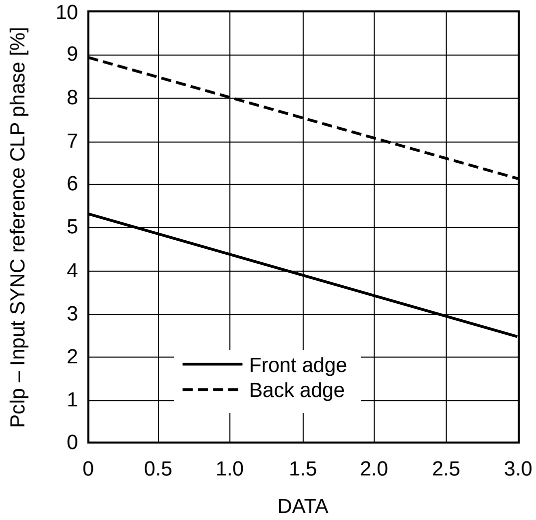


5) HP_IN, SCP

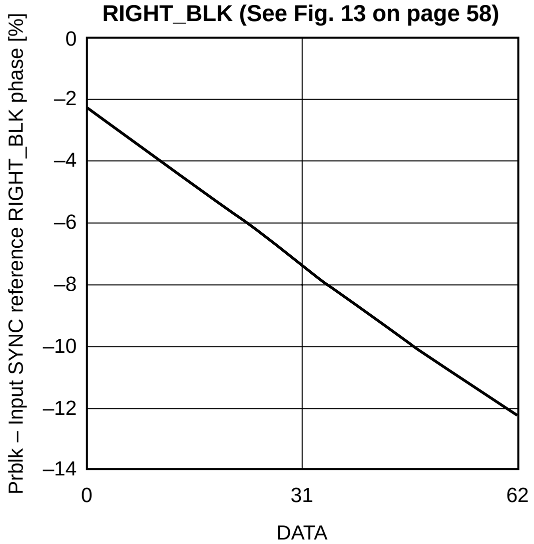
H_POSITION (See Fig. 13 on page 58)



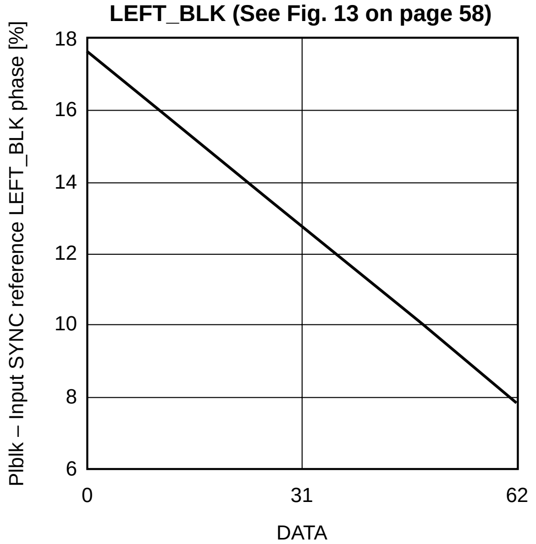
CLP_PHASE (See Fig. 13 on page 58)



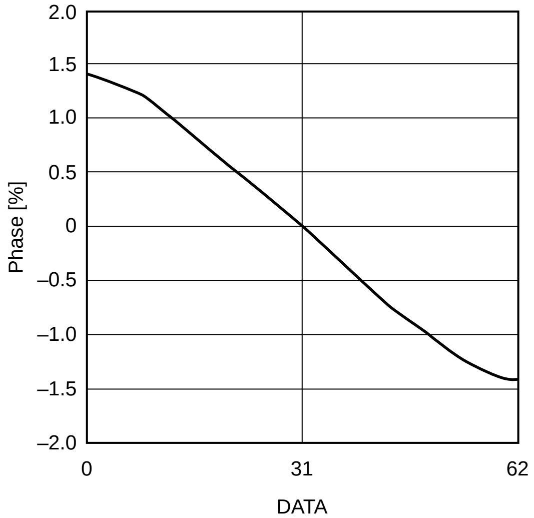
RIGHT_BLK (See Fig. 13 on page 58)



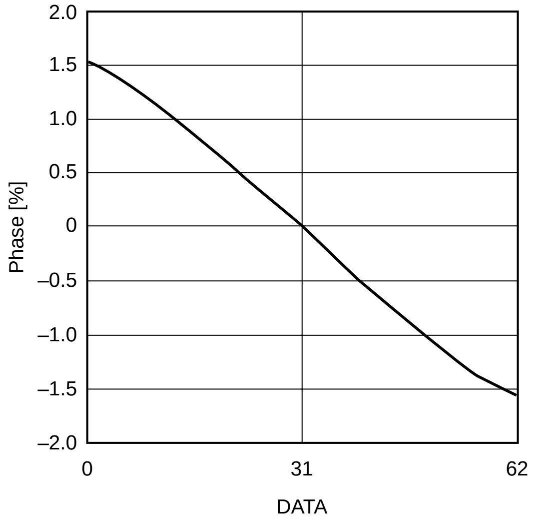
LEFT_BLK (See Fig. 13 on page 58)



AFC_ANGLE

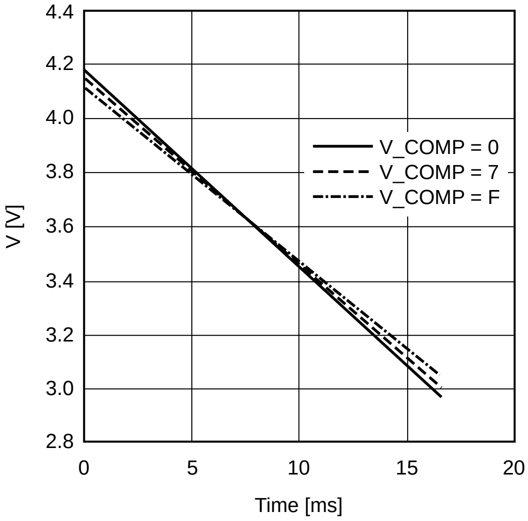


AFC_BOW

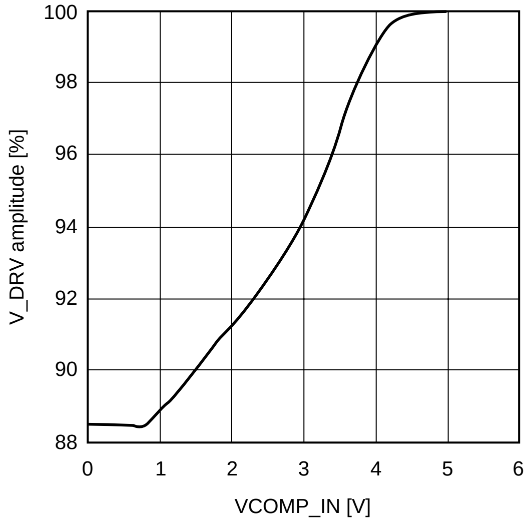


6) High Voltage Compensation

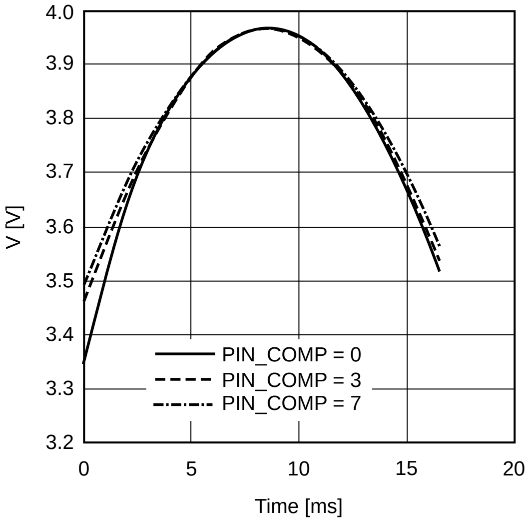
V_COMP (V_COMPIN = 0V)



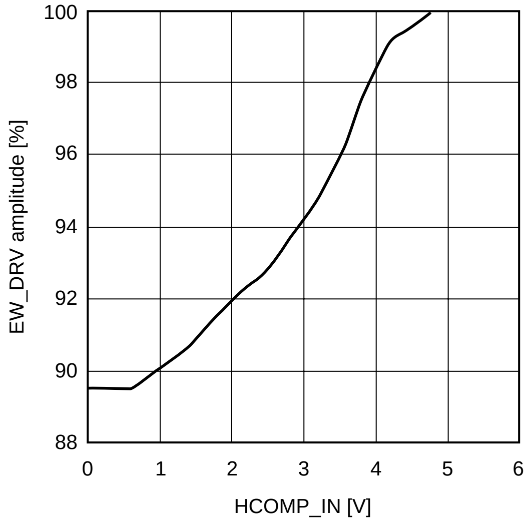
V_COMP



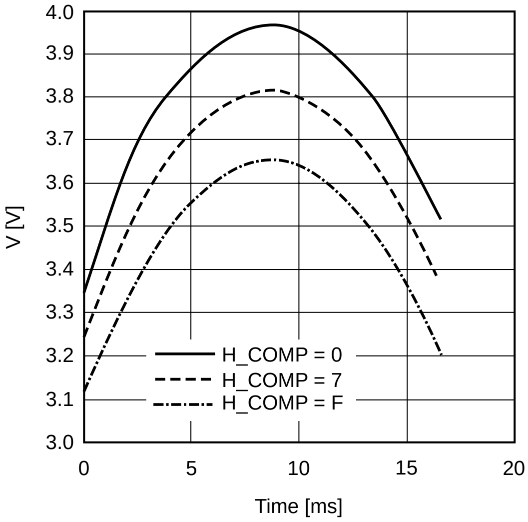
PIN_COMP (H_COMPIN = 0V)



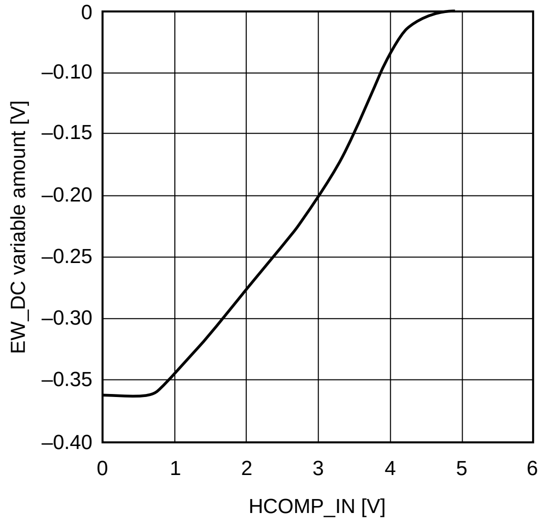
PINCOMP

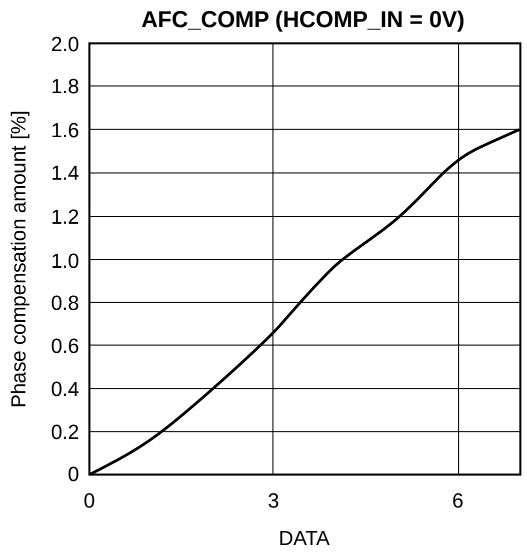


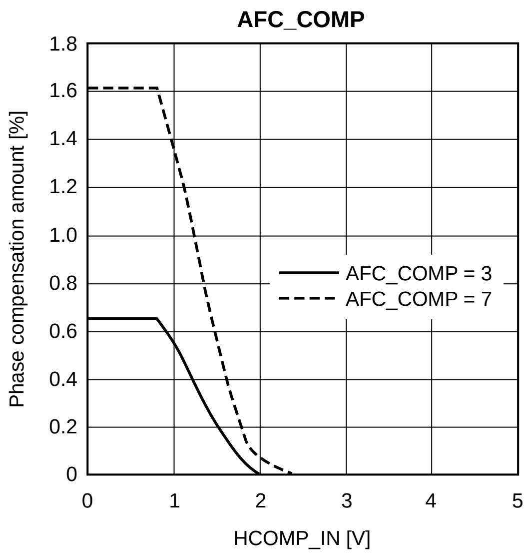
H_COMP (H_COMPIN = 0V)



H_COMP

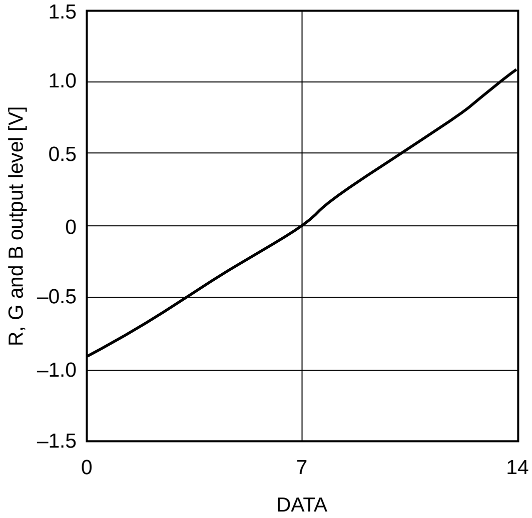



AFC_COMP (HCOMP_IN = 0V)
Phase compensation amount [%]
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0
3
6
DATA

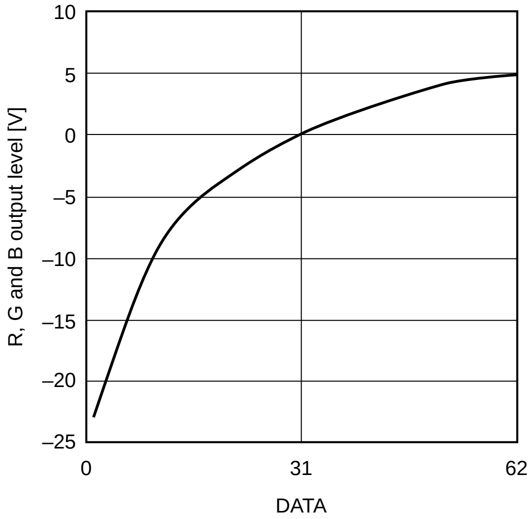

AFC_COMP
Phase compensation amount [%]
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0
1
2
3
4
5
HCOMP_IN [V]
AFC_COMP = 3
AFC_COMP = 7

7) Signal System

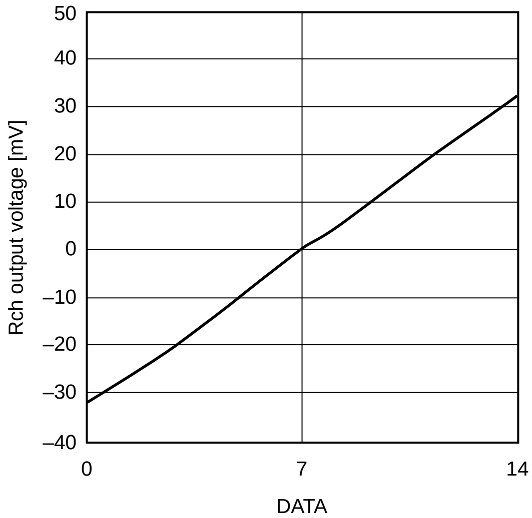
SUB_CONT



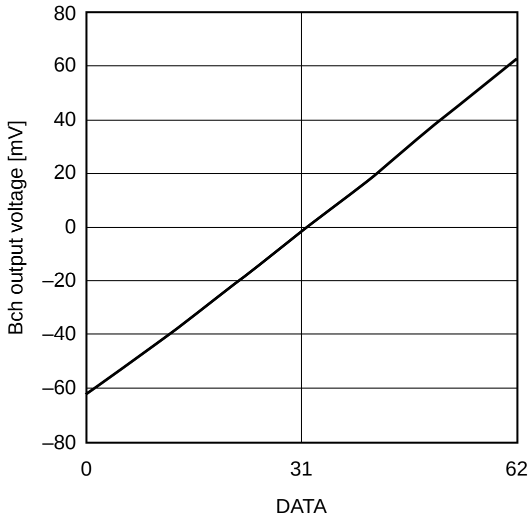
COLOR



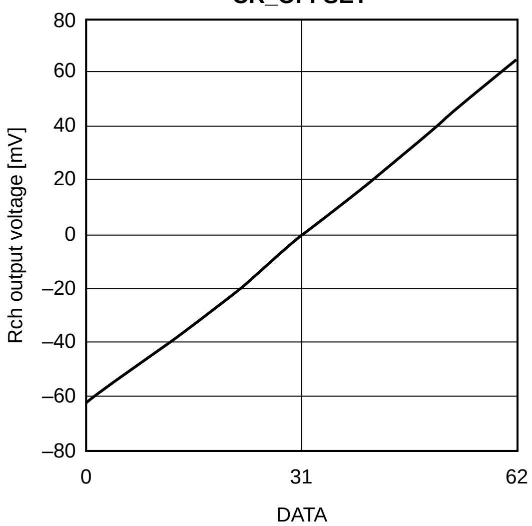
Y_OFFSET



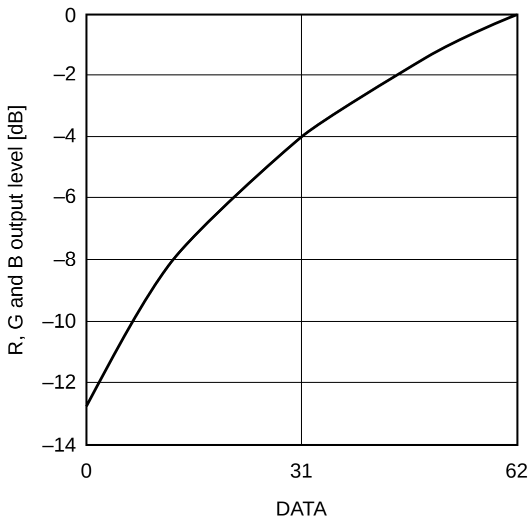
CB_OFFSET

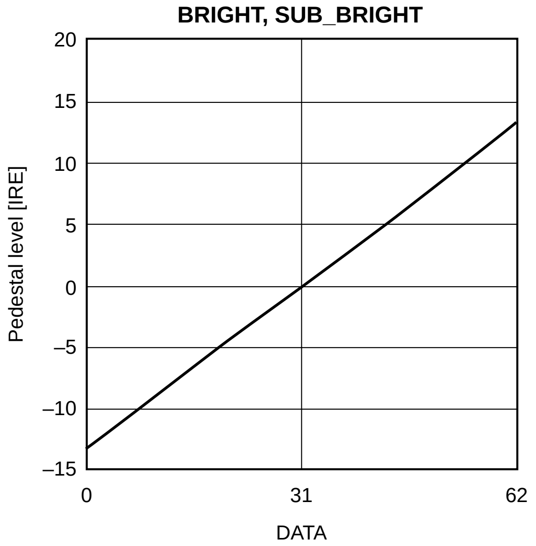


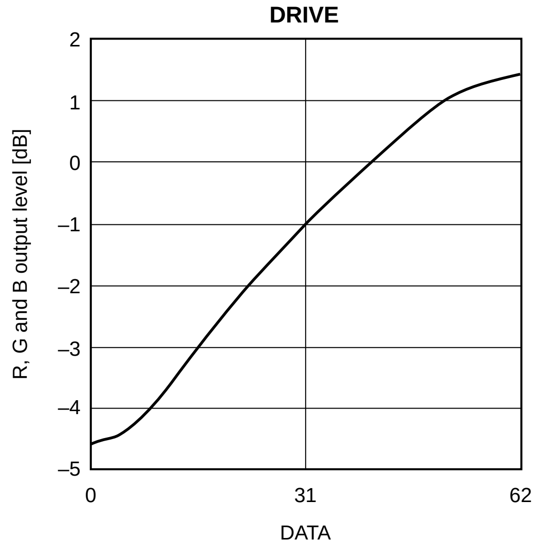
CR_OFFSET

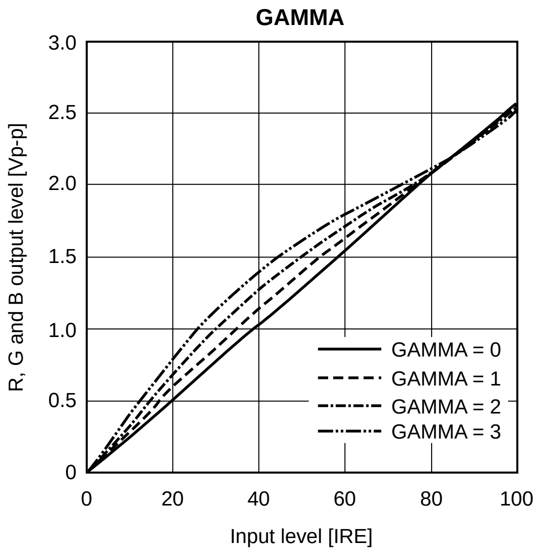


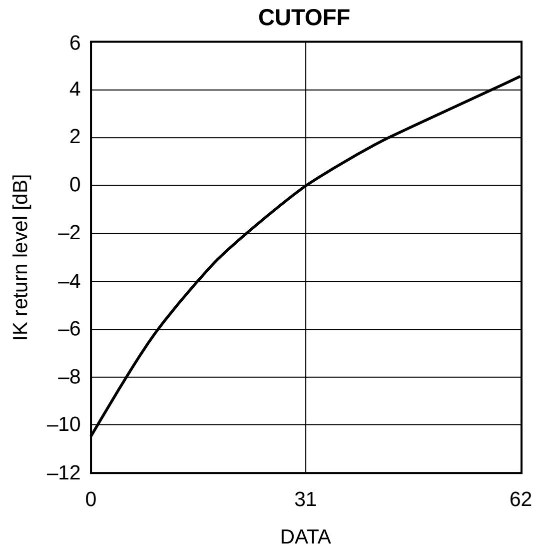
PICTURE

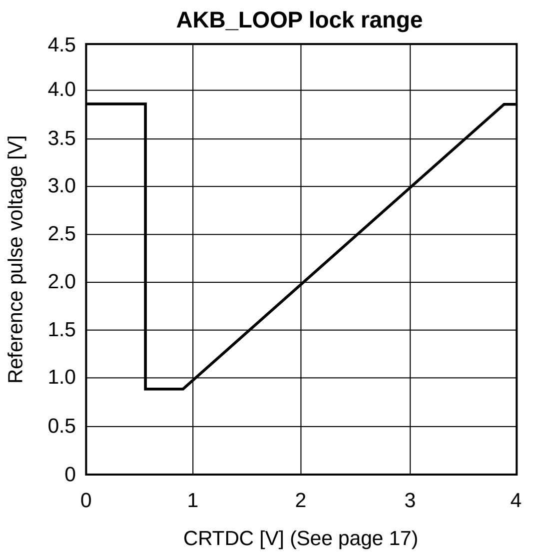


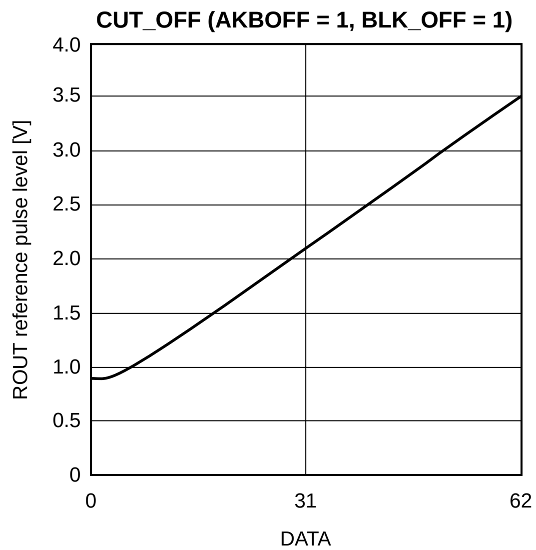

BRIGHT, SUB_BRIGHT
Pedestal level [IRE]
20
15
10
5
0
–5
–10
–15
0
31
62
DATA


DRIVE
R, G and B output level [dB]
2
1
0
–1
–2
–3
–4
–5
0
31
62
DATA

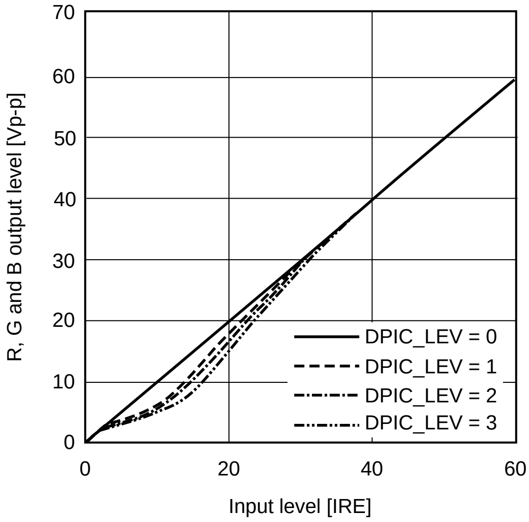

GAMMA
R, G and B output level [Vp-p]
3.0
2.5
2.0
1.5
1.0
0.5
0
0
20
40
60
80
100
Input level [IRE]
GAMMA = 0
GAMMA = 1
GAMMA = 2
GAMMA = 3


CUTOFF
IK return level [dB]
6
4
2
0
–2
–4
–6
–8
–10
–12
0
31
62
DATA

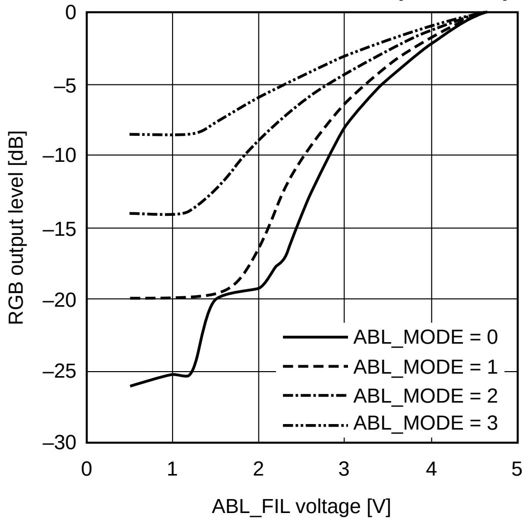

AKB_LOOP lock range
Reference pulse voltage [V]
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
0
1
2
3
4
CRTDC [V] (See page 17)


CUT_OFF (AKBOFF = 1, BLK_OFF = 1)
ROUT reference pulse level [V]
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
0
31
62
DATA

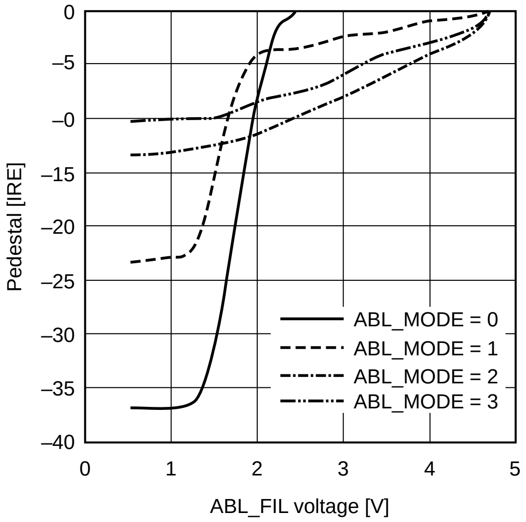
DPIC_LEV



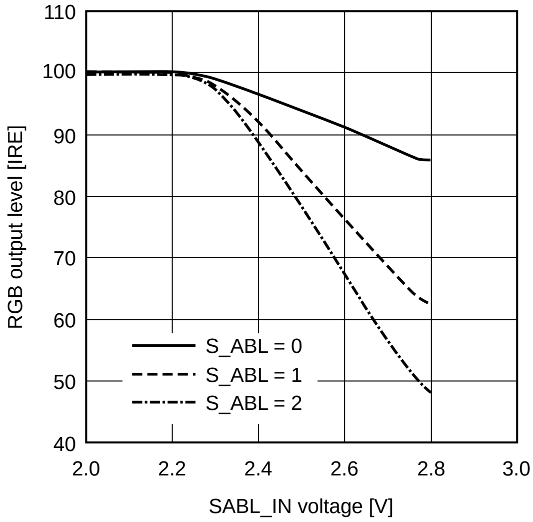
ABL_MODE Characteristics (PICTURE)



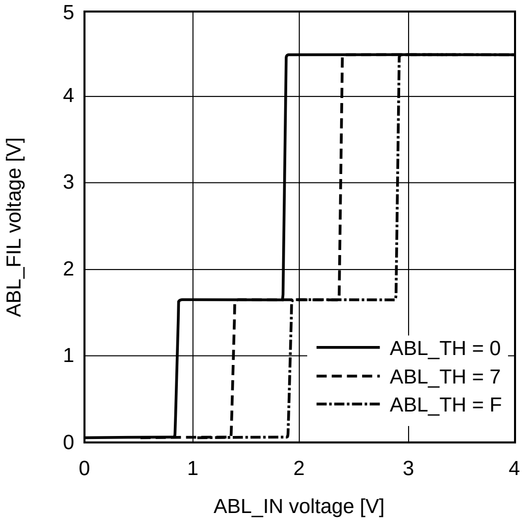
ABL_MODE Characteristics (BRIGHT)



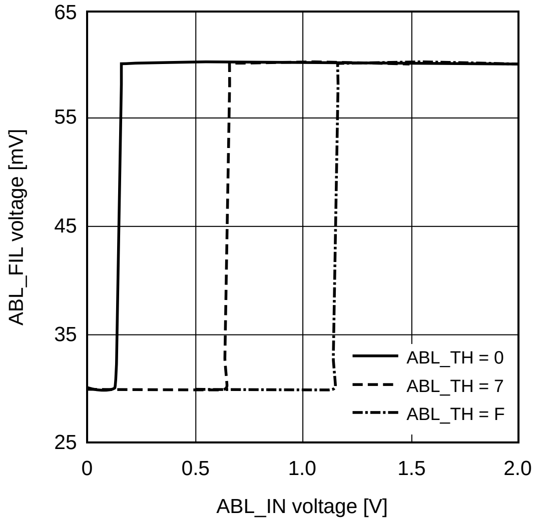
S_ABL



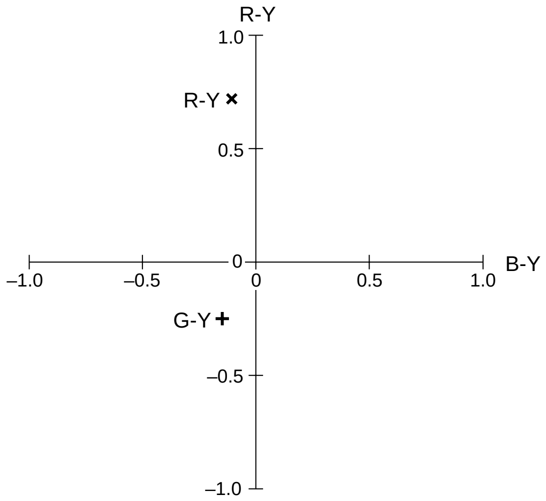
ABL_TH (Threshold in quick charge and normal charge)



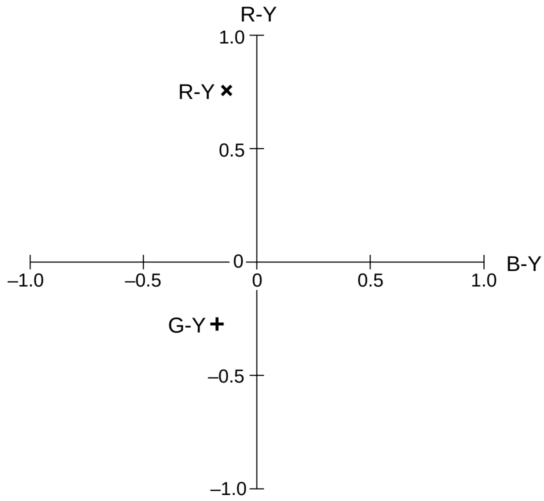
ABL_TH (Threshold in quick discharge)



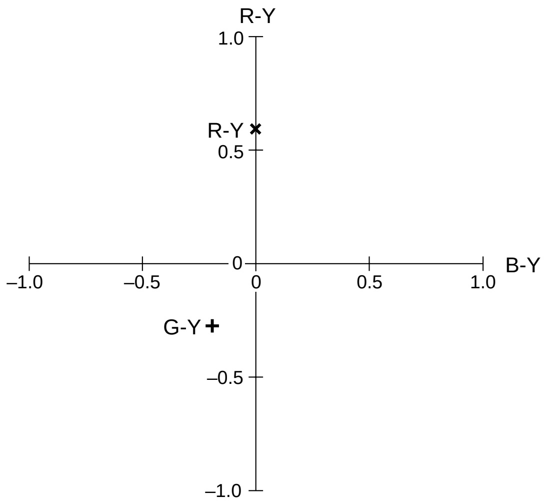
COL_AXIS = 3 (NTSC JAPAN)



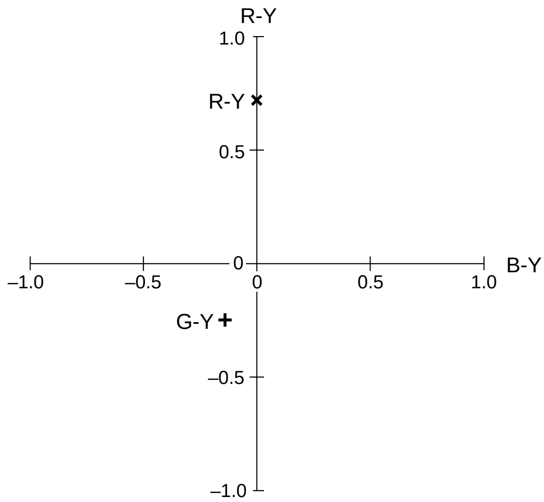
COL_AXIS = 2 (NTSC US)



COL_AXIS = 1 (PAL/SECAM)



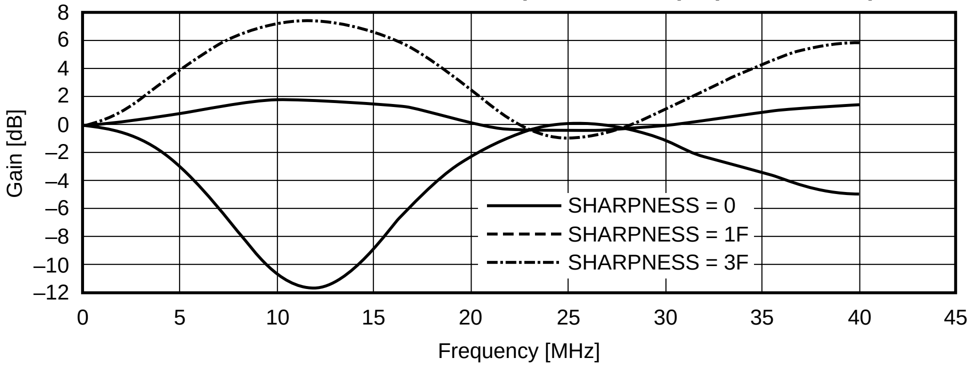
COL_AXIS = 0 (NTSC Projecter)



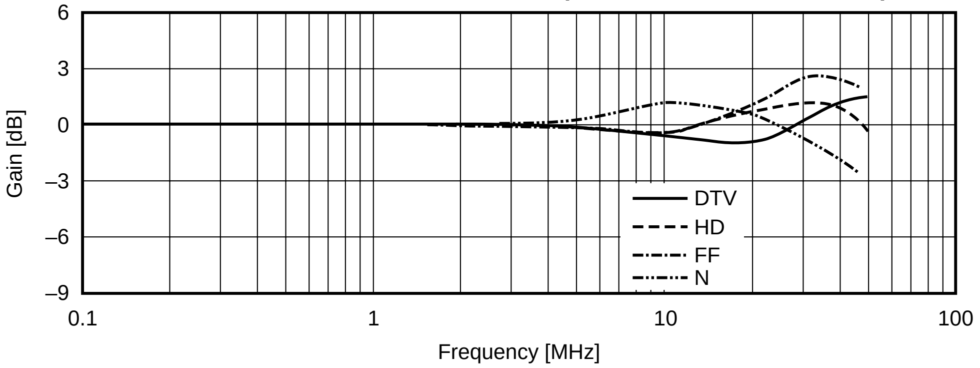
Detection Axis Adjustment

8) Frequency Response

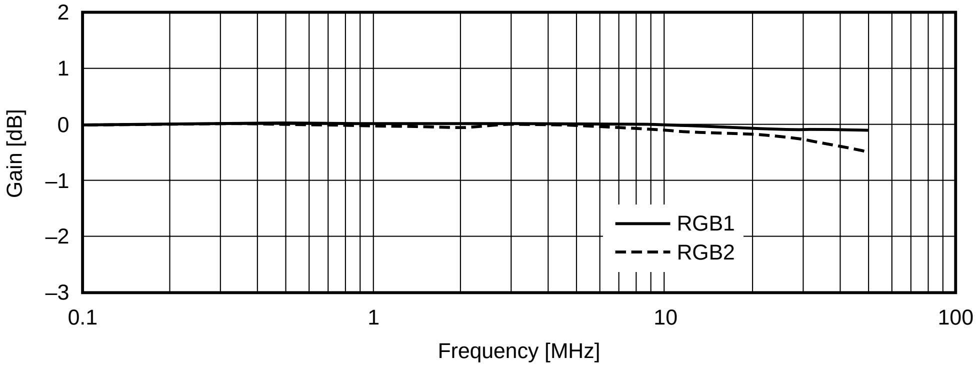
YIN → RGB_OUT SHARPNESS (SYSTEM = 2 (HD), SHP_F0 = 0)



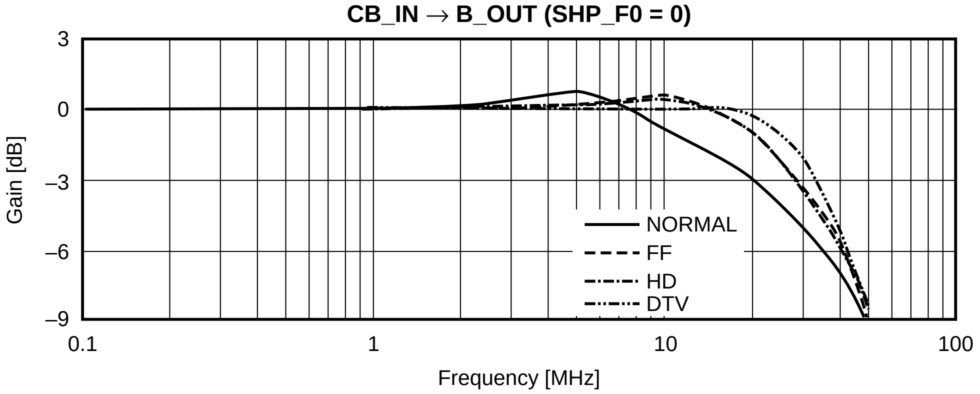
YIN → RGB_OUT SHARPNESS OFF (YF_OFF = 1.5V, SHP_F0 = 0)



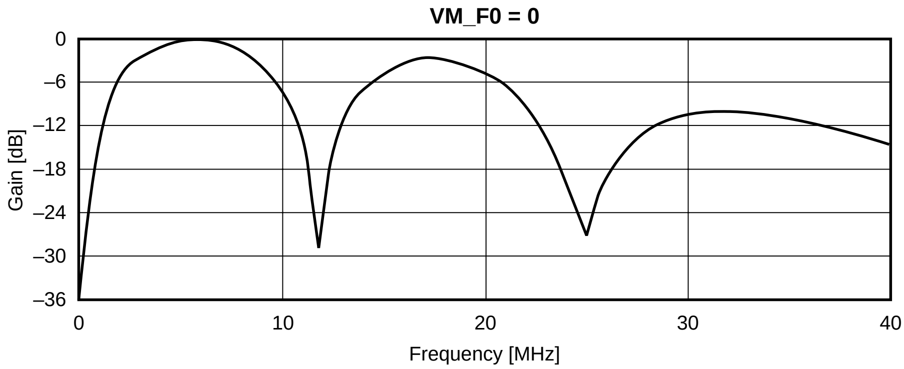
RGB1, 2_IN → RGB_OUT

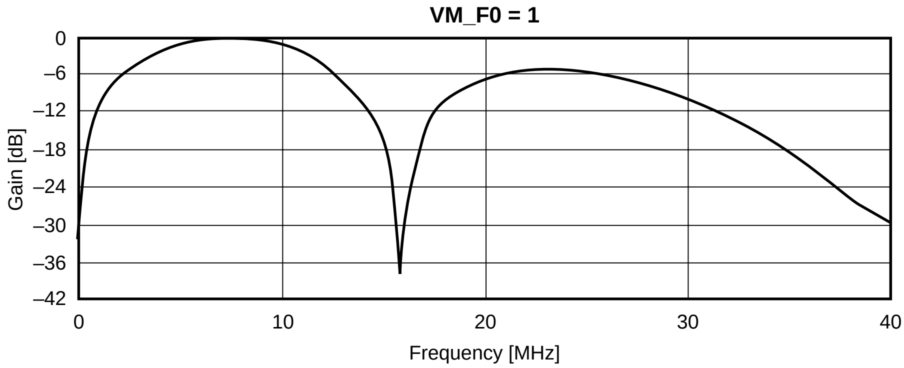


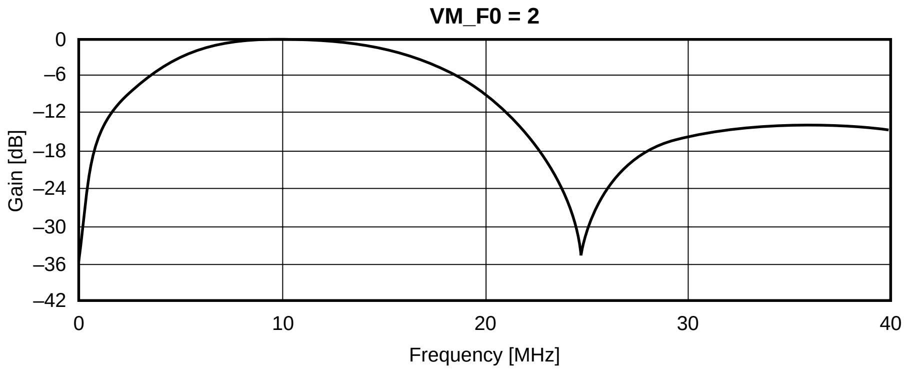
CB_IN → B_OUT (SHP_F0 = 0)

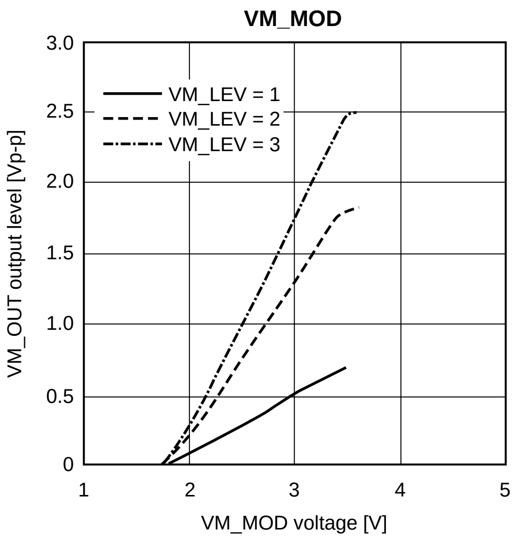


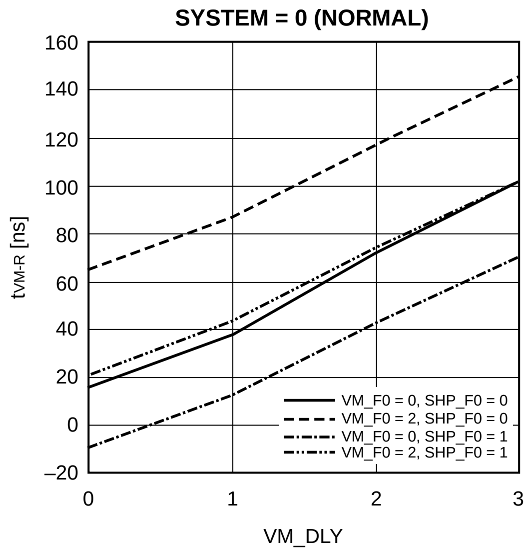
9) VM_OUT Characteristics (SYSTEM = 2, SHP_F0 = 0)

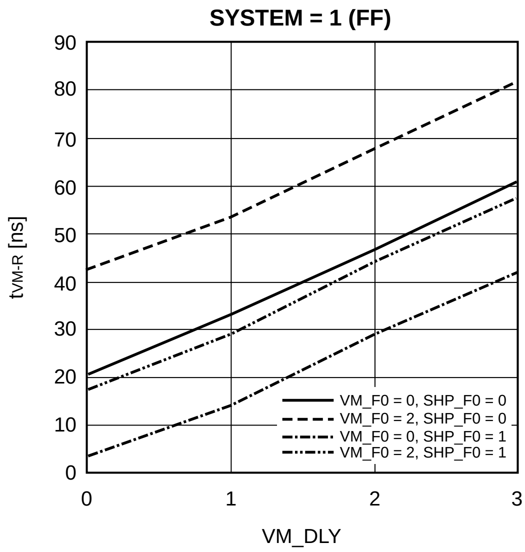


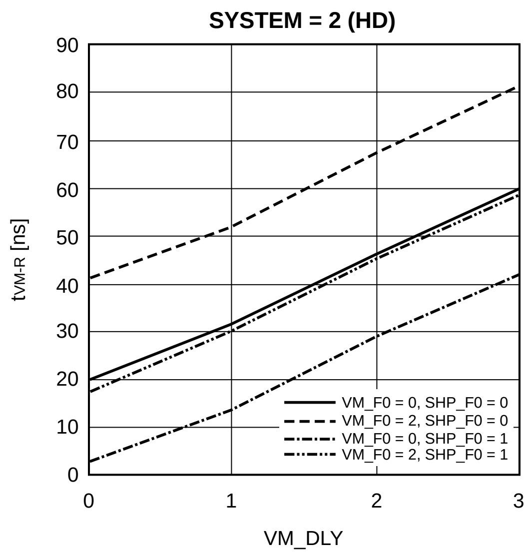


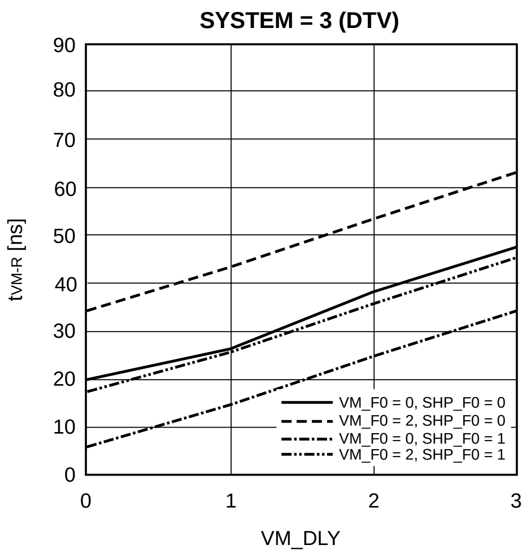


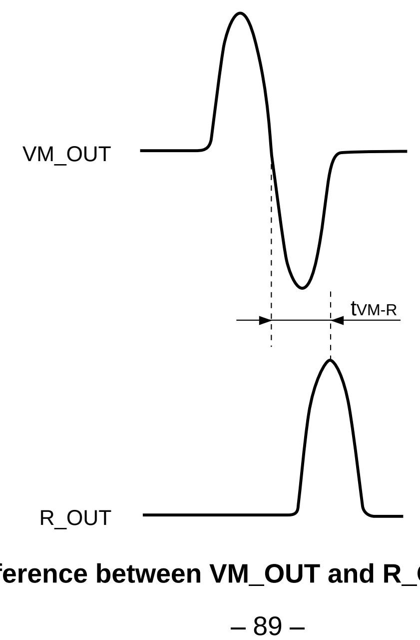








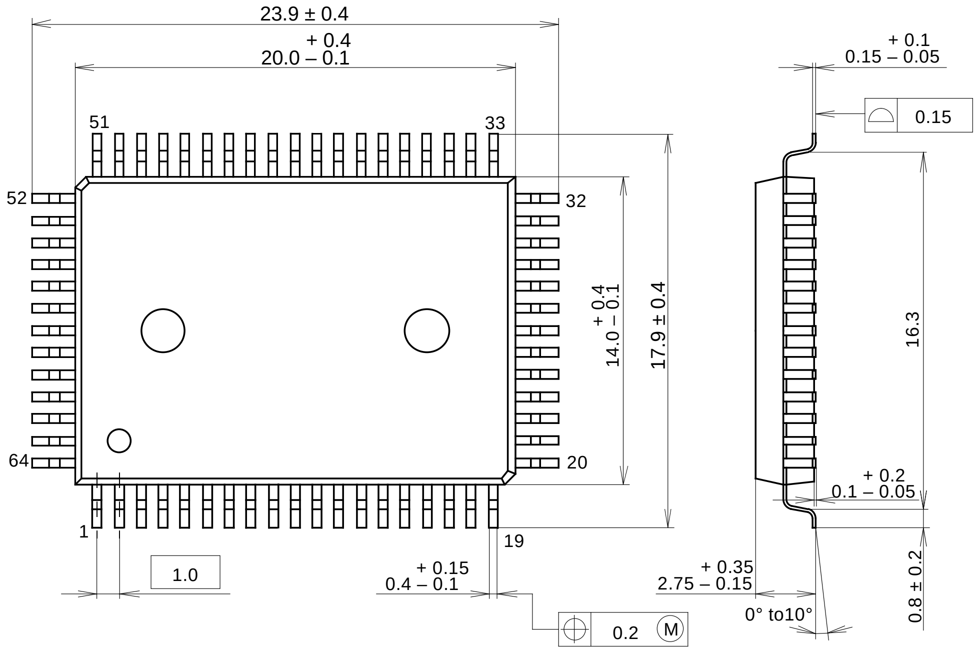




Y_IN: Phase Difference between VM_OUT and R_OUT when T-pulse Inputs

Package Outline Unit: mm

64PIN QFP(PLASTIC)



SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	——

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).