TVPO 2066
TV Controller
with On-Screen Display
for TV Receivers

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Contents

TV–Controller with Integrated On–Screen Display Ability

1. Introduction

In comparison to the older TVPO 2065 hardware, the port 3 of the TVPO 2066 consists of 6 x 12 V/2 mA open–drain outputs instead of 5 V/25 mA open–drain outputs.

“TVPO 2066” is the name of the unprogrammed hardware. The programmed versions will be called:

– TVPO 2066–Axx for analog TV–sets

– TVPO 2066–Dxx for digital TV–sets

with the version–no. xx. Application diagrams and descriptions of different software versions are available in additional data sheets.

The TVPO 2066 is an intelligent microcomputer in N–channel MOS technology. On one silicon chip, it contains all operating and tuning functions of a modern TV receiver. Thus, along with the non–volatile memory (MDA 2062, NVM 3060), the SAA 1250, IRT 1250 or IRT 1260 remote–control transmitter and the TBA 2800 preamplifier this offers a very economic solution for TV receivers with on–screen display and voltage synthesizer.

The device is available in 44–pin PLCC package and 40–pin DIL package. The PLCC version has 4 pins more for digital combined inputs/outputs.

2. The Functional Blocks of the TVPO 2066

The hardware components of the TVPO 2066 are:

– 8048–core, fully compatible to 8048 instruction set

– 10K ROM, 256 byte RAM

– four 64 steps analog output to control vol., color etc.

– single 4032 steps analog output for controlling of a VS–tuner

– IR decoder for ITT–IR (remote control with IRT 1250/60)

– mains flip–flop for standby mode

– IM–bus interface for non–volatile memory and devices of DIGIT 2000 system for digital video–processing.

– fast counter input (T1) for automatic search (for analog TV–sets)

– 12 digital combined inputs/outputs (8 or 10 for DIL–package)

– 8 digital outputs

– integrated 12–digit on–screen display

2.1. The 8049 Microcomputer

For the description of the commands and characteristics of the 8049, please refer to the CCU 2030, CCU 2050, CCU 2070 data sheet.

The 8049 provides separate address space for program, data, in/out, and external data. The ROM is organized in banks of 2 K Bytes. Bank 0 occupies the addresses 0 to 2047. The other banks (10, 11, 12, 13) share the addresses 2048 to 4095. The different banks are selected through the bank select register 15 as described for the CCU 2070 in the CCU 2030, 2050, 2070 data sheet. Banks 14 through 17 of the CCU 2070 are not available in the TVPO.

The data and control registers of the TVPO’s peripheral units are located in the address space of external data.

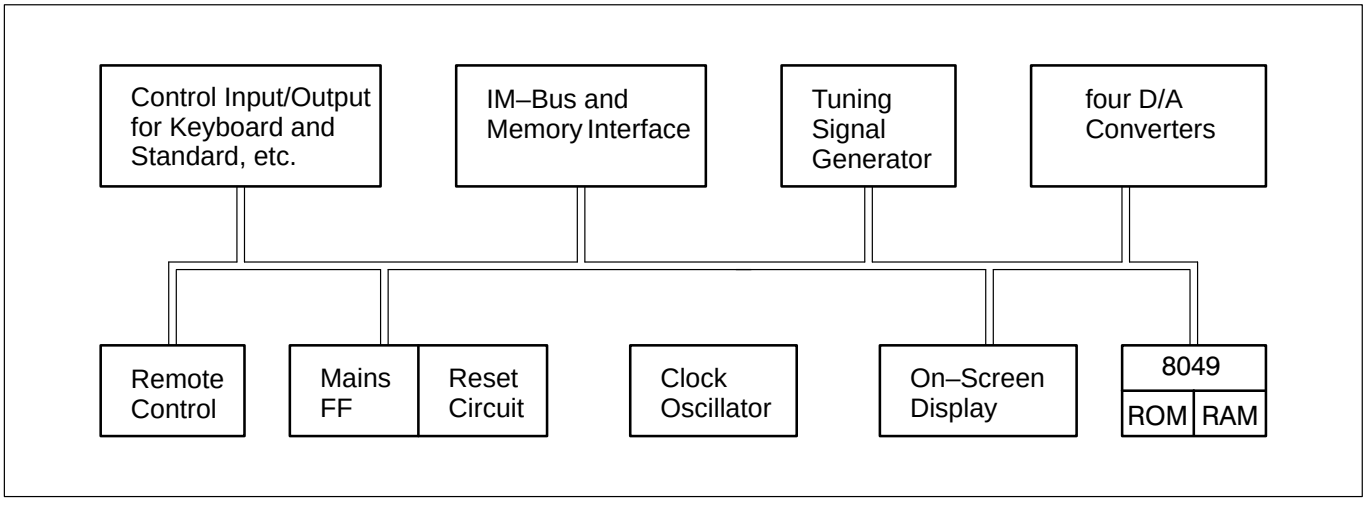


Fig. 1–1: Functional block diagram of the TVPO 2066

They are accessed by the “Move External” instruction (MOVX). Electrically, the connection is provided by the lines DB_0 to DB_7, $\overline{RD}$, $\overline{WR}$, and ALE. These connections of the 8049 microcomputer are not available during normal operation. In “Test Mode” (EA = 5 V or EA = 12 V), some pins are switched so that the TVPO’s peripherals can be accessed from the outside via DB_0 to DB_7.

In normal operation, only P2 of the 8049’s original ports remains unchanged. During test operation, $\overline{RD}$, $\overline{WR}$, ALE and $\overline{PSEN}$ are connected to $P2_4$ to $P2_7$ (compare CCU 2030, CCU 2050, CCU 2070 data sheet).

2.2. The Remote–Control Decoder

In the already mentioned standby mode, and also during normal operation, the remote–control decoder expects infrared–transmitted signals that were transmitted by the SAA 1250, IRT 1250 or IRT 1260 remote–control transmitter IC, received by an infrared photo diode, and amplified by the TBA 2800 infrared preamplifier IC. The decoder frees the remote–control signal from interference and decodes each command word that is recognized as correct. A valid command word is made available to the microcomputer by way of two registers. No interrupt is initiated. Rather, it is the task of the program to continuously check the infrared registers.

A command word transmitted via infrared consists of 10 bits – four address bits and six data bits. These two parts of the command word are provided in two different registers. Bit 7 in the address register is low when a valid command word is detected. When the data word is read, both infrared registers are cleared.

It is possible to mask–program which infrared commands also carry the power–on information and switch the TVPO from standby to full operation. For this purpose, up to five groups of commands within a binary decoder matrix are programmable for one infrared address (compare CCU 2030, CCU 2050, CCU 2070 data sheet).

2.3. The Mains Flip–Flop and Reset Circuit

Mains flip–flop and reset circuit operate from the standby supply. After switching on the standby supply it takes 100 ms at most until the TVPO is in full standby operation. The $\overline{Mains}$ output is controlled by the mains flip–flop. In the
“Mains off” position the output is high.

The mains flip–flop is set by means of the infrared “Mains on” commands or by an active low level applied to the $\overline{Mains}$ output for at least 20 µs. A reset for the mains flip–flop is generated whenever:

1. The standby supply voltage is less than approx. 3.5 V (e.g. during power–on)
2. The microcomputer executes a “Mains off” command.

The microcomputer clears the mains flip–flop by writing a 1 into bit 3 of the external register 13. In order to properly charge the stray capacitances at the $\overline{Mains}$ output, the mains flip–flop remains blocked in the “Mains off” position for 16 ms after any reset. After this time has elapsed, the TV set may be turned on again.

With no Reset option set (compare CCU 2030, CCU 2050, CCU 2070 data sheet), the mains flip–flop is also reset by any $\overline{Reset}$ signal going low. The TVPO–internal $\overline{Reset'}$, which is different from the externally–applied $\overline{Reset}$ is high only when both $\overline{Mains}$ is in the low state and $\overline{Reset}$ is at high level. Two options are mask–programmable in this respect:

Reset 1: The $\overline{Reset}$ signal, going low, does not reset the mains flip–flop. If the customer does not specify, this option will be set as default.

Reset 2: The TVPO–internal $\overline{Reset'}$ is identical to the $\overline{Reset}$ signal and independent of the state of the mains flip–flop.

Resetting the mains flip–flop clears the remote–control decoder. The other parts of the TVPO are cleared by the TVPO–internal $\overline{Reset'}$ signal via the $\overline{Reset}$ input. Delaying the $\overline{Reset}$ signal with respect to the V_{DD} supply voltage is done by an external RC network at the $\overline{Reset}$ input.

The input voltage of the regulator for the 5 V V_{DD} supply voltage should be monitored to prevent the system’s circuits from resetting improperly and the NVM 3060 EEPROM from programming false data.

With no Reset option set, any spike or excessive noise present on the $\overline{Reset}$ line may cause the mains flip–flop to be reset. In such cases, a ceramic filter capacitor should be provided near the $\overline{Reset}$ pin.

2.4. The IM–Bus and Non–Volatile–Memory

It is by means of this part of the circuit that the TVPO 2066 communicates with the non–volatile memory (MDA 2062 or NVM 3060) which stores the tuning and analog data, acquired during the Memo procedure and the options. The IM–Bus consists of three lines Clock, Ident and Data. Clock and Ident are unidirectional signals from the TVPO 2066 to the memory (and to the VSP–processor in case of a digital TV set), and Data is bidirectional for transferring the data in both directions. In addition, the MDA 2062 (not the NVM 3060) requires a memory clock signal which is issued from the TVPO 2066 (approx. 1 kHz). All these signals on the IM–Bus have TTL level. In the nonoperative state all three bus lines are high. The start of a telegram is initiated when Ident and Data are low. Data takeover occurs at the positive edge of Clock. For a detailed description of the IM–Bus protocol please refer to the data sheet of the MDA 2062 or NVM 3060.

2.5. The Clock Generator and the Sequence Control

For the purpose of generating the clock signals required to operate the TVPO 2066 the chip contains an oscillator which is designed for crystals in the frequency range from 3.5 to 4.5 MHz. For the exact requirement of “off–timer” and “sleep–timer” functions, a 4 MHz crystal is needed. The crystal is connected to the ‘Xtal’ input. All timing specification in this data sheet relate to a crystal frequency of 4 MHz. With other crystal frequencies, there will be corresponding variations.

2.6. The D/A Converters for the Analog Outputs

The TVPO 2066 provides four analog outputs for adjustment of the TV’s basic settings (e.g. volume and for analog TV sets additional brightness, contrast and color saturation). These control voltages are made available as pulse/pause modulated signals, where the ratio can be varied in 64 steps. The needed DC level signal is obtained by means of a simple RC lowpass filter.

2.7. The Tuning Voltage Generator

The tuning voltage for the capacitance diodes of the TV tuner is generated as a pulse/interval modulated signal by a modified rate multiplier. The range of variation of the pulse/interval ratio extends from 0 (no pulses) to infinity (continuous signal) with a resolution of 4032 steps. At a clock frequency of 4 MHz the basic period of the rate multiplier is 0.5 ms which results in tolerable filter expenditure.

2.8. The Ports

The TVPO 2066 has two ports (Port 2 and Port 3) which are used by the software versions as control outputs/inputs for a keyboard, band selection, multi–standard indicators, multi–video indicators and AFC switch.

The PLCC version of the TVPO 2066 has in addition four pins of Port 1 (P14...P17). The DIL version of the TVPO 2066 is also available in other pinnings: the D/A converter DA3 and DA4 can be exchanged to port input/outputs. DA3 to Port 1, Bit 5 (P15) and DA4 to Port 1, Bit 6 (P16). This possibility is very useful in digital TV sets, because in this case only one D/A converter is needed for volume control.

2.9. The On–Screen Display

2.9.1. Outputs and Inputs for the OSD

The OSD is an additional hardware module on the TVPO 2066 chip, which allows the display of 12 different characters such as the program number and analog values (volume, brightness etc.) on a TV screen. The TVPO 2066 software controls the OSD through a set of 16 external write registers.

The TVPO 2066 delivers four additional output signals:

– R_out	character signal red	(1 Vpp)
– G_out	character signal green	(1 Vpp)
– B_out	character signal blue	(1 Vpp)
– FB_out	fast blanking	(TTL level)

Fast blanking is used for switching between video and OSD signals and shows the validity of the R, G, B outputs.

For synchronization and to place the display, the TVPO 2066 needs two additional input signals:

– H_in	horizontal synchronization	(TTL level)
– V_in	vertical synchronization	(TTL level)

2.9.2. Display Format

The OSD generates a rectangular display block, which contains 2 rows of 6 characters each (see Fig. 2–1). The characters are addressed depending on their position within this display block. Each address is attached to one TVPO 2066 register. The content of each register describes the character type and its color.

0	1	2	3	4	5	(Hex)
0000	0001	0010	0011	0100	0101	(Bin)
8	9	A	B	C	D	(Hex)
1000	1001	1010	1011	1100	1101	(Bin)

Fig. 2–1: On–Screen Display Block

A character is displayed in 5 x 7 dot matrix format, which is stored in the character ROM. The size of one dot can be programmed to 4 different values (size = 1, 2, 3, 4).

– character format	= 5 x 7 dot
– dot format vertical	= 2 lines x size
– dot format horizontal	= 2 x T0 x size

T0 is the duration of one clock period of the system clock (CLK = 4 MHz → T0 = 0.25 ns).

To make the characters easier to see without increasing the storage requirement, a smoothing algorithm is implemented. The space between two diagonal dots is filled with one pixel. Thus the character appears in a 10 x 14 matrix format.

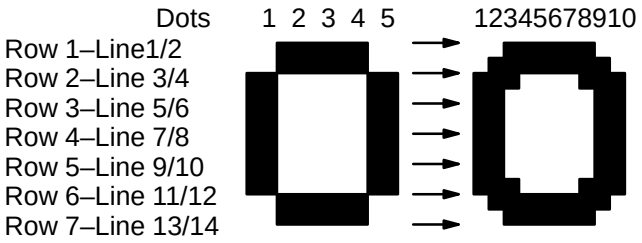


Fig. 2–2: Character smoothing

– pixel format vertical = 1 line x size

– pixel format horizontal = T0 x size

The horizontal space between two characters is 1 dot, the vertical space is 2 dots. A fringe of 1 dot lies around the 12 characters. The overall size of the display block is:

– block format vertical = 18 dot

– block format horizontal = 37 dot

The start position of the display's left, upper corner on the TV screen is specified by two registers and can be programmed in steps of 18 video lines, respectively 12 clock periods.

– start position vertical = 18 lines x Vpos

– start position horizontal = 12 x T0 x Hpos

2.9.3. Display Control

The interface between TVPO 2066 and OSD consists of 16 external write registers in which the TVPO 2066 software can store the structure, size and position of the display (see also Table 3–1).

There are 32 different character types (C4...C0) in 8 colors (R, G, B) available. One special character is the 'display off code'. In this case the display is switched off for one character. The remaining 31 codes are used as address for the character ROM which stores 31 characters represented in a 5 x 7 matrix format.

It is possible to use 3 kinds of background modes.

1. No Background
   Only the character itself is laid over the TV picture on those points where the character matrix are set. A blank character for instance is not visible.
2. Square Background
   The whole display block is visible in the desired background color. The characters differ from the background by use of another color. Only the 'display off code' switches off the background at the concerning character position.
3. Fringe Background
   This function creates a fringe of one pixel around and inside of each character. The color of the fringe is programmable. Only this fringe and the character itself is laid over the TV picture.

The display control bits are explained in the next chapter.

3. Description of Hardware Component Registers

Table 3–1: Registers of hardware components (x='0' or '1')

Register Address	Register Contents	Format 7	6	5	4	3	2	1	0
1	IR–ADDR.	CR	0	0	0	A3	A2	A1	A0
2	IR–COMM.	0	0	C5	C4	C3	C2	C1	C0
3	PORT3	B7	B6	B5	B4	B3	B2	B1	B0
7	IMB–ADDR.	A7	A6	A5	A4	A3	A2	A1	A0
8	IMB–DATH	B15	B14	B13	B12	B11	B10	B9	B8
9	IMB–DATL	B7	B6	B5	B4	B3	B2	B1	B0
10	IMB–CTRL.	BB	x	x	x	C3	C2	C1	C0
11	TUNE–VL	T3	T2	T1	T0	x	x	x	x
12	TUNE–VH	T11	T10	T9	T8	T7	T6	T5	T4
13	MAINS–FF.	x	x	x	x	MOF	x	x	x
16	DAC 1	x	x	x	B4	B3	B2	B1	B0
17	DAC 2	x	x	x	B4	B3	B2	B1	B0
18	DAC 3	x	x	x	B4	B3	B2	B1	B0
19	DAC 4	x	x	x	B4	B3	B2	B1	B0
32	CHAR 0	R	G	B	C4	C3	C2	C1	C0
33	CHAR 1	R	G	B	C4	C3	C2	C1	C0
34	CHAR 2	R	G	B	C4	C3	C2	C1	C0
35	CHAR 3	R	G	B	C4	C3	C2	C1	C0
36	CHAR 4	R	G	B	C4	C3	C2	C1	C0
37	CHAR 5	R	G	B	C4	C3	C2	C1	C0
38	CHAR 8	R	G	B	C4	C3	C2	C1	C0
39	CHAR 9	R	G	B	C4	C3	C2	C1	C0
40	CHAR A	R	G	B	C4	C3	C2	C1	C0
41	CHAR B	R	G	B	C4	C3	C2	C1	C0
42	CHAR C	R	G	B	C4	C3	C2	C1	C0
43	CHAR D	R	G	B	C4	C3	C2	C1	C0
44	SIZE/Vpos	S1	S0	x	x	V3	V2	V1	V0
45	Hpos	x	x	x	H4	H3	H2	H1	H0
46	Mode	BGR	BGG	BGB	CRF	CR0	SQ	FR	DI
47	Test	RO	GO	BO	FBO	SM	T0	TM	x

3.1. Registers for Infrared Control

Register 1: Infrared Address (READ only)
A0 ...A3: Address

CR : 0 = valid command received
1 = no command received

Register 2: Infrared Command (READ only)
C0...C5: Command

3.2. Register for Port 3

Register 3: Port 3 (WRITE only)
B0...B7 : Set status of port 3, Bit 0...7

3.3. Registers for IM–Bus Control

Register 7: IM–Bus address (WRITE only)
A0...A7 : IM–Bus address 0...255

Register 8: IM–Bus data high (READ/WRITE)
B8...B15: IM–Bus data, bit 8...15

Register 9: IM–Bus data low (READ/WRITE)
B0...B7: IM–Bus data, bit 0...7

Register 10: IM–Bus control (READ/WRITE)
C0...C3: IM–Bus control (READ/WRITE)

C3	C2	C1	C0		
1	1	0	1	Read	8 bit
1	1	1	0	Read	16 bit
1	0	1	1	Write	8 bit
0	1	1	1	Write	16 bit

3.4. Registers for Analog Outputs & MAINS–Control

Register 11: Tuning Voltage (WRITE only)
T0...T3 : LSB's of DAC–Input

Register 12: Tuning Voltage (WRITE only)
T4...T11: MSB's of DAC–Input
DAC worked with binary (dual) code
Range is 0...4031 dec. = 0...FBF hex.

Register 13: Mains Flipflop (WRITE only)
MOF: Mains off

Register 16: Digital/Analog converter Output 1 (WRITE only)
B0...B5: Input of DAC1

Register 17: Digital/Analog converter Output 2 (WRITE only)
B0...B5: Input of DAC2

Register 18: Digital/Analog converter Output 3 (WRITE only)
B0...B5: Input of DAC3

Register 19: Digital/Analog converter Output 4 (WRITE only)
B0...B5: Input DAC4
The DAC's of reg. 16...19 with a polynomial code shown in Table 5–1.

3.5. Registers for On–Screen Display

Register 32...43: C0...C4: Character to be displayed
R, G, B: RGB–color of character to be displayed
Register 32: Character 0 of OSD (WRITE only)
Register 33: Character 1 of OSD (WRITE only)
Register 34: Character 2 of OSD (WRITE only)
Register 35: Character 3 of OSD (WRITE only)
Register 36: Character 4 of OSD (WRITE only)
Register 37: Character 5 of OSD (WRITE only)
Register 38: Character 8 of OSD (WRITE only)
Register 39: Character 9 of OSD (WRITE only)
Register 40: Character A of OSD (WRITE only)
Register 41: Character B of OSD (WRITE only)
Register 42: Character C of OSD (WRITE only)
Register 43: Character D of OSD (WRITE only)

Register 44: OSD size and vertical position (WRITE only)
V0...V3: vertical position
S0...S1: size 1...4

Register 45: OSD horizontal position (WRITE only)
H0...H4: horizontal position

Register 46: OSD Mode (WRITE only)
DI : 0 = OSD off, 1 = OSD on
(set 0 by power–on reset)
SQ, FR: 00 = no background
01 = fringe background
1x = square background
CR0 : 1 = char. code 0 is 1st char.
0 = char. code 0 is blank
CRF : 1 = char. code 1F is 32nd char
0 = char. code 1F is display off
BGx : x = RGB, 1 of 8 background colors

Register 47: OSD Test (WRITE only)
TM : 1 = test mode on
(set 0 by power–on reset)
T0 : 0 = RGB–outp. sync to TVPO clock
1 = RGB–outp. sync to hor. blanking
SM : 1 = Smoothing off
FB0 : 1 = Fast–Blank. output disabled
x0 : x = RGB 1 = RGB output disabled
(all bits are set 0, if TM is set 0)

4. Specifications

4.1. Outline Dimensions

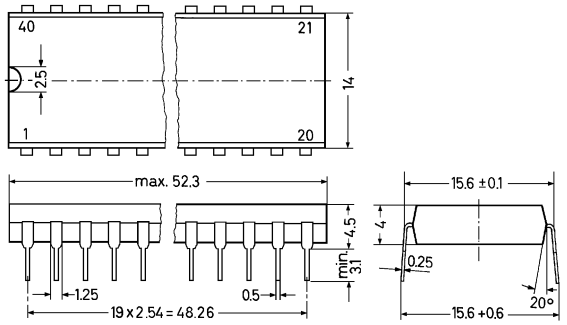


Fig. 4–1: TVPO 2066 in 40–pin DIL Package
20 B 40 according to DIN 41866

Weight approx. 6 g Dimensions in mm

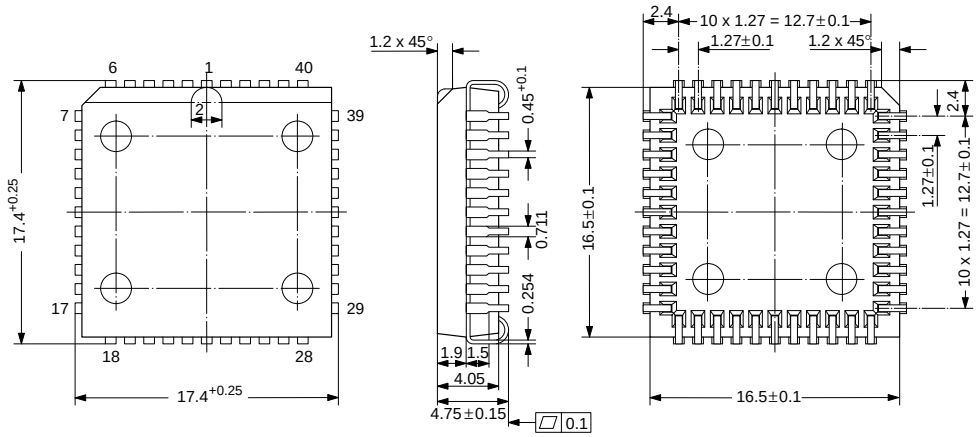


Fig. 4–2: TVPO 2066 in 44–pin PLCC Package
Weight approx. 2.2 g Dimensions in mm

4.2. Pin Connections

4.2.1. 40–Pin DIL Package

1 Vin: Vertical Blanking Pulse Input

2 Hin: Undel. Horizontal Blanking Pulse Input

3 DA3: Analog 3 Output (P15: Port P1, Bit 5)

4 DA4: Analog 4 Output (P16: Port P1, Bit 6)

5 P24: Port P2, Bit 4

6 P25: Port P2, Bit 5

7 P26: Port P2, Bit 6

8 P27: Port P2, Bit 7

9 Vstb: Standby Supply Voltage

10 GND: Ground, 0

11 Vsup: Supply Voltage

12 Xtal: Oscillator Input

13 T1: T1 Input

14 Clck: Memory Clock Output

15 $\overline{\text{Reset}}$: $\overline{\text{Reset}}$ Input

16 $\overline{\text{Mains}}$: $\overline{\text{Mains}}$ Switch Input/Output

17 EA (normally at GND)

18	IMD: IM Bus Data Input/Output
19	IMI: IM Bus Ident Output
20	IMC: IM Bus Clock Output
21	DA1: Analog 1 Output
22	DA2: Analog 2 Output
23	IR: Infrared Remote Control Input
24	VS: Tuning Voltage Output
25	P30: Port P3, Bit 0
26	P31: Port P3, Bit 1
27	P32: Port P3, Bit 2
28	P33: Port P3, Bit 3
29	P34: Port P3, Bit 4
30	P35: Port P3, Bit 5
31	P36: Port P3, Bit 6
32	P37: Port P3, Bit 7
33	P20: Port P2, Bit 0
34	P21: Port P2, Bit 1
35	P22: Port P2, Bit 2
36	P23: Port P2, Bit 3
37	R_out: RED Output
38	G_out: GREEN Output
39	B_out: BLUE Output
40	FB_out: Fast Blanking Pulse Output

4.2.2. 44–Pin PLCC Package

1	Vsup: Supply Voltage
2	GND: Ground, 0
3	Vstb: Standby Supply Voltage
4	P27: Port P2, Bit 7
5	P26: Port P2, Bit 6
6	P25: Port P2, Bit 5
7	P24: Port P2, Bit 4
8	P17: Port P1, Bit 7
9	P16: Port P1, Bit 6
10	P15: Port P1, Bit 5
11	P14: Port P1, Bit 4
12	Hin: Undel. Horizontal Blanking Pulse Input
13	Vin: Vertical Blanking Pulse Input
14	FB_out: Fast Blanking Pulse Output
15	B_out: BLUE Output
16	G_out: GREEN Output
17	R_out: RED Output
18	P23: Port P2, Bit 3
19	P22: Port P2, Bit 2
20	P21: Port P2, Bit 1
21	P20: Port P2, Bit 0
22	P37: Port P3, Bit 7
23	P36: Port P3, Bit 6
24	P35: Port P3, Bit 5
25	P34: Port P3, Bit 4
26	P33: Port P3, Bit 3
27	P32: Port P3, Bit 2
28	P31: Port P3, Bit 1
29	P30: Port P3, Bit 0
30	VS: Tuning Voltage Output
31	IR: Infrared Remote Control Input
32	DA2: Analog 2 Output
33	DA1: Analog 1 Output
34	DA4: Analog 4 Output
35	DA3: Analog 3 Output
36	IMC: IM Bus Clock Output
37	IMI: IM Bus Ident Output

38 IMD: IM Bus Data Input/Output

39 EA (normally at GND)

40 $\overline{\text{Mains}}$: $\overline{\text{Mains}}$ Switch Input/Output

41 $\overline{\text{Reset}}$: $\overline{\text{Reset}}$ Input

42 Clck: Memory Clock Output

43 T1: T1 Input

44 Xtal: Oscillator Input

4.3. Pin Descriptions for 44–Pin PLCC

Pin 1 – Vsup
This pin must be connected to the positive of the 5 V supply.

Pin 2 – Ground
This pin must be connected to the negative of the supply.

Pin 3 – Vstb: Standby Supply pin +5 V
Via this pin, clock oscillator, reset circuit and remote–control decoder are powered. By means of this, it is possible to switch on the TV receiver by remote control. The standby consumption is very small.

Pins 4 to 7, 8 to 21 – Port P2, Bits 0 to 7
The internal configuration of these in/outputs is shown in Fig. 4–3. Direct data transfer with the µC can be executed via this port. The push–pull outputs drive one TTL gate.

Pins 8 to 11 – Port P1, Bits 4 to 7
The internal configuration of these in/outputs is shown in Fig. 4–4. Direct data transfer with the µC can be executed via this port. The outputs are open–drain with a 12 V rating. Four outputs are available in the 44–pin PLCC package. In the 40–pin DIL package up to two P1–outputs (instead of analog outputs) are available by changing the bonding.

Pins 12 and 13 – Vertical and Horizontal synchronization Inputs
These inputs are shown in Fig. 4–5. They are used to synchronize the on–screen display. Negative pulses are needed. The internal delayed–clock–generator for the OSD section synchronizes to the positive edge of the Hin signal.

Pin 14 – Fast Blank Output
This output, which is shown in Fig. 4–6, is used to stop the normal display, and thus characters can be displayed on the screen.

Pins 15 to 17 – Video Outputs Red, Green and Blue (RGB)
These outputs are shown in Fig. 4–7 and used for on–screen display outputs. Therefore, there are different colors to represent the output.

Pins 22 to 29 – Port P3, Bits 0 to 7
The diagram of these open–drain outputs is shown in Fig. 4–8. The voltage handling capability of Port–bits 0 and 1 (pins 28 and 29) is limited to Vsup, but supplies a high output current. The Port–bits 2 to 7 (pins 22 to 27) are outputs with a 12 V rating and a lower output current. In standby, bit 7 of P3 is grounded.

Pin 30 – Tuning Voltage Output
Fig. 4–9 shows the diagram of this push–pull output. Pin 30 supplies the tuning voltage for the capacitance diodes of the TV tuner in the shape of a pulsewidth–modulated signal. After amplification by an external transistor, the tuner DC voltage is derived by multiple RC filtering. A temperature–compensated Zener diode ZTK 33 must be provided for stabilizing the tuning voltage against variations of supply voltage and ambient temperature.

Pin 31 – IR: Remote–Control Input
The internal configuration of this pin is shown in Fig. 4–10. Via an external coupling capacitor of 10 nF, the remote–control signal, amplified by the TBA 2800 preamplifier IC, is fed to the remote–control decoder. The input is self–biasing to approximately 1.4 V, and the input DC resistance is approximately 150 kOhm. For highest input sensitivity, this pin must not be loaded resistively. A small capacitor connected from pin 31 to ground can be useful to suppress steep transients.

Pins 32 to 35 – Analog Outputs
These pins are open–drain outputs with diagram shown in Fig. 4–11. They supply the squarewave signals whose variable pulse/interval ratio is described in section 2.5. These signals serve for actuating the analog control elements. External pull–up resistors are required to produce the squarewave output signals.

Pins 36 to 38 – IM Bus Connections
The internal configuration of these pins are shown in Figs. 4–12 and 4–13. Via these pins, the TVPO 2066 is connected to the IM bus (see section 2.3.). This bus interlinks the TVPO 2066 and the non–volatile memory. The ident and clock outputs are unidirectional (see Fig. 4–12). The data pin acts as input and output for reading and writing data (Fig. 4–13).

Pin 40 – $\overline{\text{Mains}}$: Mains Switch Input/Output
The internal configuration of this input/output is shown in Fig. 4–13. Pin 40 represents the output of the mains flip–flop with a resistive pull–up. The output is active low (mains on). In the case of infrared remote control, this pin acts as output and drives an external switching amplifier, the mains relay, In the case of direct operation, this pin is used as input for switching on the TV receiver by means of an active low level applied to this pin, which sets the main flip–flop. More information is given in section 2.3.

Pin 41 – $\overline{\text{Reset}}$: Reset Input
The internal configuration of this input is shown in Fig. 4–14. The function of this pin is explained in section 2.4. The input circuit is of a Schmitt trigger configuration and provides some noise immunity. In critical applications, however, an additional ceramic capacitor, connected between this pin and GND, may be necessary to increase noise immunity.

Pin 42 – Osc Out: fosc/4096 Output
The internal configuration of this output is shown in Fig. 4–15. This push–pull output provides the memory clock signal for the non–volatile memory MDA 2062 EEPROM (1 kHz). The drive capability of this pin is one TTL gate. This pin is not needed for the non–volatile memory NVM 3060.

Pin 43 – T1: T1 Input
This input can be used as timer input or normal input (e.g. to count the pulses of the horizontal frequency for autosearch function in analog TV sets). For more details about this input, see the CCU 2030, CCU 2050, CCU2070 data sheet.

Pin 44 – Xtal: Oscillator Crystal
The internal configuration of this input/output is shown in Fig. 4–16. For normal use, a 4 MHz crystal is connected to this oscillator pin and to GND. The input is self–biasing to approximately 3.8 V, input DC resistance is approx. 350 kOhm. The output signal is the 4 MHz clock signal of the TVPO 2066.

4.4. Pin Circuits

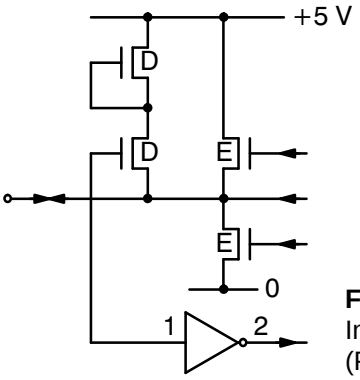


Fig. 4–3:
Inputs and Outputs (Port 2)

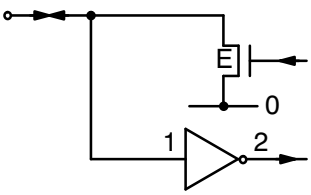


Fig. 4–4:
Inputs and Outputs (Port 1)

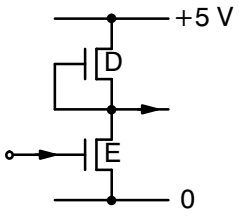


Fig. 4–5:
Inputs (Vin, Hin)

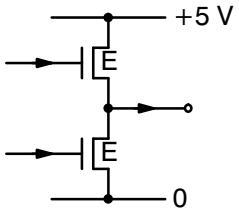


Fig. 4–6:
Output (Fast Blank)

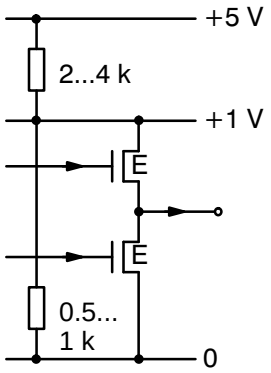


Fig. 4–7:
Outputs (RGB)

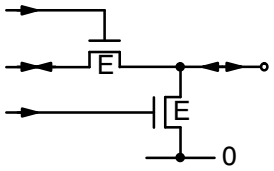


Fig. 4–8:
Outputs (Port 3)

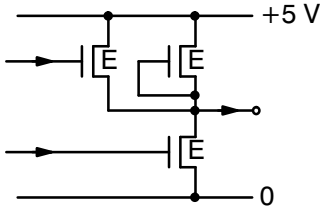


Fig. 4–9:
Output (VS)

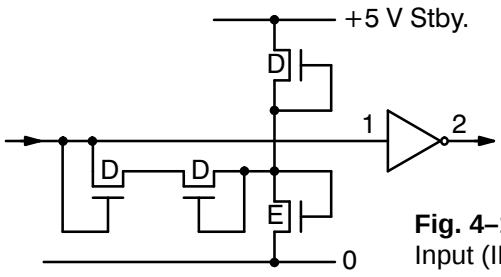


Fig. 4–10:
Input (IR)

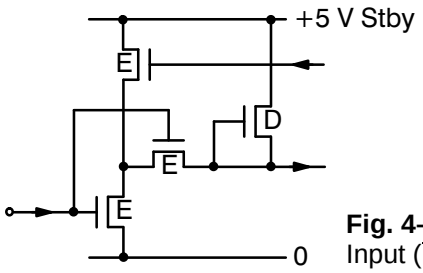


Fig. 4–14:
Input ($\overline{\text{Reset}}$)

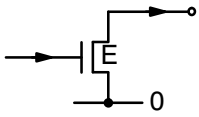


Fig. 4–11:
Outputs (DAC1...4)

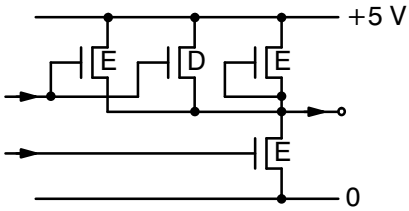


Fig. 4–15:
Output (Mem Osc.)

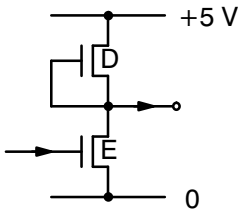


Fig. 4–12:
Outputs (IMC, IMI)

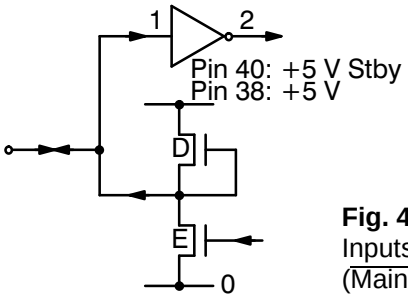


Fig. 4–13:
Inputs/Outputs
($\overline{\text{Mains}}$, IMD)

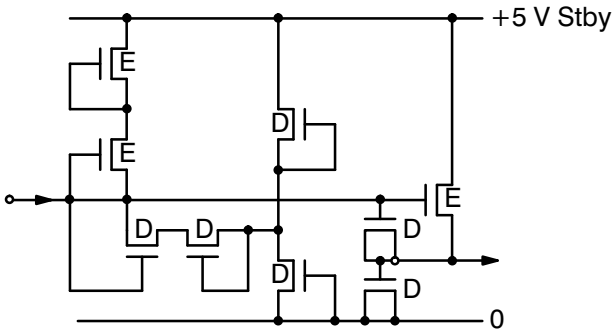


Fig. 4–16: Oscillator (Xtal)

4.5. Electrical Characteristics

All voltages are referred to pin 2. Pins for 44–pin PLCC package.

4.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125	°C
V_{SUP}	Supply Voltage	1	–	6	V
V_{Stby}	Standby Voltage	3	–	6	V
	Output Voltages				
V_{P1O}	Port P1	8 to 11	–0.3	+13.5	V
V_{P2O}	Port P2	4 to 7,			
	Open Drain Configuration	18 to 21	–0.3	V_{SUP}	V
	TTL Configuration		–0.3	V_{SUP}	V
V_{P3O}	Port P3, Bits 0 to 1	28 to 29	–0.3	V_{SUP}	V
	Bits 2 to 7	22 to 27	–0.3	+13.5	V
V_{AO}	Analog	32 to 35	–0.3	+13.5	V
V_{TO}	Tuning	30	–0.3	V_{SUP}	V
V_{IMO}	IM Bus	36 to 38	–0.3	V_{SUP}	V
V_{MO}	Mains	40	–0.3	V_{SUP}	V
V_{OO}	Oscillator	42	–0.3	V_{SUP}	V
	Output Currents				
I_{P1O}	Port P1	8 to 11	–	5	mA
I_{P2O}	Port P2	4 to 7,			
	Open Drain Configuration	18 to 21	–	5	mA
	TTL Configuration		–2	5	mA
I_{P3O}	Port P3	22 to 27	–	5	mA
		28, 29	–	25	mA
I_{AO}	Analog	32 to 35	–	5	mA
I_{TO}	Tuning	30			
	TTL Configuration		–2	5	mA
I_{IMO}	IM Bus	36 to 38			
	TTL Configuration		–2	5	mA
I_{MO}	Mains	40			
	TTL Configuration		–2	5	mA
I_{OO}	Oscillator	42			
	TTL Configuration		–2	5	mA
V_I	**Input Voltages,**				
V_{In}	all Inputs except Pins 8 to 11		–0.3	V_{SUP}	V
V_{IP1}	Port P1	8 to 11	–0.3	13.5	V

4.5.2. Recommended Operating Conditions

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	1	4.75	5.0	5.25	V
V_{Stby}	Standby Voltage	3	4.75	5.0	5.25	V
	Input Voltages					
V_{IRI}	IR	31	400	–	–	mVpp
V_{MIL}	Mains (active)	40	–	–	0.8	V
	Reset	41				
V_{RIL}	(active)		–	–	0.8	V
V_{RIH}	(inactive)		1.8	–	–	V
	All other inputs					
V_{nIH}			2.4	–	–	V
V_{nIL}			–	–	0.8	V
f_{cr}	Clock Frequency	44	3.5	–	4.6	MHz
f_s	Ser. Resonance Freqency of the Crystal at C_L = 20 pF		3.5	–	4.6	MHz
R_r	Effective Series Resistance of the Crystal at C_L = 20 pF		–	–	60	Ω
	Equivalent Load Configuration (in addition to the crystal, see Fig. 4–17)					
C_L	Load Capacitance		–	–	3	pF
C_S	Series Load Capacitance		–	–	5	pF
R_S	Series Load Resistance		300	–	–	kΩ
C31	Coupling Capacitor at Pin 31	31	–	10	–	nF
C_L	Load Capacitance					
	at Pins 30 and 42	30, 42	–	–	150	pF
	at Pins 14 to 17	14 to 17	–	–	15	pF

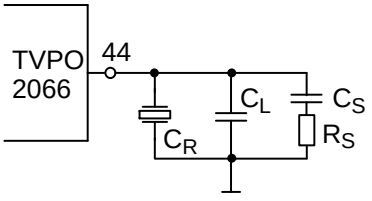


Fig. 4–17: Maximum equivalent load configuration

4.5.3. Characteristics at $V_{SUP} = V_{Stby} = 5$ V, $T_A = 25$ °C

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
	Current Consumption						
I_{SUP}		1	–	90	115	mA	
I_{Stby}		3	–	10	20	mA	
	Output Voltages						
	Port P2, FB TTL Configuration	4 to 7, 14, 18 to 21					
	Tuning, Osc.	30, 42					
V_{OH}			2.7	–	–	V	$-I_{OH} = 100$ µA
V_{OL}			–	–	0.4	V	$I_{OL} = 1.6$ mA
	Port P1	8 to 11					
	Port P3 Bits 2 to 7	22 to 27					
	Analog	32 to 35					
V_{OL}			–	–	0.4	V	$I_{OL} = 4$ mA
V_{OH}	Port P3 Bits 0 and 1	28 to 29	–	–	0.5	V	$I_{OL} = 20$ mA
	RGB	15 to 17					
V_{OH}			0.8	1.0	1.2	V	$-I_{OH} = 25$ µA
V_{OL}			–	–	100	mV	$I_{OL} = 25$ µA
	IM Bus	36 to 38					
V_{OH}			2.7	–	–	V	$-I_{OH} = 200$ µA
V_{OL}			–	–	0.4	V	$I_{OL} = 200$ µA
	Mains	40					
V_{OH}			V_{Stby} –0.4	–	–	V	$-I_{OH} = 100$ µA
V_{OL}			–	–	1	V	$I_{OL} = 1.0$ mA
	Output Leakage Currents						
	Port P1	8 to 11					
	Port P3 Bits 2 to 7	22 to 27					
	Analog	32 to 35					
I_R			–	–	20	µA	$V_O = 12$ V
I_R	Port P3 Bits 0 and 1	28, 29	–	–	20	µA	$V_O = 5$ V
$-I_K$	Short Circuit Output Current IM Bus	36 to 38	–	–	2.8	mA	$V_O = 0$
C_I	Input Capacitance	12, 13	–	5	–	pF	
	Code of the Infrared Transmitter	see Data Sheets SAA 1250, IRT 1250, IRT 1260					

5. Appendix

5.1. DAC Poly–Counter Code

Table 5–1: DAC Poly–Counter Code

Step	**Code** [bin]	**Code** [hex]	**Step**	**Code** [bin]	**Code** [hex]
1	00111111	3F	33	00110110	36
2	00011111	1F	34	00011011	1B
3	00101111	2F	35	00101101	2D
4	00110111	37	36	00010110	16
5	00111011	3B	37	00001011	0B
6	00111101	3D	38	00100101	25
7	00011110	1E	39	00010010	12
8	00001111	0F	40	00001001	09
9	00100111	27	41	00000100	04
10	00110011	33	42	00100010	22
11	00111001	39	43	00010001	11
12	00011100	1C	44	00001000	08
13	00101110	2E	45	00100100	24
14	00010111	17	46	00110010	32
15	00101011	2B	47	00011001	19
16	00110101	35	48	00001100	0C
17	00011010	1A	49	00100110	26
18	00001101	0D	50	00010011	13
19	00000110	06	51	00101001	29
20	00000011	03	52	00010100	14
21	00100001	21	53	00101010	2A
22	00010000	10	54	00010101	15
23	00101000	28	55	00001010	0A
24	00110100	24	56	00000101	15
25	00111010	3A	57	00000010	02
26	00011101	1D	58	00000001	01
27	00001110	0E	59	00000000	00
28	00000111	07	60	00100000	20
29	00100011	23	61	01100000	30
30	00110001	31	62	00111000	38
31	00011000	18	63	00111100	3C
32	00101100	2C	64	00111110	3E

5.2. On–Screen Display Format

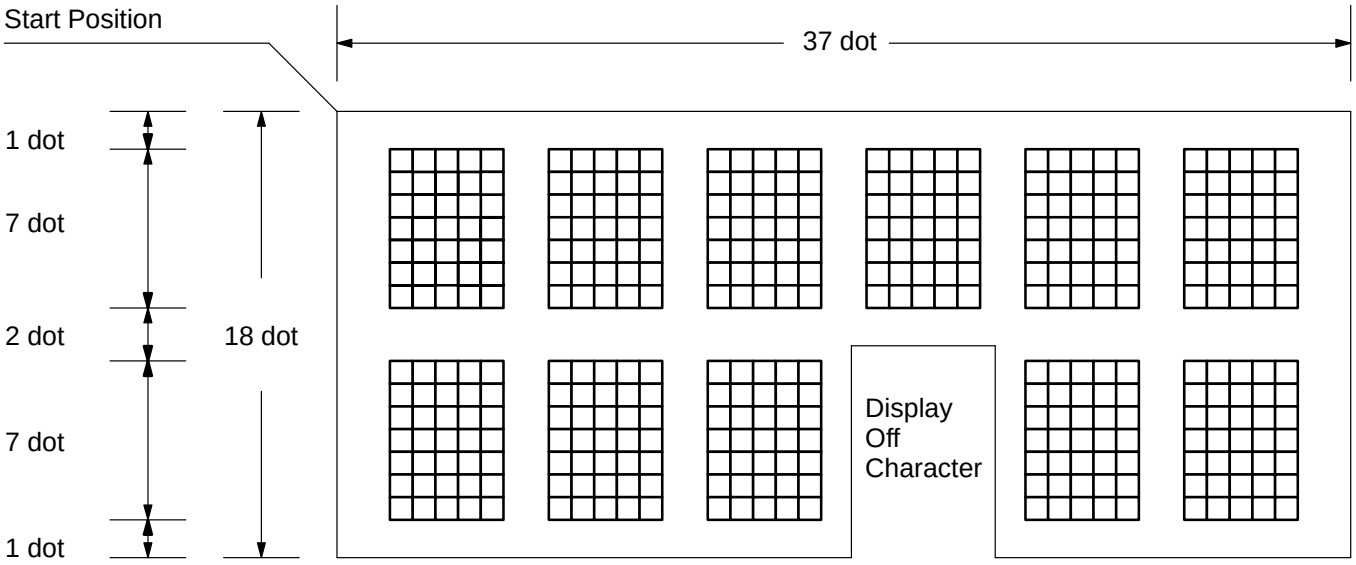
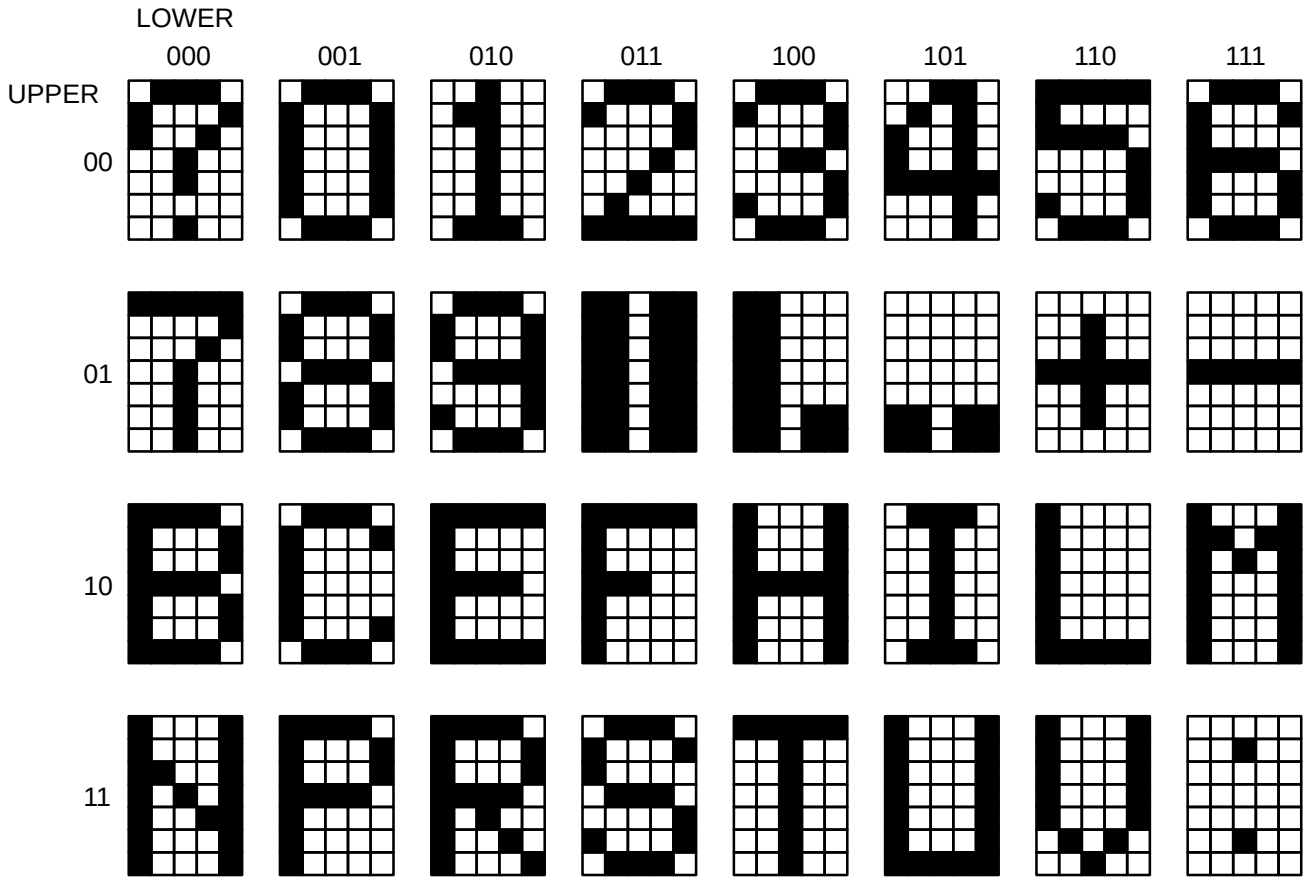
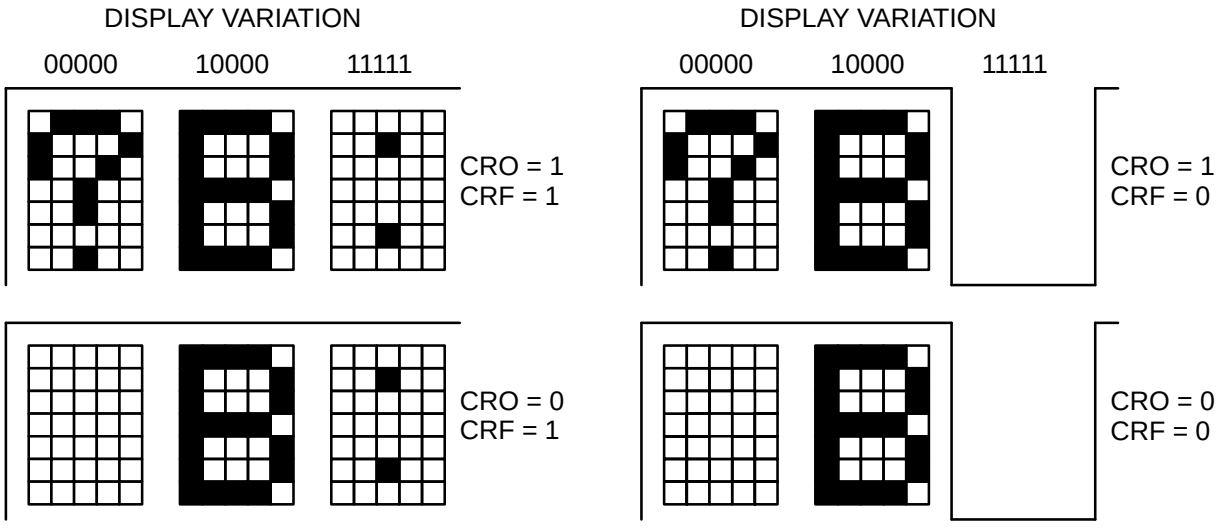


Fig. 5–1: On–screen display format

5.3. Character Set



Also available:
– character set 2: code 0EH = ‘A’ instead of ‘+’
– character set 3: code 0EH = ‘A’ instead of ‘+’
code 0FH = ‘D’ instead of ‘ – ’



5.4. Programmed Versions of TVPO 2066

Some programmed versions of the TVPO 2066 are available (all versions use the non–volatile–memory NVM 3060):

– TVPO 2066–A25
for analog TV–sets. With auto–searching of stations,

4 multi–standards, up to 99 stations, sleep–timer, Teletext with TPU 2735 with FLOF & exended characters (Spanish, Polish, Hungarian and Turkish).

– TVPO 2066–D03
for digital TV–sets. Along with the VSP 2860 and the VCU 2133 it offers a very economical solution of digital TV–sets (simple TV). Some features are 4 standards: PAL, NTSC, SECAM East/West, up to 99 stations, 3 video modes, auto–searching analog output for analog audio (volume) control and more.

Separate data sheets are available for analog and digital versions. Application diagrams will be found there. The last page shows an application diagram for analog TV–sets.

5.5. User Options

If the manufacturer writes his own software for the TVPO 2066, he can choose some options by program mask or diffusion mask.

For explanation of the RESET option see section 2.3.

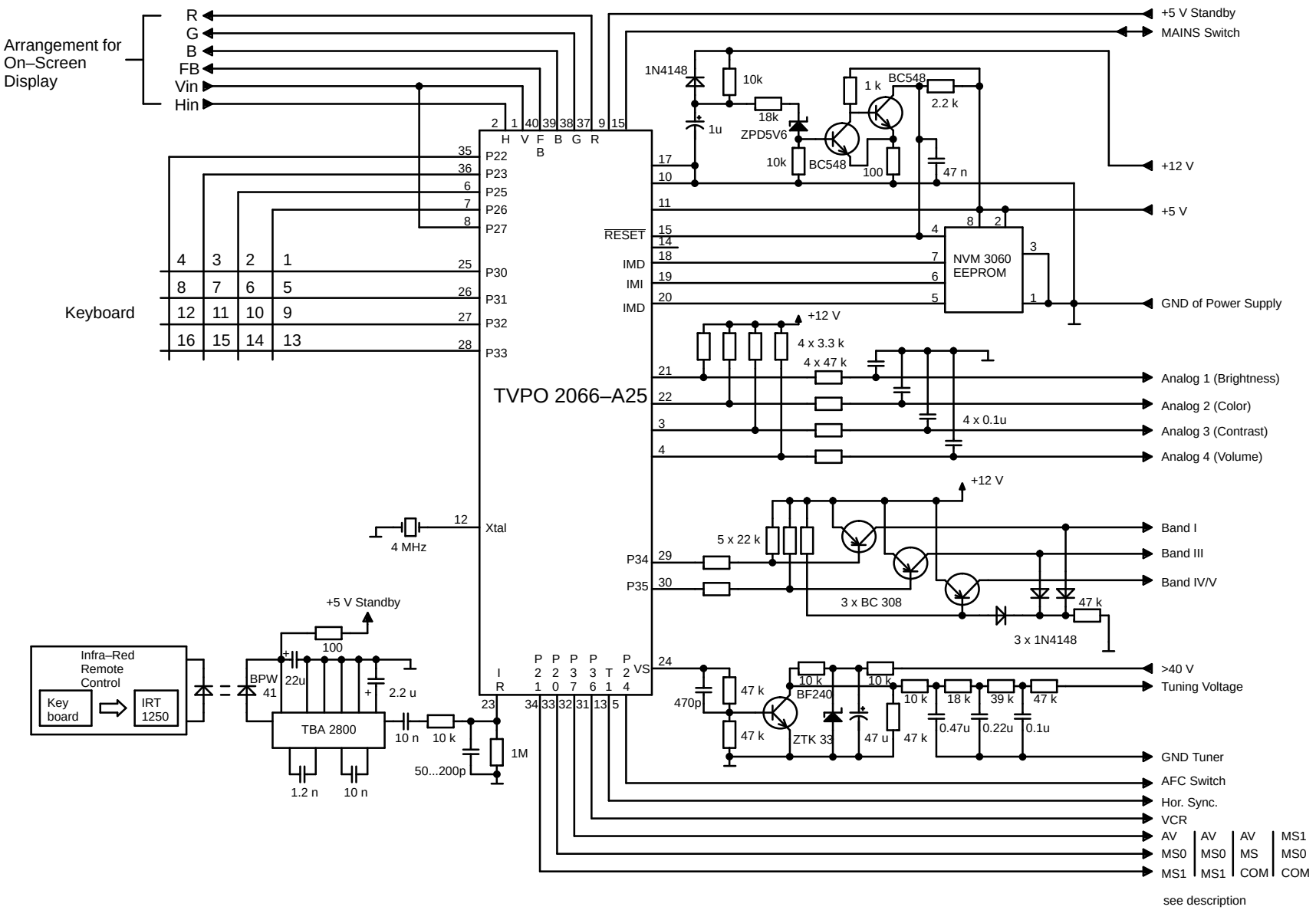
Table 5–2: Options

Option	Default Setting	Alternative Setting
Reset	Reset 1	none or Reset 2
Port 2 configuration	TTL	open–drain
address and commands for power on in the remote–control decoder	address 16, commands 3, 17...26, 35, 36	up to 5 groups in a binary decoder matrix
Character set	Set 1	Set 2, Set 3 or customer specific setting

5.6. Application Circuit (pin numbers for 40–pin DIL package)

ITT Semiconductors Group
World Headquarters
INTERMETALL
Hans-Bunte-Strasse 19
D-7800 Freiburg
Tel. (0761) 517-0, Telex 772 715
Telefax (0761) 517-174

Printed in Germany
by A. Simon & Sohn, Freiburg (9/92)
Order No. 6251-327-3E


Arrangement for On–Screen Display
R
G
B
FB
Vin
Hin
Keyboard
4 3 2 1
8 7 6 5
12 11 10 9
16 15 14 13
TVPO 2066–A25
2 1 40 39 38 37 9 15
H V F B G R B
35 P22
36 P23
6 P25
7 P26
8 P27
25 P30
26 P31
27 P32
28 P33
12 Xtal
4 MHz
23 IR
34 33 32 31 13 5 24
P21 P20 P37 P36 T1 P14 VS
RESET
IMD
IMI
IMD
17
10
11
15
14
18
19
20
21
22
3
4
P34 29
P35 30
+5 V Standby
MAINS Switch
+12 V
+5 V
GND of Power Supply
1N4148
10k
18k
1u
ZPD5V6
BC548
1 k
2.2 k
100
47 n
NVM 3060 EEPROM
4 x 3.3 k
4 x 47 k
4 x 0.1u
Analog 1 (Brightness)
Analog 2 (Color)
Analog 3 (Contrast)
Analog 4 (Volume)
5 x 22 k
3 x BC 308
3 x 1N4148
47 k
Band I
Band III
Band IV/V
>40 V
Tuning Voltage
470p
BF240
ZTK 33
47 u
0.47u
0.22u
0.1u
GND Tuner
AFC Switch
Hor. Sync.
VCR
AV MS0 MS1
AV MS0 MS1
AV MS COM
MS1 MS0 COM
see description
Infra–Red Remote Control
Key board
IRT 1250
BPW 41
22u
2.2 u
100
TBA 2800
10 n
10 k
1M
50...200p
1.2 n
10 n