

High Speed CMOS Logic Quad 2-Input NAND Gate with Open Drain

February 1998

Features

- Buffered Inputs
- Typical Propagation Delay: 8ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$
- Output Pull-up to 10V
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The Harris CD74HC03 and CD74HCT03 logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 74HCT logic family is functionally as well as pin compatible with the standard 74LS logic family.

These open drain NAND gates can drive into resistive loads to output voltages as high as 10V. Minimum values of R_L required versus load voltage are shown in Figure 2.

Ordering Information

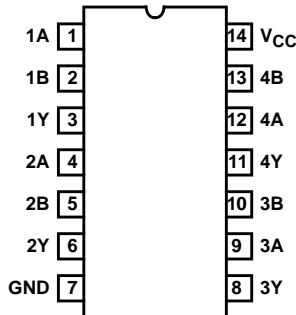
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|-------------|------------------|------------|----------|
| CD74HC03E | -55 to 125 | 14 Ld PDIP | E14.3 |
| CD74HCT03E | -55 to 125 | 14 Ld PDIP | E14.3 |
| CD74HC03M | -55 to 125 | 14 Ld SOIC | M14.15 |
| CD74HCT03M | -55 to 125 | 14 Ld SOIC | M14.15 |

NOTES:

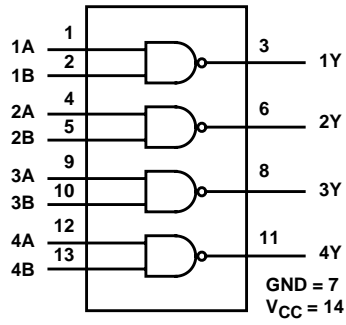
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

CD74HC03, CD74HCT03
(PDIP, SOIC)
TOP VIEW



Functional Diagram



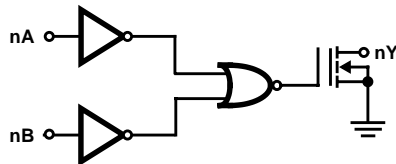
TRUTH TABLE

| A | B | Y | |
|---|---|------------|------------|
| L | L | Z (Note 4) | H (Note 3) |
| H | L | Z (Note 4) | H (Note 3) |
| L | H | Z (Note 4) | H (Note 3) |
| H | H | L | L |

NOTES:

- 3. Requires pull-up (R_L to V_L)
- 4. Without pull-up (high impedance)

Logic Symbol



CD74HC03, CD74HCT03

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC Drain Current, per Output, I_O | |
| For $-0.5V < V_O$ | $-25mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} | $\pm 50mA$ |

Thermal Information

| | |
|--|----------------------------------|
| Thermal Resistance (Typical, Note 5) | θ_{JA} ($^{\circ}C/W$) |
| PDIP Package | 90 |
| SOIC Package | 175 |
| Maximum Junction Temperature (Hermetic Package or Die) . . . | $175^{\circ}C$ |
| Maximum Junction Temperature (Plastic Package) | $150^{\circ}C$ |
| Maximum Storage Temperature Range | $-65^{\circ}C$ to $150^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | $300^{\circ}C$ |
| (SOIC - Lead Tips Only) | |

Operating Conditions

| | |
|---|----------------------------------|
| Temperature Range (T_A) | $-55^{\circ}C$ to $125^{\circ}C$ |
| Supply Voltage Range, V_{CC} | |
| HC Types | $.2V$ to $6V$ |
| HCT Types | $4.5V$ to $5.5V$ |
| DC Input or Output Voltage, V_I , V_O | $0V$ to V_{CC} |
| Input Rise and Fall Time | |
| $2V$ | $1000ns$ (Max) |
| $4.5V$ | $500ns$ (Max) |
| $6V$ | $400ns$ (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25 $^{\circ}C$ | | | -40 $^{\circ}C$ TO 85 $^{\circ}C$ | | -55 $^{\circ}C$ TO 125 $^{\circ}C$ | | UNITS | |
|--|----------|-------------------------|------------|---------------|----------------|-----|-----------|-----------------------------------|---------|------------------------------------|---------|---------|---|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| HC TYPES | | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V | |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V | |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V | |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V | |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V | |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V | |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V | |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V | |
| - | | | - | - | - | - | - | - | - | - | - | V | |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V | |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V | |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA | |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 6 | - | - | 2 | - | 20 | - | 40 | μA | |
| HCT TYPES | | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V | |
| Low Level Input Voltage | V_{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V | |

CD74HC03, CD74HCT03

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} and GND | 4 | 5.5 | - | | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 2 | - | 20 | - | 40 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} (Note 6) | V _{CC} - 2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

6. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|--------|------------|
| nA, nB | 1 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| Propagation Delay, Input to Output (Figure 1) | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 100 | - | 125 | - | 150 | ns |
| | | | 4.5 | - | - | 20 | - | 25 | - | 30 | ns |
| | | | 6 | - | - | 17 | - | 21 | - | 26 | ns |
| Propagation Delay, Data Input to Output Y | t _{PLH} , t _{PHL} | C _L = 15pF | 5 | - | 8 | - | - | - | - | ns | |
| Transition Times (Figure 1) | t _{TLH} , t _{THL} | C _L = 50pF | 2 | - | - | 75 | - | 95 | 18 | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | C _I | - | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 7, 8) | C _{PD} | - | 5 | - | 6.4 | - | - | - | - | - | pF |
| HCT TYPES | | | | | | | | | | | |
| Propagation Delay, Input to Output (Figure 1) | t _{PLH} , t _{PHL} | C _L = 50pF | 4.5 | - | - | 24 | - | 30 | - | 36 | ns |
| Propagation Delay, Data Input to Output Y | t _{PLH} , t _{PHL} | C _L = 15pF | 5 | - | 9 | - | - | - | - | - | ns |
| Transition Times (Figure 1) | t _{TLH} , t _{THL} | C _L = 50pF | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Input Capacitance | C _I | - | - | - | - | 10 | - | 10 | - | 10 | pF |

CD74HC03, CD74HCT03

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|----------|-----------------|--------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Power Dissipation Capacitance (Notes 7, 8) | C_{PD} | - | 5 | - | 9 | - | - | - | - | - | pF |

NOTES:

7. C_{PD} is used to determine the dynamic power consumption, per gate.
8. $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + \sum (V_L^2/R_L)$ (Duty Factor "Low")
 where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage, Duty Factor "Low" = percent of time output is "low", V_L = output voltage, R_L = pull-up resistor.

Test Circuits and Waveforms

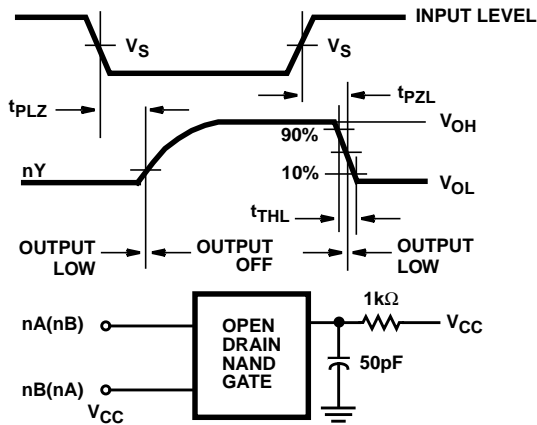


FIGURE 1. TRANSITION TIMES, PROPAGATION DELAY TIMES, AND TEST CIRCUIT

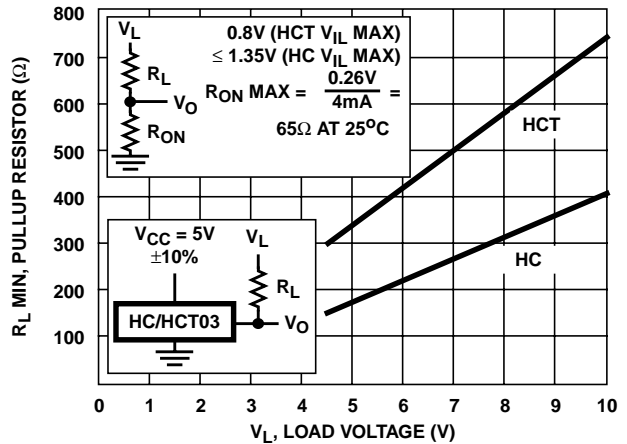


FIGURE 2. MINIMUM RESISTIVE LOAD vs LOAD VOLTAGE

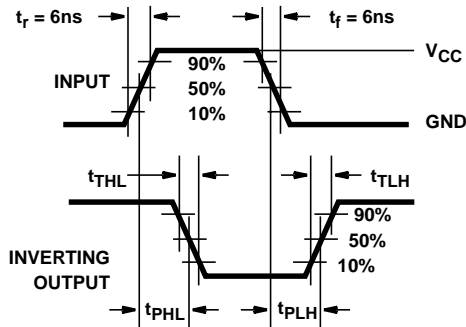


FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

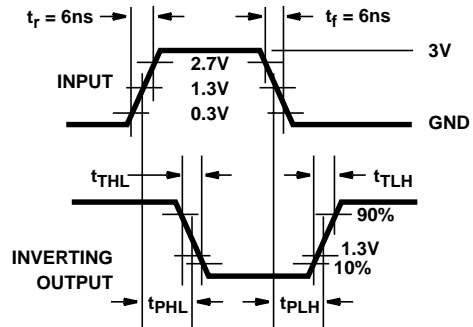


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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