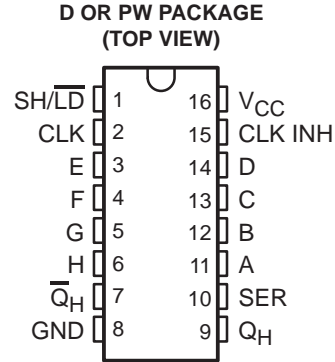- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 13 ns
- $\pm$4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

† Contact factory for details. Q100 qualification data available on request.

D OR PW PACKAGE
(TOP VIEW)

SH/$\overline{\text{LD}}$	1	16	V_{CC}
CLK	2	15	CLK INH
E	3	14	D
F	4	13	C
G	5	12	B
H	6	11	A
$\overline{Q}_H$	7	10	SER
GND	8	9	Q_H

description/ordering information

The SN74HC165 is an 8-bit parallel-load shift register that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/$\overline{\text{LD}}$) input. The SN74HC165 also features a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{\text{LD}}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{\text{LD}}$ is held high. While SH/$\overline{\text{LD}}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOIC – D	Tape and reel	SN74HC165QDRQ1	HC165Q1
	TSSOP – PW	Tape and reel	SN74HC165QPWRQ1	HC165Q1

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{\text{LD}}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift[†]
H	↑	L	Shift[†]

[†] Shift = content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

logic diagram (positive logic)

TEXAS INSTRUMENTS
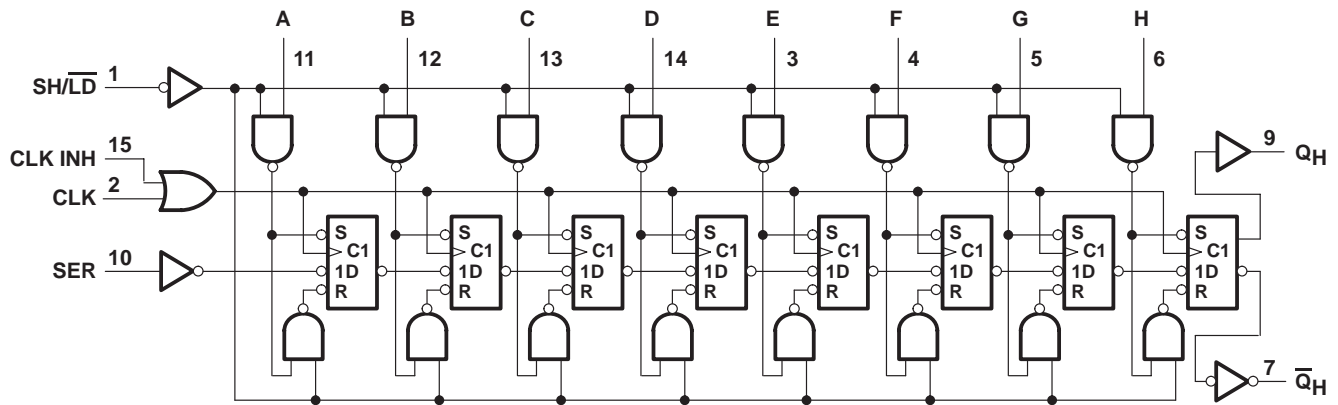
typical shift, load, and inhibit sequence

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 73°C/W
PW package .... 108°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1.   The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2.   The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$‡	Input transition rise/fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–40		125	°C

NOTE 3:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu A$	2 V	1.9	1.998		1.9		V
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
		$I_{OH} = -4\ mA$	4.5 V	3.98	4.3		3.7		
		$I_{OH} = -5.2\ mA$	6 V	5.48	5.8		5.2		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu A$	2 V		0.002	0.1		0.1	V
			4.5 V		0.001	0.1		0.1	
			6 V		0.001	0.1		0.1	
		$I_{OL} = 4\ mA$	4.5 V		0.17	0.26		0.4	
		$I_{OL} = 5.2\ mA$	6 V		0.15	0.26		0.4	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	$I_O = 0$	6 V			8		160	μA
C_i			2 V to 6 V		3	10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	$T_A = 25°C$		MIN MAX		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V		6		4.2	MHz
		4.5 V		31		21	
		6 V		36		25	
t_w	Pulse duration	SH/$\overline{LD}$ low	2 V	80	120		ns
			4.5 V	16	24		
			6 V	14	20		
		CLK high or low	2 V	80	120		
			4.5 V	16	24		
			6 V	14	20		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	2 V	80	120		ns
			4.5 V	16	24		
			6 V	14	20		
		SER before CLK↑	2 V	40	60		
			4.5 V	8	12		
			6 V	7	10		
		CLK INH low before CLK↑	2 V	100	150		
			4.5 V	20	30		
			6 V	17	25		
		CLK INH high before CLK↑	2 V	40	60		
			4.5 V	8	12		
			6 V	7	10		
		Data before SH/$\overline{LD}$↓	2 V	100	150		
			4.5 V	20	30		
			6 V	17	26		
t_h	Hold time	SER data after CLK↑	2 V	5	5		ns
			4.5 V	5	5		
			6 V	5	5		
		PAR data after SH/$\overline{LD}$↓	2 V	5	5		
			4.5 V	5	5		
			6 V	5	5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			2 V	6	13		4.2		MHz
			4.5 V	31	50		21		
			6 V	36	62		25		
t_{pd}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	2 V		80	150		225	ns
			4.5 V		20	30		45	
			6 V		16	26		38	
	CLK	Q_H or $\overline{Q}_H$	2 V		75	150		225	
			4.5 V		15	30		45	
			6 V		13	26		38	
	H	Q_H or $\overline{Q}_H$	2 V		75	150		225	
			4.5 V		15	30		45	
			6 V		13	26		38	
t_t		Any	2 V		38	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	

operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	75	pF

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**
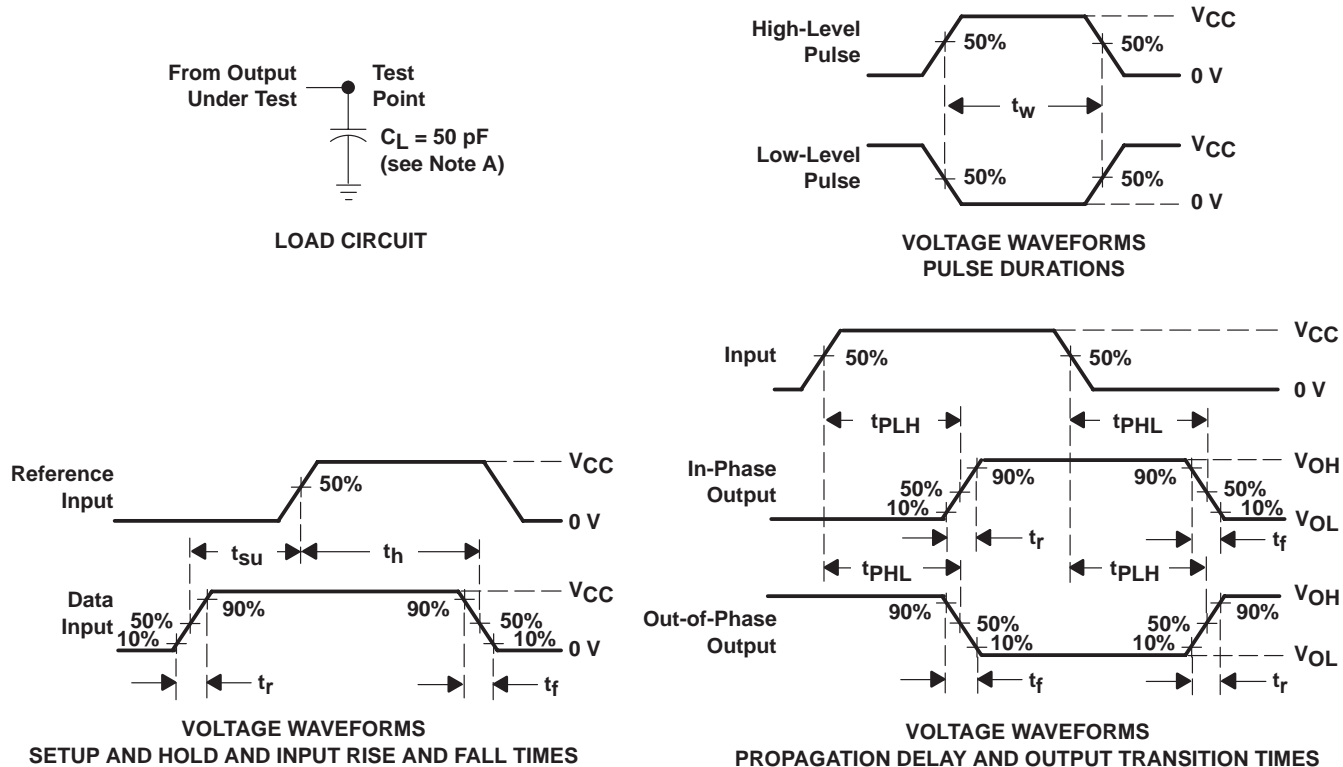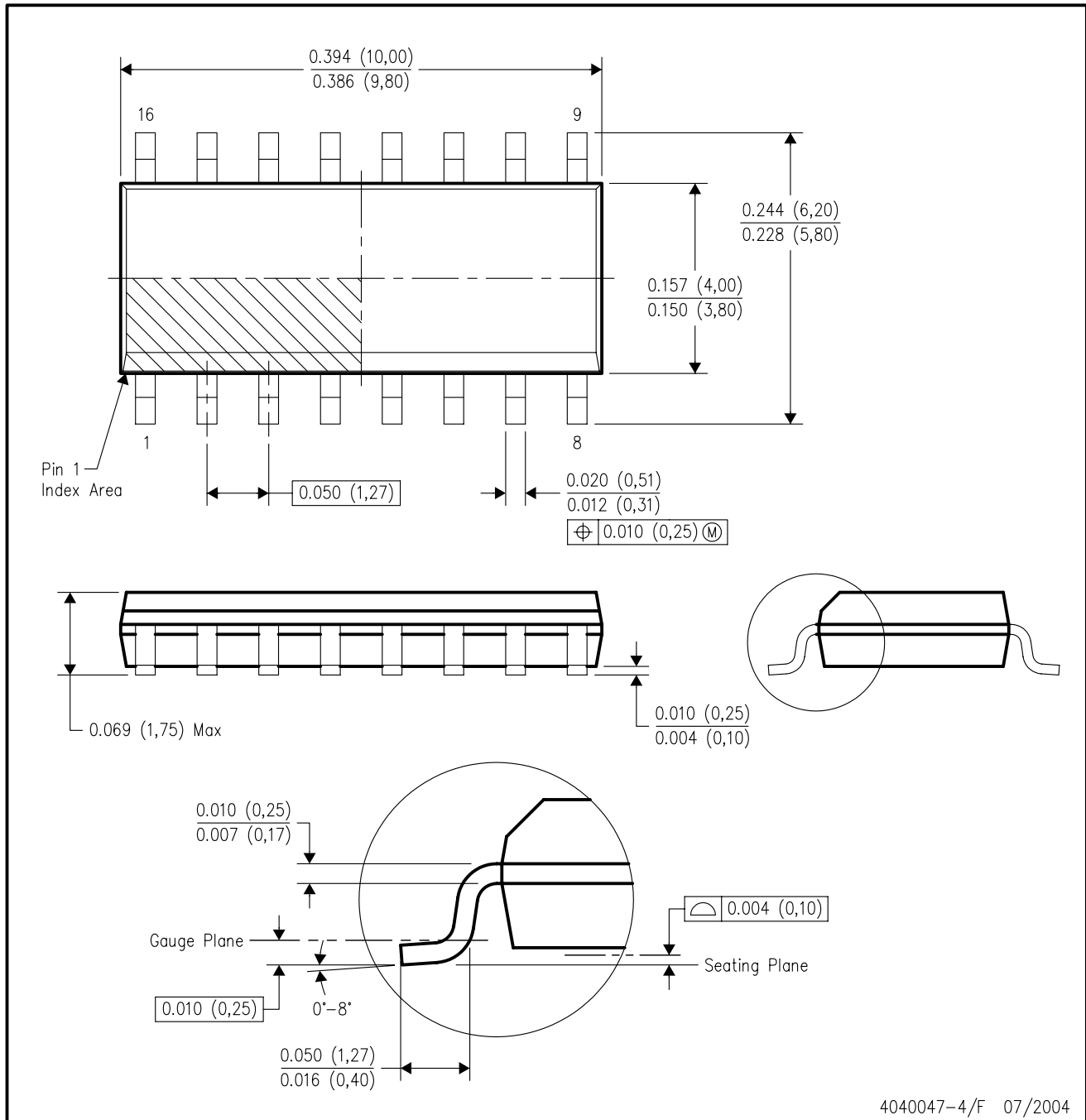
NOTES: A. C_L includes probe and test-fixture capacitance.
  B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
  C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
  D. The outputs are measured one at a time with one input transition per measurement.
  E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

D (R−PDSO−G16) PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)

16

9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/F 07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−012 variation AC.

MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

0,65

0,30
0,19
⊕ 0,10 Ⓜ

14   8

4,50
4,30

6,60
6,20

0,15 NOM

Gage Plane

0,25

0°–8°

0,75
0,50

1   7

A

1,20 MAX

0,15
0,05

Seating Plane

⌓ 0,10

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
      B. This drawing is subject to change without notice.
      C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
      D. Falls within JEDEC MO-153

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