Monolithic JFET Input Operational Amplifiers

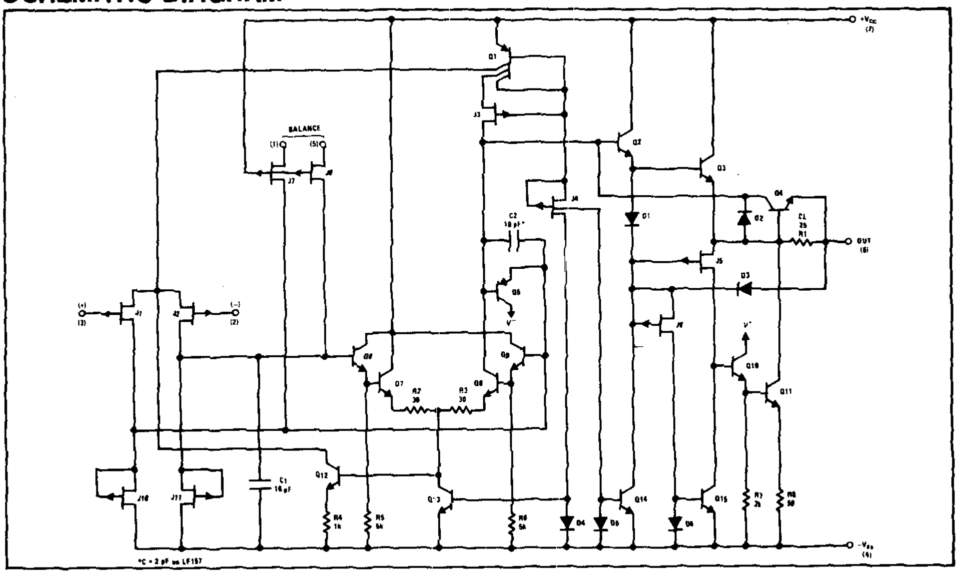
GENERAL DESCRIPTION

The LF155A, 156A and 157A family is composed of JFET input operational amplifiers which by using advanced processing techniques, contain both bipolar transistors and closely matched JFET's on the same chip. The resulting amplifiers feature low input offset voltage and offset voltage drift, low input bias and offset current, and low noise. These devices also feature wide bandwidth, high slew rate and fast settling time making them extremely versatile in such applications as A/D and D/A conversion, sample and hold circuits; analog function circuits, active filters and instrumentation circuits.

DESIGN FEATURES

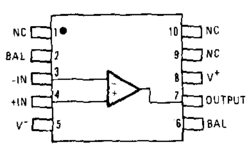
- Low input offset voltage – 1 mV
- Low input offset current – 3 pA
- Low input bias current – 30 pA
- Low input noise voltage – 12 nV/$\sqrt{Hz}$ 156A,157A
  20 nV/$\sqrt{Hz}$ 155A
- Low input noise current – 0.01 pA/$\sqrt{Hz}$
- High DC voltage gain – 200,000 V/V

SCHEMATIC DIAGRAM



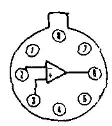
CONNECTION INFORMATION

CQ Flat Package
(Top View)



Order Part Nos.:
LF155AF, LF155F,
LF156AF, LF156F,
LF157AF, LF157F

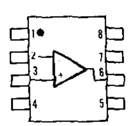
T (TO-99)
Metal Can Package
(Top View)



Note 4: Pin 4 connected to case.

Order Part Nos.:
LF155AH, LF355AH, LF156AH,
LF356AH, LF157AH, LF357AH,
LF155H, LF255H, LF355H, LF156H,
LF256H, LF356H, LF157H, LF257H,
LF357H

DE and NB
Dual In-line Packages
(Top View)



Order Part Nos.:
LF155ADE, LF355ADE, LF156ADE,
LF356ADE, LF157ADE, LF357ADE,
LF155DE, LF255DE, LF355DE, LF156DE,
LF256DE, LF356DE, LF157DE, LF257DE,
LF357DE, LF355AN, LF356AN, LF357AN,
LF355N, LF356N, LF357N

PIN	FUNCTION
1	COMP/BAL
2	–INPUT
3	+INPUT
4	V–
5	BAL
6	OUTPUT
7	V+
8	COMP

ABSOLUTE MAXIMUM RATINGS

	LF155A/6A/7A	LF355A/6A/7A	LF155/6/7	LF255/6/7	LF355/6/7
Supply Voltage	±22V	±22V	±22V	±22V	±18V
Power Dissipation (Note 1) TO-99 (H package)	670 mW	500 mW	670 mW	570 mW	500 mW
Operating Temperature Range	-55 to +125°C	0 to +70°C	-55 to +125°C	-25 to +85°C	0 to +70°C
$T_j(MAX)$	150°C	100°C	150°C	110°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	-65 to +150°C	-65 to +150°C	-65 to +150°C	-65 to +150°C	-65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C	300°C

Note: LF157A, 357A, 157, 257, 357 are decompensated for use in circuits with $A_V > 5$ only.

DC ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	LF155A/156A/157A MIN	TYP	MAX	LF355A/356A/357A MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ KΩ		1.0	2.0		1.0	2.0	mV
Input Offset Current			3	10		3	10	pA
Input Bias Current			30	50		30	50	pA
Input Resistance			10^6			10^6		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ KΩ V_{OUT} ±10V	50K	200K		50K	200K		V/V
The following specifications apply for -55°C ≤ T_A ≤ +125°C for LF155A/156A/157A; 0°C ≤ T_A ≤ +70°C for LF355A/356A/357A.								
Input Offset Voltage	$R_S \leq 10$ KΩ			2.5			2.3	mV
Input Offset Current				10			1.0	nA
Input Bias Current				25			5	nA
Large Signal Voltage Gain	$R_L \geq 2$ KΩ V_{OUT} ±10V	25K			25K			V/V
Output Voltage Swing	$R_L \geq 10$ KΩ	±12	±13		±12	±13		V
Average Offset Voltage Drift			3	5		3	5	μV/°C
Common Mode Rejection Ratio	$R_S \leq 10$ KΩ ΔV ±5V	85	100		85	100		dB
Power Supply Rejection Ratio	$R_S \leq 10$ KΩ ΔV ±5V	85	100		85	100		dB
Input Voltage Range		±11	+15.1 -12		±11	+15.1 -12		V

AC ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	LF155A/355A MIN	TYP	MAX	LF156A/356A MIN	TYP	MAX	LF157A/357A MIN	TYP	MAX	UNITS
Gain Bandwidth Product			2.5		4.0	4.5		15	20		MHz
Settling Time	To 0.01%		4			1.5			1.5		μs
Slew Rate	LF155A/156A: $A_V = 1$ LF157A: $A_V = 5$	3	5		10	12		40	50		V/μs
Input Capacitance			3			3			3		pF
Input Noise Current	F = 100 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$
	F = 1 kHz		0.01			0.01			0.01		pA/$\sqrt{Hz}$
Input Noise Voltage (R_S = 100Ω)	F = 100 Hz		25			15			15		nV/$\sqrt{Hz}$
	F = 1 kHz		20			12			12		nV/$\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$

PARAMETER	LF155A/355A LF155/255		LF355		LF156A/356A LF156/256		LF356		LF157A/357A LF157/257		LF357		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

DC ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	LF155/156/157			LF255/256/257			LF355/356/357			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ K\Omega$		3	5		3	5		3	10	mV
Input Offset Current			3	20		3	20		3	50	pA
Input Bias Current			30	100		30	100		30	200	pA
Input Resistance			10^6			10^6			10^6		MΩ
Large Signal Voltage Gain	$R_L \geq 2\ K\Omega$ V_{OUT} ±10V	50K	200K		50K	200K		25K	200K		V/V
The following specifications apply for -55° C ≤ T_A ≤ +125° C for LF155/156/157; -25° C ≤ T_A ≤ +85° C for LF255/256/257; 0° C ≤ T_A ≤ +70° C for LF355/356/357.											
Input Offset Voltage	$R_S \leq 10\ K\Omega$			7			6.5			13	mV
Input Offset Current				20			1			2	nA
Input Bias Current				50			5			8	nA
Large Signal Voltage Gain	$R_L \geq 2\ K\Omega$ V_{OUT} ±10V	25K			25K			15K			V/V
Output Voltage Swing	$R_L \geq 10\ K\Omega$	±12	±13		±12	± 13		± 12	±13		V
Average Offset Voltage Drift			5			5			5		μV/°C
Common Mode Rejection Ratio	$R_S \leq 10\ K\Omega$ ΔV ±5V	85	100		85	100		80	100		dB
Power Supply Rejection Ratio	$R_S \leq 10\ K\Omega$ ΔV ±5V	85	100		85	100		80	100		dB
Input Voltage Range		±11	+15.1 -12		±11	+15.1 -12		±11	+15.1 -12		V

AC ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	LF155/255/355 TYP	LF156/256 MIN	LF156/256/356 TYP	LF157/257 MIN	LF157/257/357 TYP	UNITS
Gain Bandwidth Product		2.5		5.0		20	MHz
Settling Time	To 0.01%	4		1.5		1.5	μs
Slew Rate	LF155/156: A_V=1 LF157: A_V=5	5	7.5	12	30	50	V/μs
Input Capacitance		3		3		3	pF
Input Noise Current	F = 100 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
	F = 1 kHz	0.01		0.01		0.01	
Input Noise Voltage (R_S = 100Ω)	F = 100 Hz	25		15		15	$nV/\sqrt{Hz}$
	F = 1 kHz	20		12		12	

Note 1: The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = -125°C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For LF255/6/7, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-25°C \leq T_A$ +85°C and $T_{HIGH} = +85°C$ unless otherwise stated. For LF355A/6A/7A, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $0°C \leq T_A \leq +70°C$ and THIGH = +70°C, and for the LF355/6/7 these specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

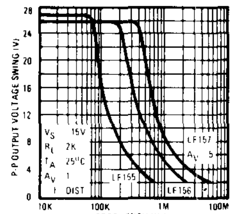
Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/°C typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d. $T_j = T_A + \theta_{jA} P_d$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

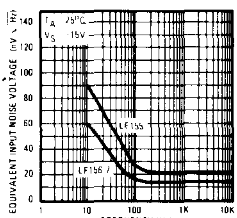
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Setting time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF115/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (see Setting Time Test Circuit).

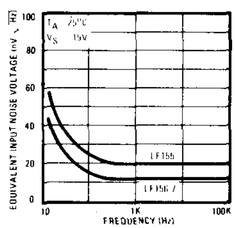
TYPICAL AC PERFORMANCE CHARACTERISTICS



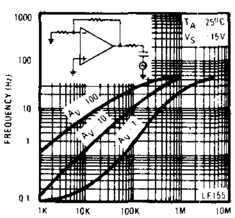
Undistorted Output Voltage Swing



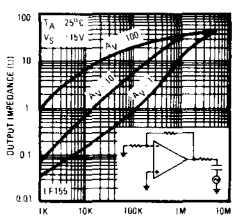
Equivalent Input Noise Voltage



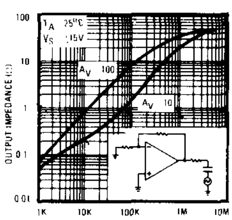
Equivalent Input Noise Voltage (Expanded Scale)



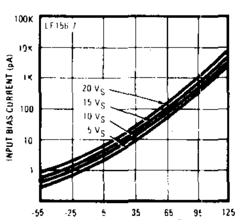
Output Impedance



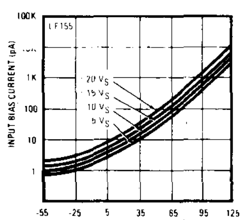
Output Impedance



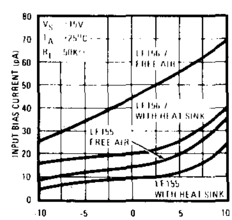
Output Impedance



Input Bias Current

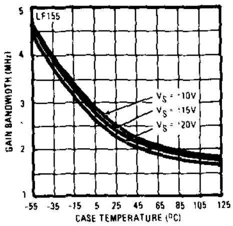


Input Bias Current

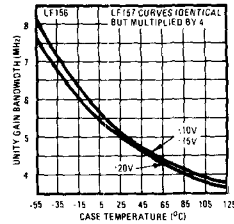


Input Bias Current

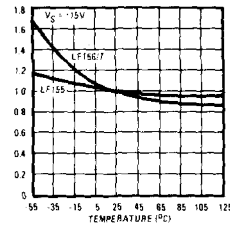
TYPICAL AC PERFORMANCE CHARACTERISTICS (CONT)



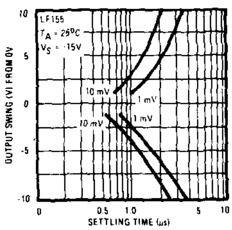
Gain Bandwidth



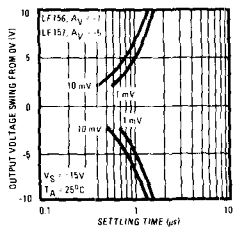
Unity Gain Bandwidth



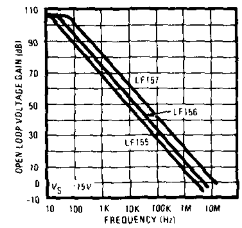
Normalized Slew Rate



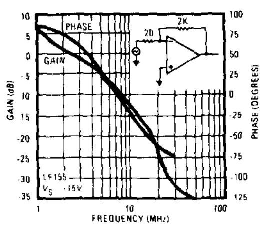
Inverter Setting Time



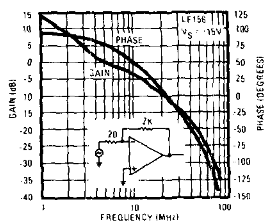
Inverter Setting Time



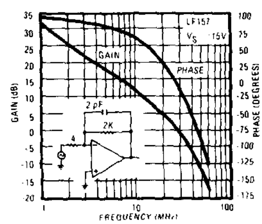
Open Loop Frequency Response



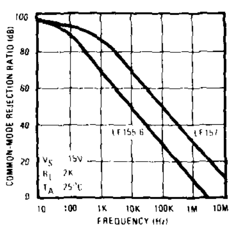
Bode Plot



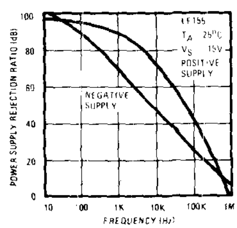
Bode Plot



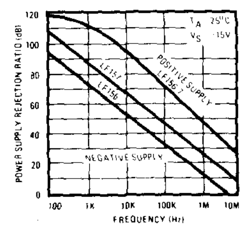
Bode Plot



Common Mode Rejection Ratio

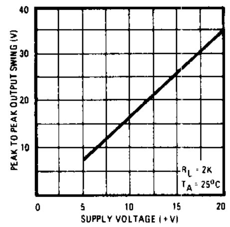


Power Supply Rejection Ratio

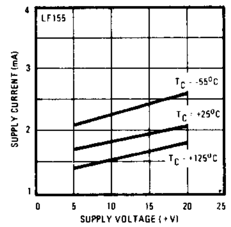


Power Supply Rejection Ratio

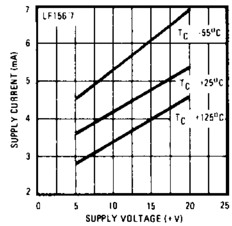
TYPICAL DC PERFORMANCE CHARACTERISTICS



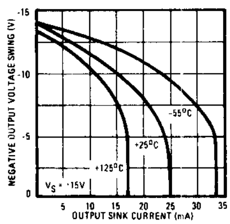
Voltage Swing



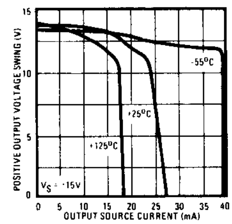
Supply Current



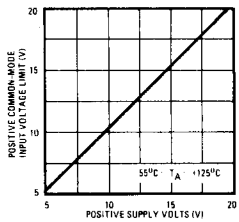
Supply Current



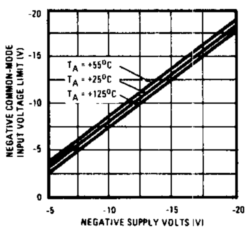
Negative Current Limit



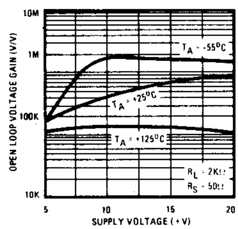
Positive Current Limit



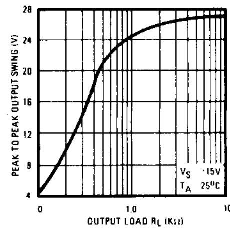
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



Output Voltage Swing

INPUT PROTECTION

This family of op amps has an ion-implanted, P-Channel-JFET input stage. The reverse breakdown voltages are large; therefore there is no need for protective diode-clamps across the inputs. Also, large differential-input voltages can be accommodated without causing large increases in input-bias current. The maximum differential-input-voltage is independent of the supply voltages. These amplifiers have JFET inputs rather than MOSFET inputs, so special handling is not needed. The only word of caution: Do *not* let either input voltage exceed the negative supply voltage. If either input becomes more negative than the negative supply voltage, then excessive currents may flow through the input stage and destroy the unit.

INPUT COMMON-MODE RANGE

An unusual feature of these amplifiers is that the common-mode-input-voltage range for linear operation extends to the positive supply voltage. The common-mode input voltage can even exceed the positive supply voltage by approximately 100 mV. This ability to operate with common-mode voltages of up to, and slightly over, the positive supply voltage holds over the full power-supply range and rated operating temperature range. This capability is very useful in comparator applications where the positive supply voltage can be used as a reference voltage on one of the inputs.

On the negative side, the specified range must be adhered to for proper operation. Exceeding the negative common-mode limit on either input will cause a reversal of phase at the output and will force the amplifier output to the corresponding high or low state (positive or negative saturation). Exceeding the negative common-mode voltage limit on both inputs forces the amplifier output into positive saturation. The amplifier will not "latch" or become damaged by exceeding the negative common-mode limits as long as the peak input current is limited to 30 mA. But there is reversal of phase and this should be carefully considered in designing oscillator circuits, comparators, etc. where common-mode limits might be exceeded.

BROADBANDING

The LF157 family is decompensated to obtain very high slew-rate and gain-bandwidth product. This sacrifices phase-margin and thereby limits the usage to selected applications, but the performance improvement in those particular applications is often substantial. External compensation can be used to optimize overall performance.

The LF157 series is a LF156 circuit decompensated by a factor of 5, and is therefore 5 times faster than the LF156. But to obtain the same degree of stability, the LF157 op amp must be operated at a minimum closed-loop gain of 5 (maximum feedback factor of 0.2). Stability is determined by the phase shift and magnitude of the loop gain. Instability occurs if the loop gain is greater than unity at a frequency where phase shift of 180°C can occur.

Wideband decompensated amplifiers can be used as low gains if frequency compensation is used. An example of a unity-gain circuit is shown in Figure 1.

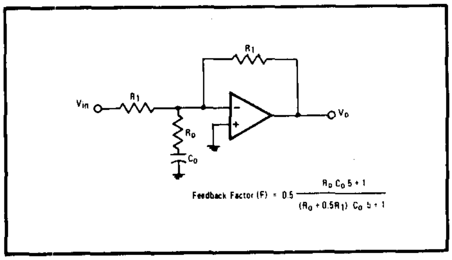


Figure 1. LF157 Unity Gain Operation

At high frequencies, the C_O impedance becomes low and resistor R_O serves to reduce the feedback factor. This circuit has improved AC response with no sacrifice of DC parameters.

INPUT OFFSET VOLTAGE

Conventional FET-input op amps often have an undesirable interaction between adjustment of input offset voltage and drift. With some designs, CMR is also degraded by adjusting input offset voltage. This family of monolithic FET-input op amps has very little interaction of offset adjustment with other parameters. Each mV of offset adjustment typically causes less than $\pm 0.5\mu V/^{\circ}C$ change in drift. The low initial offset, low drift, and low degree of interaction between offset and drift, all combine to make this amplifier family an ideal choice for any high-gain circuit. For example, the LF356A has a maximum input offset voltage at 25°C of 2 mV and a maximum average temperature of $5\mu V/^{\circ}C$. Adjusting input offset on the LF356A will typically cause less than $\pm 1\mu V/^{\circ}C$ of additional drift.

A circuit for adjusting input offset voltage is shown in Figure 2. The range of adjustment will be sufficient to zero any of these amplifiers. For applications requiring very low drift, we recommend using the "A" versions (± 2 mV V_{OS} Max).

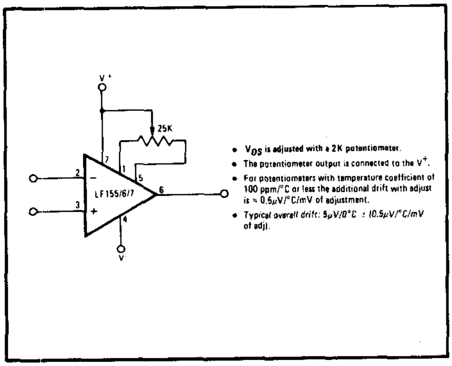


Figure 2. Offset Voltage Adjust

INPUT BIAS CURRENT

Low input bias current is the primary advantage of using FET-input op amps. The reduction in bias current is approximately 1000:1 when compared to standard 741-type op amps. This significantly reduces offset and noise when using high-impedance summing networks or when driving the noninverting input with a high-impedance signal source.

Because the input bias currents are junction leakage currents, there will be a doubling of bias current for each 10°C increase in junction temperature. In normal operation, the junction temperature will rise above the ambient temperature by approximately 10°C to 20°C due to the internal power dissipation. In addition, input bias current varies somewhat with common-mode voltage and power supply voltages. The performance curves illustrate typical changes in bias current due to these effects. For applications where input bias currents must be minimized, these secondary effects should be considered.

APPLICATIONS

General-Purpose Instrumentation Amplifier

The three-op-amp instrumentation amplifier circuit shown in Figure 3 provides excellent performance when implemented with op amps from the LF156 family. The circuit will amplify millivolt-level differential signals with very good rejection of common-mode inputs. The FET-input stages of A1 and A2 provide high-input impedance and very low input-bias-currents. CMR vs frequency is usually good due to the excellent AC response. The interaction between input offset adjustment and drift is unusually low, which is very important when using this circuit at high gain.

Circuit operation is straight-forward: The input amplifiers A1 and A2 buffer and amplify the differential-input-voltage V_d, and the common-mode voltage V_{cm} is rejected by the output amplifier A3. To adjust offsets, ground both inputs ($V_d \to 0$) and set the gain A_d to some high value ($A_d > 100$). Adjust the offset of amplifier A1 for zero at amplifier A3 output ($V_O \to 0$). Then open up the gain-setting path ($R_g \to \infty$) and adjust amplifier A3 offset pot for zero at amplifier A3 output ($V_O \to 0$). Now the gain can be varied over a wide range (1 to 1000 is reasonable) without changing the offset.

To adjust common-mode rejection, connect the two amplifier inputs together ($V_d = 0$) and drive them with an AC input. A low-frequency sine wave with an amplitude of about ±10V will give the best results. Drive the horizontal input of a scope with the AC signal and observe the output V_O on the vertical channel. Vary the CMR adjust pot for minimum peak-to-peak error voltage at V_O. Differential phase shift between amplifiers A1 and A2 and amplifier nonlinearities will limit the CMR obtainable, but 100 dB to 120 dB at 60 Hz is practical. One advantage of using the 156 family is that the R2 impedance can be larger than usual due to the low input bias currents. Therefore, the CMR adjust pot value can be chosen to provide improved resolution. A value of 100 kΩ is a good choice for R2.

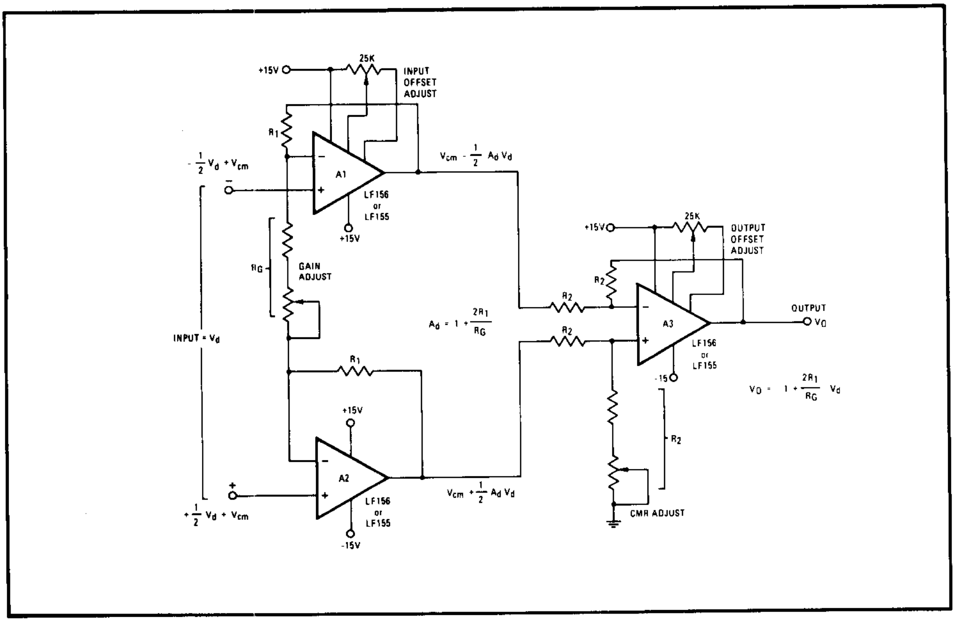


Figure 3. Instrumentation Amplifier

Gain can be varied by changing R_g, and the gain formula is:

$$V_o = \left[1 + \frac{2R_1}{R_g}\right] V_d$$

Minimum gain is unity and the maximum gain is limited by the op-amp open-loop gain. A gain range of 1 to 1000 is readily achieved with excellent performance.

High Q, Bandpass Filter

The LF157 version is recommended for use in active filter circuits. The extra margin of AC response provides much higher performance than can be achieved using standard 741-type op amps.

A bandpass filter using LF157 op amps is shown in Figure 4. This circuit uses positive feedback to achieve high Q. A Q-range of 10 to 50 is practical for this circuit. The transfer function for this circuit is:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{\frac{1}{R_1C_1} K s}{s^2 + \frac{1}{R_1C_1}\left(2 - K\frac{R_1}{R_2}\right) s + \left(\frac{1}{R_1C_1}\right)^2 \left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}\right)}$$

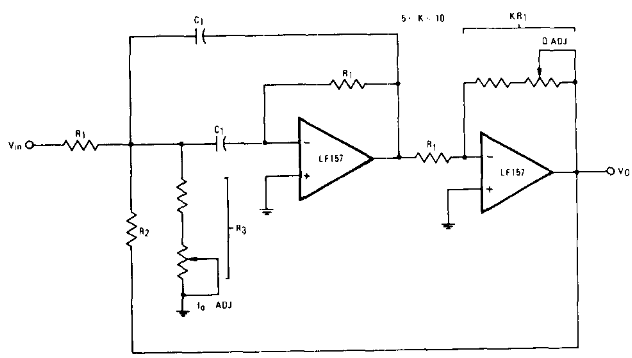
Center frequency f_o is determined primarily by the time constant R_1C_1 and the ratio of R_1 to R_3. Values are chosen such that $R_1 \gg R_3$. A range of 5 to 10 is practical for the gain K.

Center frequency and Q are given by:

$$\omega_o = \frac{1}{R_1C_1}\sqrt{1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}}$$

$$Q = \frac{\omega_o}{\frac{1}{R_1C_1}\left(2 - K\frac{R_1}{R_2}\right)} = \frac{\sqrt{1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}}}{2 - K\frac{R_1}{R_2}}$$

Center frequency can be most easily set by adjusting R_3. The Q can then be independently set by adjusting gain K. Both op amps are operated at loop gains above 5 in this circuit, so the LF157 can be used without encountering stability problems. As with any high-Q bandpass filter, *reasonable care must be taken to lead dress*, grounding, and power-supply bypassing, to avoid undesired oscillation and noise pick-up.



RAYTHEON

Monolithic JFET Input Operational Amplifiers

155/155A 156/156A 157/157A

SELECTION GUIDE

Model No.	Temp. Range	V_{os} (max)		Avg. T_C (max)	I_{os} (max)	I_b (max)	Slew Rate	I_{cc} (max)
		at 25°C	Over T					
LOW SUPPLY CURRENT								
LF155	-55/125	5 mV	7.0 mV		20 pA	100 pA	5V/μsec	4 mA
LF155A	-55/125	2 mV	2.5 mV	5μV/°C	10 pA	50 pA	3V/μsec (min)	4 mA
LF255	-25/85	5 mV	6.5 mV		20 pA	100 pA	5V/μsec	4 mA
LF355	0/70	10 mV	13.0 mV		50 pA	200 pA	5V/μsec	4 mA
LF355A	0/70	2 mV	2.3 mV	5μV/°C	10 pA	50 pA	3V/μsec (min)	4 mA
WIDE BAND								
LF156	-55/125	5 mV	7.0 mV		20 pA	100 pA	7.5V/μsec (min)	7 mA
LF156A	-55/125	2 mV	2.5 mV	5μV/°C	10 pA	50 pA	10V/μsec (min)	7 mA
LF256	-25/85	5 mV	6.5 mV		20 pA	100 pA	7.5V/μsec (min)	7 mA
LF356	0/70	10 mV	13.0 mV		50 pA	200 pA	12V/μsec	10 mA
LF356A	0/70	2 mV	2.3 mV	5μV/°C	10 pA	50 pA	10V/μsec (min)	7 mA
WIDE BAND DECOMPENSATED (AV_{min} = 5)								
LF157	-55/125	5 mV	7.0 mV		20 pA	100 pA	30V/μsec (min)	7 mA
LF157A	-55/125	2 mV	2.5 mV	5μV/°C	10 pA	50 pA	40V/μsec (min)	7 mA
LF257	-25/85	5 mV	6.5 mV		20 pA	100 pA	30V/μsec (min)	7 mA
LF357	0/70	10 mV	13.0 mV		50 pA	200 pA	50V/μsec	10 mA
LF357A	0/70	2 mV	2.3 mV	5μV/°C	10 pA	50 pA	40V/μsec (min)	7 mA

HIGH RELIABILITY OPTIONS

Part Type	Added Screening	To Order:
All LF15X types	With MIL-STD-883 Class B processing	Add suffix 3 example: LF156DE3
All LF35S DE types ceramic	With A+3 processing including burn-in and tightened AQL*	Add suffix 3 example: LF356DE3
All LF35S N types plastic	With A+2 processing including "Hot Rail" testing, burn-in, temp cycle and tightened AQL*	Add suffix 02 example: LF356N02
	With A+1 processing including "Hot Rail" testing, temp cycle and tightened AQL*	Add suffix 01 example: LF356N01

*Full description contained in the quality section of this catalog.