

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4515B

MSI

1-of-16 decoder/demultiplexer with input latches

Product specification
File under Integrated Circuits, IC04

January 1995

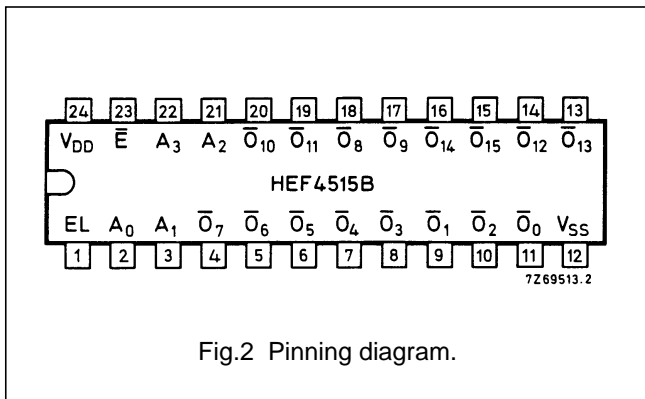
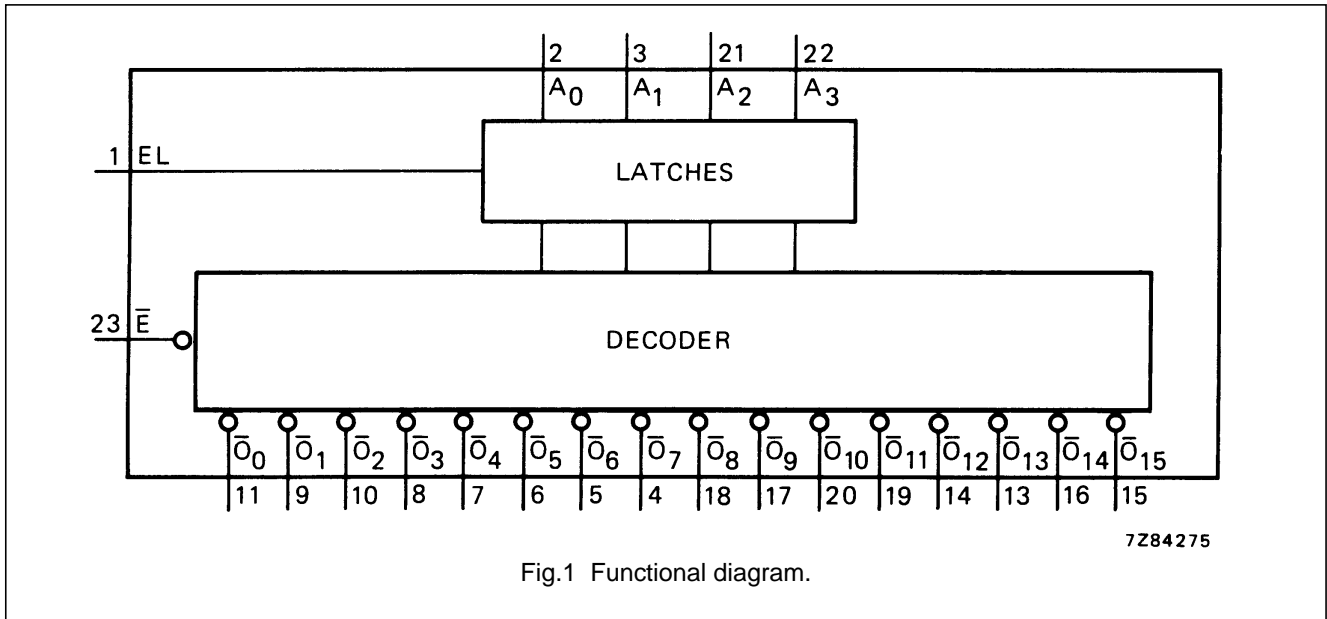
1-of-16 decoder/demultiplexer with input latches

HEF4515B
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DESCRIPTION

The HEF4515B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input (\bar{E}). The 16 outputs (\bar{O}_0 to \bar{O}_{15}) are mutually exclusive active LOW. When EL is HIGH, the selected output is determined by the data on A_n . When EL goes LOW, the last data

present at A_n are stored in the latches and the outputs remain stable. When \bar{E} is LOW, the selected output, determined by the contents of the latch, is LOW. At \bar{E} HIGH, all outputs are HIGH. The enable input (\bar{E}) does not affect the state of the latch. When the HEF4515B is used as a demultiplexer, \bar{E} is the data input and A_0 to A_3 are the address inputs.



PINNING

- A_0 to A_3 address inputs
- \bar{E} enable input (active LOW)
- EL latch enable input
- \bar{O}_0 to \bar{O}_{15} outputs (active LOW)

- HEF4515BP(N): 24-lead DIL; plastic (SOT101-1)
- HEF4515BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)
- HEF4515BT(D): 24-lead SO; plastic (SOT137-1)
- (): Package Designator North America

APPLICATION INFORMATION

Some examples of applications for the HEF4515B are:

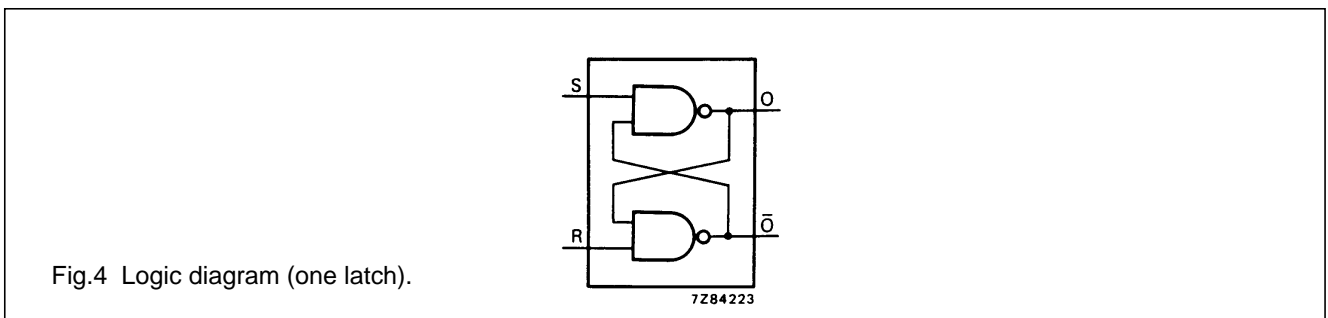
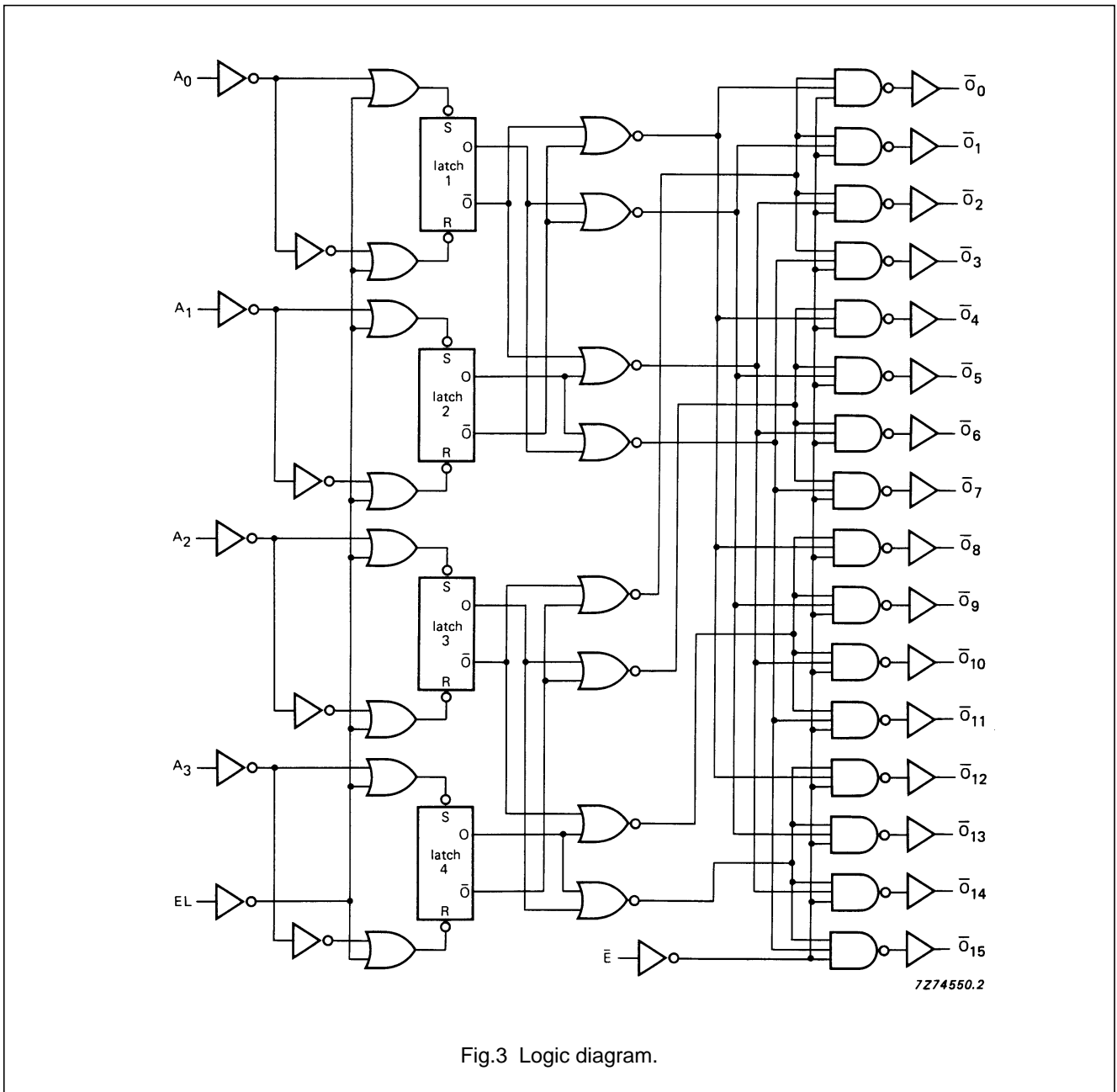
- Digital multiplexing.
- Address decoding.
- Hexadecimal/BCD decoding.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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TRUTH TABLE

INPUTS					OUTPUTS																
\bar{E}	A ₀	A ₁	A ₂	A ₃	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7	\bar{O}_8	\bar{O}_9	\bar{O}_{10}	\bar{O}_{11}	\bar{O}_{12}	\bar{O}_{13}	\bar{O}_{14}	\bar{O}_{15}	
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

Notes

- EL = HIGH; H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage); X = state is immaterial

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays A _n , EL → \bar{O}_n HIGH to LOW	5	t _{PHL}	260	520	ns	233 ns + (0,55 ns/pF) C _L	
	10		95	190	ns	84 ns + (0,23 ns/pF) C _L	
	15		65	130	ns	57 ns + (0,16 ns/pF) C _L	
	LOW to HIGH	5	t _{PLH}	270	550	ns	243 ns + (0,55 ns/pF) C _L
		10		95	190	ns	84 ns + (0,23 ns/pF) C _L
		15		65	130	ns	57 ns + (0,16 ns/pF) C _L
\bar{E} → \bar{O}_n HIGH to LOW	5	t _{PHL}	175	350	ns	148 ns + (0,55 ns/pF) C _L	
	10		65	130	ns	54 ns + (0,23 ns/pF) C _L	
	15		45	90	ns	37 ns + (0,16 ns/pF) C _L	
	LOW to HIGH	5	t _{PLH}	200	400	ns	173 ns + (0,55 ns/pF) C _L
		10		70	140	ns	59 ns + (0,23 ns/pF) C _L
		15		50	100	ns	42 ns + (0,16 ns/pF) C _L

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AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA			
Output transition times	5	t_{THL}		90	180	ns	40 ns + (1,0 ns/pF) C_L 14 ns + (0,42 ns/pF) C_L 11 ns + (0,28 ns/pF) C_L 35 ns + (1,0 ns/pf) C_L 14 ns + (0,42 ns/pF) C_L 11 ns + (0,28 ns/pF) C_L		
				HIGH to LOW	35	65		ns	
					25	50		ns	
	5		t_{TLH}		85	170		ns	
					LOW to HIGH	35		70	ns
						25		50	ns
Set-up time $A_n \rightarrow \text{EL}$	5	t_{su}	120	60	ns	see also waveforms Fig.5			
	10		40	20	ns				
	15		30	15	ns				
Hold time $A_n \rightarrow \text{EL}$	5	t_{hold}	0	60	ns				
	10		0	20	ns				
	15		0	15	ns				
Minimum EL pulse width; HIGH	5	t_{WELH}	120	60	ns				
	10		40	20	ns				
	15		30	15	ns				

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1100 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5500 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$16\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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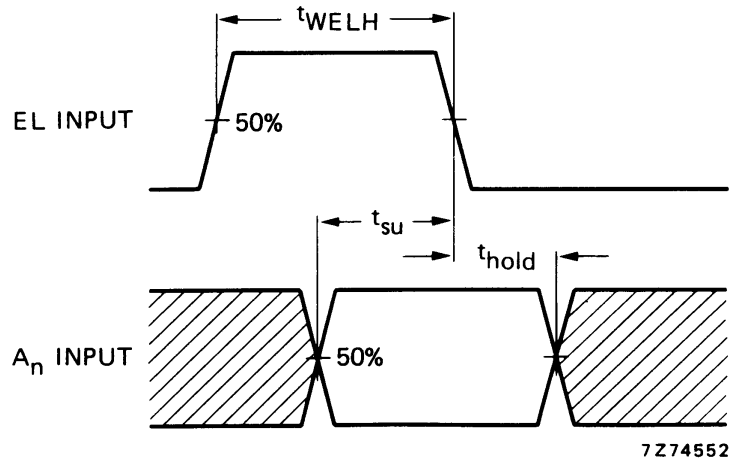


Fig.5 Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL. Set-up and hold times are shown as positive values but may be specified as negative values.