

SANYO

No. 4817A

LC78211, 78212, 78213**Analog Function Switch**

Applications

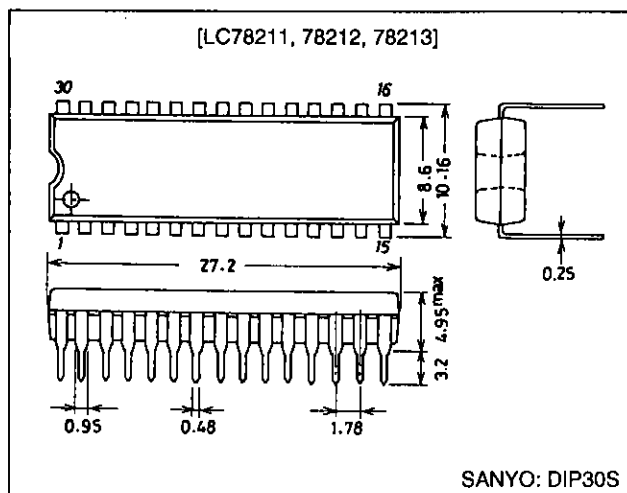
Function switching under serial data control in amplifiers, receivers, and other electronic equipment

Features

- Two sets of eight (or in the LC78213, seven) built-in circuits with three switching configurations available based on differing internal connections
- Control according to serial data sent from a microprocessor, and easy connection to 5 V microprocessors
- Two identical products can be connected to a shared bus due to the provision of a select pin (S).
- A reset pin that turns off all analog switches
- A ± 20 V withstand voltage rating allows these products to provide a wide dynamic range.

Package Dimensions

unit: mm

3061-DIP30S

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

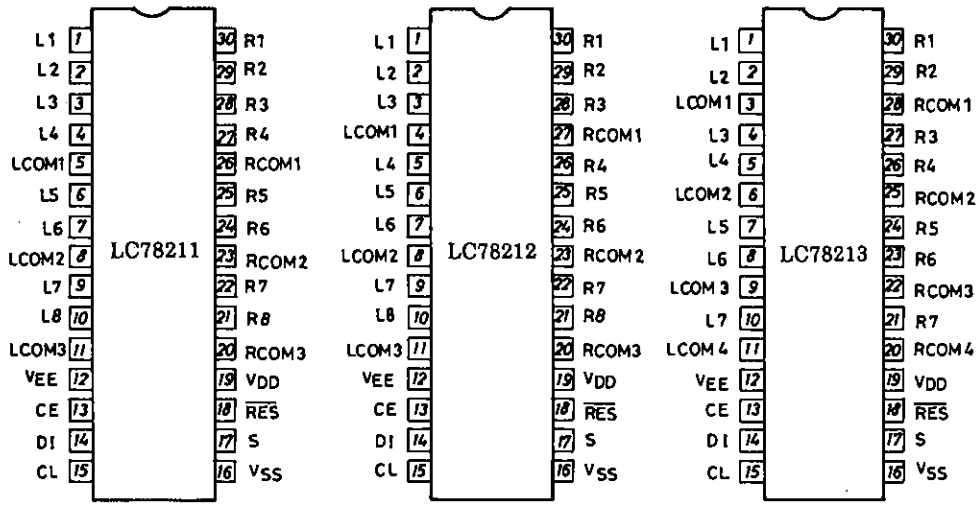
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD \text{ max}}$	V_{DD}	-0.3 to +20	V
	$V_{EE \text{ max}}$	V_{EE}	-20 to +0.3	V
Maximum input voltage	V_{I1}	DI, CL, CE, S, $\overline{\text{RES}}$	-0.3 to +20	V
	V_{I2}	L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	$V_{EE} - 0.3$ to $V_{DD} + 0.3$	V
Analog switch potential difference when on	ΔV_{ON}	With the switch on	0.5	V
Allowable power dissipation	$P_d \text{ max}$	$T_a \leq 75^\circ\text{C}$	100	mW
Operating temperature range	T_{opr}		-30 to +75	$^\circ\text{C}$
Storage temperature range	T_{stg}		-40 to +125	$^\circ\text{C}$

SANYO Electric Co., Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

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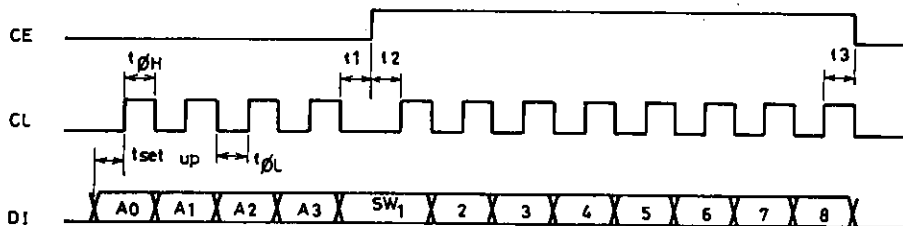
Pin Assignments



Allowable Operating Ranges at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $|V_{DD}| \geq |V_{EE}|$

Parameter	Symbol	Conditions	min	typ	max	Unit
Maximum supply voltage	V_{DD}	$V_{DD} - V_{EE} \geq 12\text{ V}; V_{DD}$	6.0		18.5	V
	V_{EE}	$V_{DD} - V_{EE} \geq 12\text{ V}; V_{EE}$	-18.5		0	V
Input high level voltage	V_{IH1}	DI, CL, CE	4.0		18.5	V
	V_{IH2}	S, RES	$0.7 V_{DD}$		V_{DD}	V
Input low level voltage	V_{IL1}	DI, CL, CE	0		0.7	V
	V_{IL2}	S, RES	0		$0.3 V_{DD}$	V
Analog switch input voltage range	V_{IN}	L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	V_{EE}		V_{DD}	V
Low level clock pulse width	$t_{\theta L}$	CL	0.5			μs
High level clock pulse width	$t_{\theta H}$	CL	0.5			μs
Setup time	$t_{\text{set up}}$	CL, DI	0.5			μs
	$t1^*$	CL, CE	0.5			μs
	$t2^*$	CL, CE	0.5			μs
	$t3^*$	CL, CE	0.5			μs
Minimum reset pulse width	t_{wRES}	$V_{DD} \geq 6\text{ V}; RES$	1.0			μs
Hysteresis	V_H	CL, CE, DI	0.3			V

Note: * CE, CL and DI waveforms

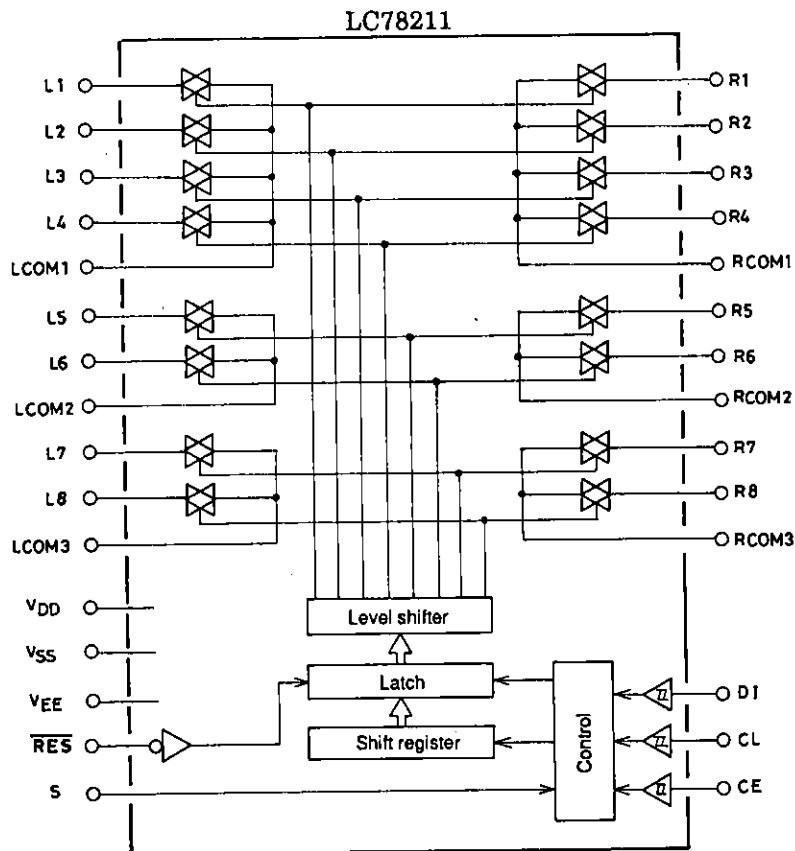


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Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Analog switch on resistance	R_{ON1}	$I = 1\text{ mA}$, $V_{DD} - V_{EE} = 12\text{ V}$: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		150		Ω
	R_{ON2}	$I = 1\text{ mA}$, $V_{DD} - V_{EE} = 37\text{ V}$: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		70		Ω
Total harmonic distortion	THD1	$V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, $V_{DD} - V_{EE} = 37\text{ V}$: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		0.0015	0.01	%
	THD2	$V_{IN} = 0.1\text{ Vrms}$, $f = 1\text{ kHz}$, $V_{DD} - V_{EE} = 37\text{ V}$: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		0.01	0.05	%
Feedthrough	F_{TH}	$V_{IN} = 0\text{ dBV}$, $f = 10\text{ kHz}$, $V_{DD} - V_{EE} = 37\text{ V}$: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		55		dB
Crosstalk	CT	$V_{IN} = 0\text{ dBV}$, $f = 10\text{ kHz}$, $V_{DD} - V_{EE} = 37\text{ V}$: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		75		dB
Input high level current	I_{IH}	$V_i = 18.5\text{ V}$: DI, CL, CE, S, $\overline{\text{RES}}$			+10	μA
Input low level current	I_{IL}	$V_i = 0\text{ V}$: DI, CL, CE, S, $\overline{\text{RES}}$	-10			μA
Analog switch leakage current (off state)	I_{OFF}	$V_i = V_{EE}$ to $V_{EE} + 37\text{ V}$: L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4	-10		+10	μA
Current drain	I_{DD}	V_{DD}			1.0	mA

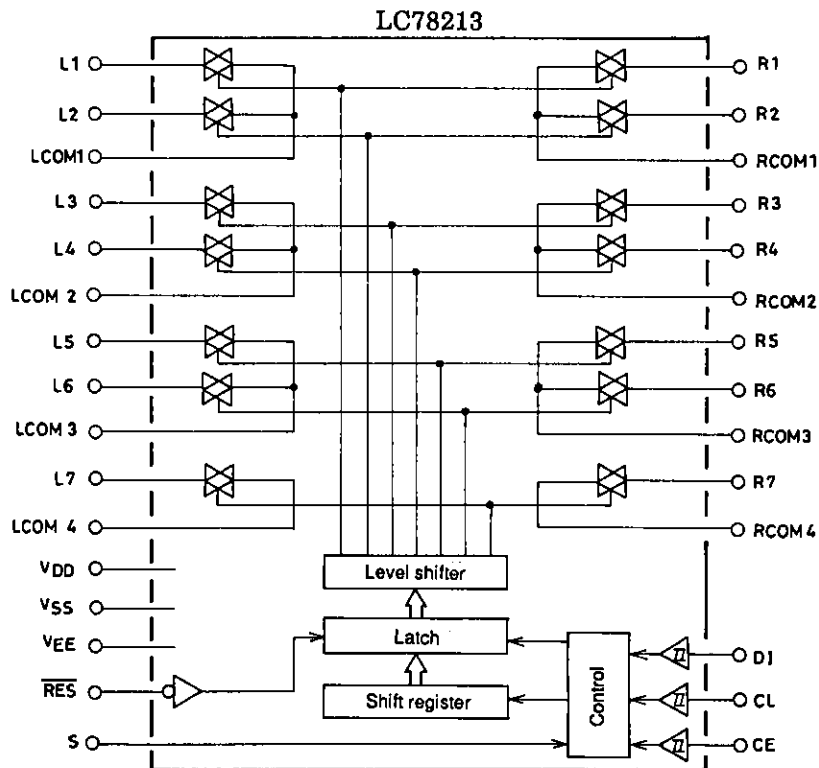
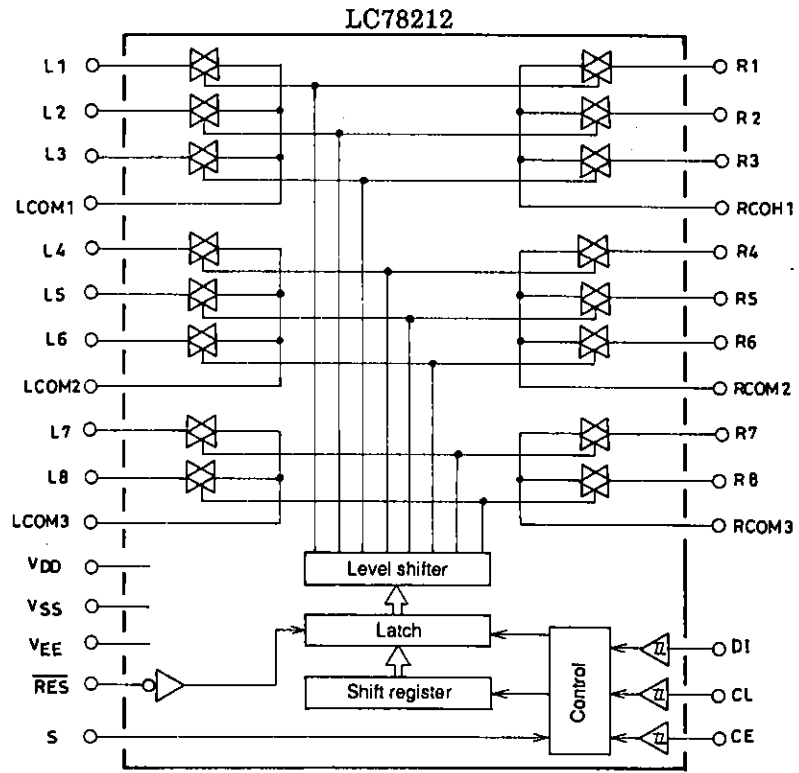
Equivalent Circuit Block Diagrams



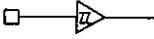


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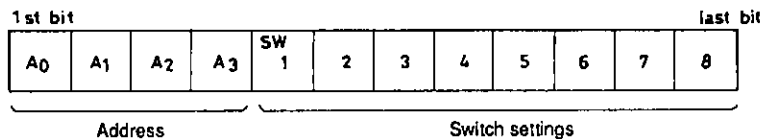
Pin Functions

Pin	I/O	Internal equivalent circuit	Pin function																																											
V _{DD} , V _{SS} , V _{EE}			Power supply																																											
L1 to L8, R1 to R8, LCOM1 to LCOM4, RCOM1 to RCOM4		See the block diagram.	Analog switch input and output																																											
CL, DI, CE	I		Serial data input (Schmitt buffer) CLClock input DIData input CEChip enable																																											
S	I		Selection of one of two chips The address is set to the values shown in the table below according to the level input to the S pin. <table border="1" data-bbox="852 692 1458 949"> <thead> <tr> <th rowspan="2">Product</th> <th rowspan="2">S pin level</th> <th colspan="4">Address</th> </tr> <tr> <th>A₀</th> <th>A₁</th> <th>A₂</th> <th>A₃</th> </tr> </thead> <tbody> <tr> <td rowspan="2">LC78211</td> <td>L</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>H</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td rowspan="2">LC78212</td> <td>L</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>H</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td rowspan="2">LC78213</td> <td>L</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>H</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Product	S pin level	Address				A ₀	A ₁	A ₂	A ₃	LC78211	L	0	1	0	1	H	1	1	0	1	LC78212	L	0	0	1	1	H	1	0	1	1	LC78213	L	0	1	1	1	H	1	1	1	1
Product	S pin level	Address																																												
		A ₀	A ₁	A ₂	A ₃																																									
LC78211	L	0	1	0	1																																									
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LC78213	L	0	1	1	1																																									
	H	1	1	1	1																																									
$\overline{\text{RES}}$	I		Reset input The states of the analog switches are undefined when power is first applied. Setting this pin low will force all switches the off state.																																											

Operation

1. Data Input Procedure

The LC78211, LC78212 and LC78213 are controlled by inputting specified data to the CL, DI and CE pins. The input data consists of 12 bits, of which four bits are address and eight bits are data.



Bits correspond to the L1 to L8 and R1 to R8 analog switches, and a value of one turns the corresponding switch on, and a value of zero turns it off.

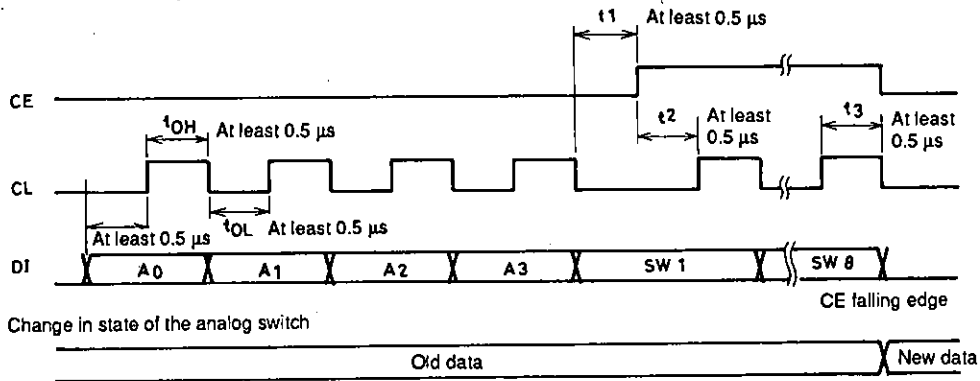
- 0Off
- 1On

The address is used when the chip is connected to a shared bus. The data (address) that must be transmitted depends on the S pin and the particular product as shown in the table below.

Product	S pin level	Address			
		A ₀	A ₁	A ₂	A ₃
LC78211	L	0	1	0	1
	H	1	1	0	1
LC78212	L	0	0	1	1
	H	1	0	1	1
LC78213	L	0	1	1	1
	H	1	1	1	1

Note: The bit for switch eight in the LC78213 is a "don't care" bit, that is it can be either 0 or 1 without affecting chip function. This is because the LC78213 has two sets of seven (not eight) circuits.

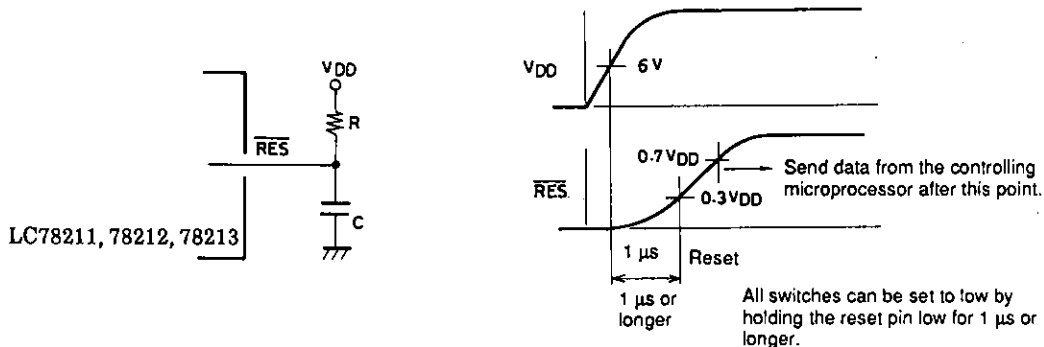
2. DI, CL and CE Timing



Data is read in on the rising edge of CL and latched on the falling edge of CE.

3. Notes on the Reset Pin

The states of the analog switches are undefined when power is first applied. However, it is possible to use the reset pin to force all switches to the off state by connecting an RC circuit to this pin.



4. Using a CCB Bus with Multiple ICs

The LC78211, LC78212 and LC78213 retain their prior state until they receive data with a matching address.

5. Replacing Earlier Models

Caution is required when replacing an LC7821N, LC7823N and LC7823N with an LC78211, LC78212 and LC78213, since the S pin threshold levels differ.

6. Handling of Unused Input Pins

We recommend connecting any unused switch pin to V_{SS} through a resistor of up to a few 100 k Ω to prevent damage from static electricity.

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