Ordering number: EN 3584A

Silicon-gate CMOS IC

SANYO No.3584A

LC7215, 7215F, 7215FM

MW/LW PLL Frequency Synthesizers

OVERVIEW

The LC7215, LC7215F and LC7215FM are phase-locked-loop frequency synthesizers that provide accurate reference frequencies over the MW and LW bands, making them ideally suited for AM tuners.

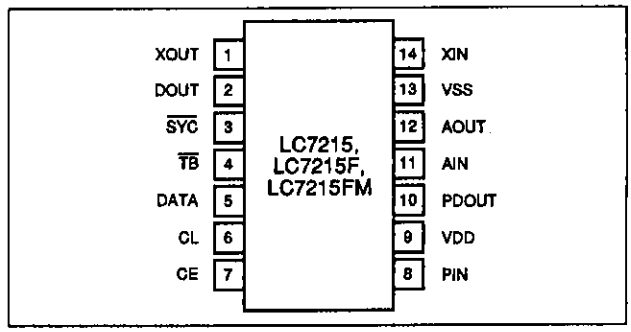
Each device comprises a 20-bit shift register and latch, a 14-bit programmable divider, a reference divider, a phase detector and a charge pump. The LC7215 has a maximum input frequency of 13 MHz, and the LC7215F and LC7215FM, 20 MHz. User-selectable reference frequencies are 1, 5, 9 and 10 kHz. All devices can be used for double-conversion demodulation.

The LC7215, LC7215F and LC7215FM operate from a 5 V supply. The LC7215 and LC7215F are available in 14-pin DIPs, and the LC7215FM, 14-pin MFPs.

FEATURES

- Reference frequencies of 1, 5, 9 and 10 kHz
- 20 MHz (LC7215F, LC7215FM) and 13 MHz (LC7215) maximum input frequencies
- 60 kHz controller clock output
- 8 Hz time-base output
- On-chip transistor for the low-pass filter amplifier
- On-chip programmable divider
- 5 V supply
- 14-pin DIP (LC7215, LC7215F) and 14-pin MFP (LC7215FM)

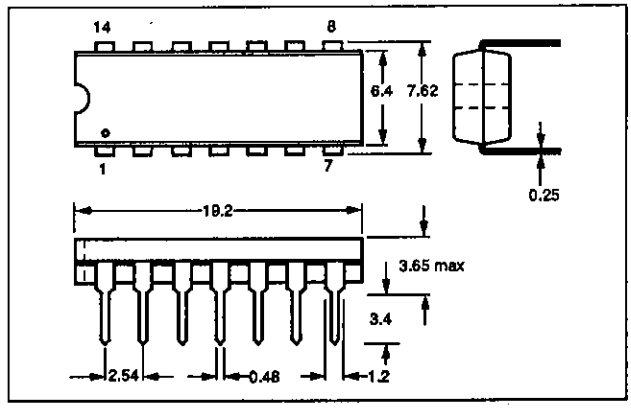
PINOUT



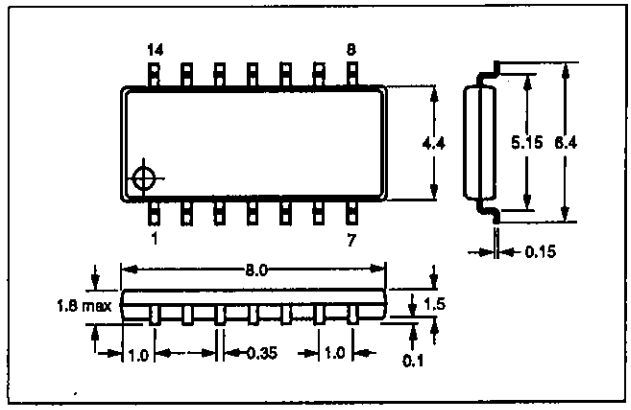
PACKAGE DIMENSIONS

Unit: mm

3003A-DIP14 (LC7215, LC7215F)



3111-MFP14S (LC7215FM)



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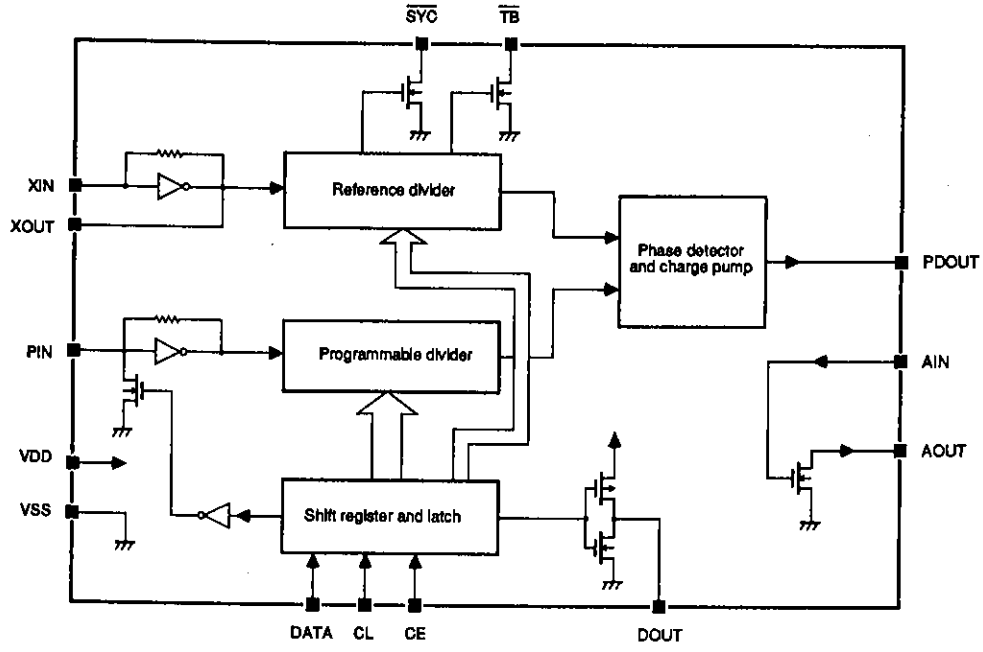
BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	XOUT	11.16 MHz crystal oscillator output
2	DOUT	Single-bit data output
3	$\overline{SYC}$	60 kHz controller clock output
4	$\overline{TB}$	8 Hz time-base output
5	DATA	Serial data input
6	CL	Clock input
7	CE	Chip enable
8	PIN	Local oscillator input
9	VDD	5 V supply
10	PDOUT	Charge pump output
11	AIN	Low-pass filter amplifier input
12	AOUT	Low-pass filter amplifier output
13	VSS	Ground
14	XIN	11.16 MHz crystal oscillator input

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD} max	–0.3 to 6.5	V
Input voltage range	V_{IN1}	–0.3 to V_{DD} + 0.3	V
Logic-level input voltage range	V_{IN2}	–0.3 to 6.5	V

Parameter	Symbol	Rating	Unit
Amplifier output current range	I_{OUT}	0 to 5	mA
Amplifier output voltage range	V_{OUT1}	–0.3 to 15	V
$\overline{SYC}$ and $\overline{TB}$ output voltage range	V_{OUT2}	–0.3 to 6.5	V
Output voltage range	V_{OUT3}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_d max	150	mW
Operating temperature range	Topr	–40 to 85	°C
Storage temperature range	T_{stg}	–55 to 125	°C

Recommended Operating Conditions

T_a = –40 to 85 deg. C, V_{SS} = 0 V. Values in parentheses are for the LC7215F and LC7215FM.

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD} op	3.0 (4.5) to 5.5 (5.5)	V

Electrical Characteristics

V_{DD} = 5 V, V_{SS} = 0 V, T_a = 25 deg. C unless otherwise noted. Values in parentheses are for LC7215F and LC7215FM.

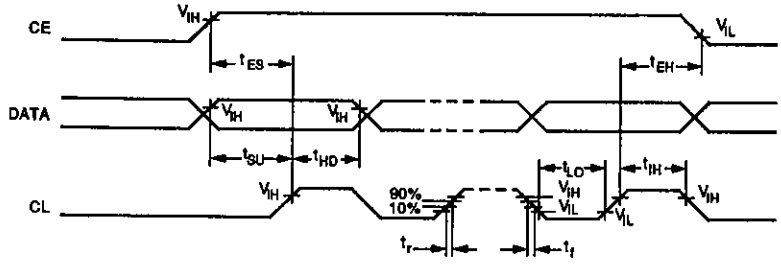
Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	f_{IN} = 13 MHz, S = 1. See note 1.	–	–	10	mA
		f_{IN} = 20 MHz, S = 1. See note 1.	–	–	(12)	
		f_{IN} = 2.5 MHz, S = 0. See note 1.	–	–	5	
		V_{DD} = 5.5 V, O = 0, P = 1. See note 1.	–	1.2	2.0	
		V_{DD} = 4.5 V, O = 0, P = 1. See note 2.	–	0.7	1.5	
		V_{DD} = 3.0 V, O = 0, P = 1. See note 2.	–	0.4	1.0	
Logic LOW-level input voltage	V_{IL}		0	–	0.5	V
Logic HIGH-level input voltage	V_{IH}		2.0	–	V_{DD}	V
LOW-level input currents	I_{IL1}	XIN: V_{IN} = V_{SS}	–	–	20	µA
	I_{IL2}	PIN: V_{IN} = V_{SS}	–	–	40	
	I_{IL3}	CE, CL, DATA: V_{IN} = V_{SS}	–	–	3.0	
	I_{IL4}	AIN: V_{IN} = V_{SS}	–	0.01	1.0	
HIGH-level input currents	I_{IH1}	XIN: V_{IN} = V_{DD}	–	–	20	µA
	I_{IH2}	PIN: V_{IN} = V_{DD}	–	–	40	
	I_{IH3}	CE, CL, DATA: V_{IN} = V_{DD}	–	–	3.0	
	I_{IH4}	AIN: V_{IN} = V_{DD}	–	0.01	1.0	

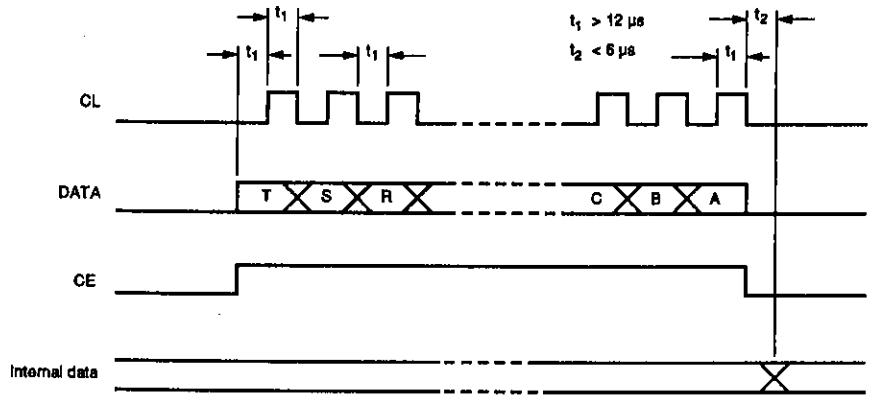
Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
LOW-level output voltages	V_{OL1}	DOUT: I_O = 1 mA	–	–	1.0	V
	V_{OL2}	PDOUT: I_O = 0.5 mA	–	–	1.0	
	V_{OL3}	XOUT: I_O = 0.1 mA	–	–	1.0	
	V_{OL4}	$\overline{SYC}$, $\overline{TB}$: I_O = 0.5 mA	–	–	1.0	
	V_{OL5}	AOUT: I_O = 1 mA	–	–	1.0	
HIGH-level output voltages	V_{OH1}	DOUT: I_O = 1 mA	V_{DD} – 1.0	–	–	V
	V_{OH2}	PDOUT: I_O = 0.5 mA	V_{DD} – 1.0	–	–	
	V_{OH3}	XOUT: I_O = 0.1 mA	V_{DD} – 1.0	–	–	
Amplifier output voltage	V_{OUT1}		–	–	13	V
$\overline{SYC}$ and $\overline{TB}$ output voltage	V_{OUT2}		–	–	5.5	
Input frequency	f_{IN}	Sine wave, capacitive coupling, S = 1	2.3 (2.3)	–	13 (20)	MHz
		Sine wave, capacitive coupling, S = 0	0.5	–	2.5	
Crystal oscillator frequency	f_{XTAL}	Cl ≤ 30 Ω	8.00	11.16	12.00	MHz
Local oscillator input amplitude	V_{IN}	Sine wave, capacitive coupling, S = 1	100	–	1,000	mV
		Sine wave, capacitive coupling, S = 0	100	–	1,000	
Output leakage currents	I_{OFF1}	$\overline{SYC}$, $\overline{TB}$: V_O = 13 V	–	–	3.0	μA
	I_{OFF2}	AOUT: V_O = 13 V	–	–	5.0	
Tristate output LOW-level leakage current	I_{OFFL}	PDOUT: V_O = V_{SS}	–	0.01	1.0	nA
Tristate output HIGH-level leakage current	I_{OFFH}	PDOUT: V_O = V_{DD}	–	0.01	1.0	nA

Notes

1. V_{IN1} = V_{IN2} = 100 mV. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are grounded and all other outputs are open.
2. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are connected to V_{DD} and all other outputs are open. Backup mode when PLL is halted.
3. S, O, and P are serial data control bits.
4. A capacitor of 1000 pF or more should be connected between V_{DD} and V_{SS} for supply decoupling.

Input Timing Characteristics





V_{IH} = 2.0 V to V_{DD}, V_{IL} = 0 to 0.5 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Enable setup time	t_{ES}	11.16 MHz crystal	12	–	–	µs
		Other crystal frequencies	124 / f_{XTAL}	–	–	
Enable hold time	t_{EH}	11.16 MHz crystal	12	–	–	µs
		Other crystal frequencies	124 / f_{XTAL}	–	–	
Data setup time	t_{SU}	11.16 MHz crystal	12	–	–	µs
		Other crystal frequencies	124 / f_{XTAL}	–	–	
Data hold time	t_{HD}	11.16 MHz crystal	12	–	–	µs
		Other crystal frequencies	124 / f_{XTAL}	–	–	
Clock LOW-level pulsewidth	t_{LO}	11.16 MHz crystal	12	–	–	µs
		Other crystal frequencies	124 / f_{XTAL}	–	–	
Clock HIGH-level pulsewidth	t_{HI}	11.16 MHz crystal	12	–	–	µs
		Other crystal frequencies	124 / f_{XTAL}	–	–	
Rise time	t_r		–	–	1	µs
Fall time	t_f		–	–	1	µs

FUNCTIONAL DESCRIPTION

Data Control

Data is clocked into a 20-bit shift register on the rising edge of the clock. When 20 bits have been received and CE goes LOW, the data is latched and input to the programmable divider and reference divider.

Data Format

The 20-bit input data word comprises a 14-bit programmable divider ratio code, a 2-bit mode selection code, a 2-bit reference frequency selection code, a 1-bit programmable divider sensitivity code and a 1-bit output selection code as shown in figure 1.

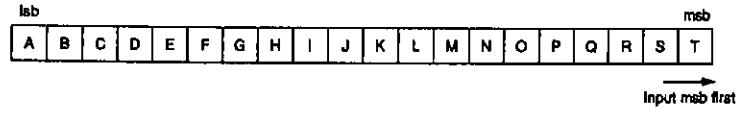


Figure 1. Data format

Operating Modes

Data bits O and P determine the operating mode of the synthesizer, and bit T, the 1-bit data output as shown in table 1.

Table 1. Mode selection

Mode	O	P	DOUT	$\overline{TB}$	Description
NOR1	0	0	T	8 Hz	Normal operation (with PLL operating)
NOR2	0	1	T	8 Hz	Normal operation (backup when PLL is halted)
TEST1	1	0	X	X	Device test mode
TEST2	1	1			

Programmable Divider

The programmable divider is set to the required ratio between the output frequency and the reference frequency. Data bits A to N determine the ratio as shown in figure 2. The output frequency is input from the voltage-controlled oscillator in the phase-locked loop.

Bit S selects the programmable divider's input frequency range. When S is 1, the frequency range is 2.3 to 13 MHz for the LC7215, and 2.3 to 20 MHz for the LC7215F and LC7215FM. When S is 0, the frequency range is 0.5 to 2.5 MHz.

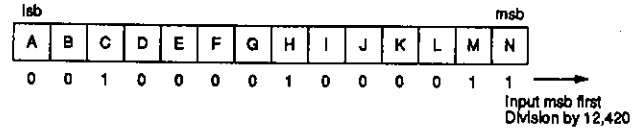


Figure 2. Divider ratio

Reference Divider

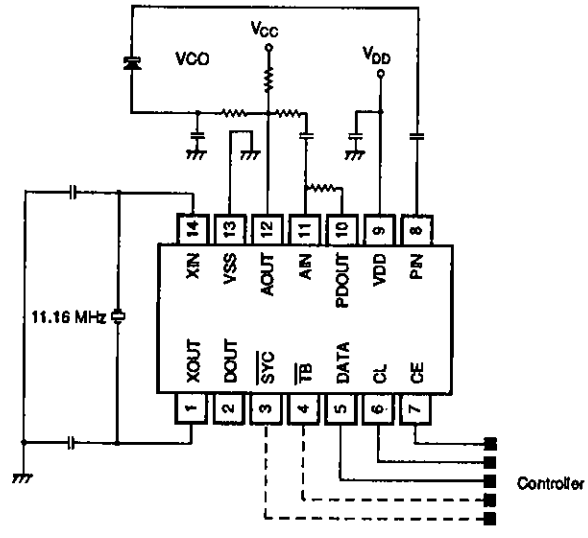
The reference divider sets the reference frequency in the phase-locked loop. Data bits Q and R determine the reference frequency as shown in table 2.

Table 2. Reference frequency

Q	R	Reference frequency
0	0	9 kHz
0	1	10 kHz
1	0	1 kHz
1	1	5 kHz

TYPICAL APPLICATIONS

VCO Components



Double-conversion Receiver