Description

The GM71V18163CJ-6E is the new generation dynamic RAM organized 1,048,576 x 16 bit. GM71V18163CJ-6E has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V18163CJ-6E offers Extended Data out(EDO) Mode as a high speed access mode. Multiplexed address inputs permit the GM71V18163CJ-6E to be packaged in standard 400 mil 42pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

Features

* 1,048,576 Words x 16 Bit Organization
* Extended Data Out Mode Capability
* Single Power Supply (3.3V+/-0.3V)
* Fast Access Time & Cycle Time

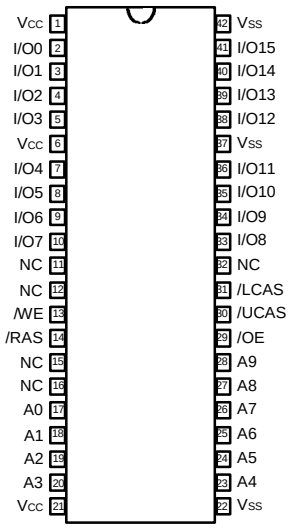
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
GM71V18163CJ-6E	60	15	104	25

* Low Power
  Active : 684/612/540mW (MAX)
  Standby : 7.2mW (CMOS level : MAX)
  0.83mW (L-version : MAX)
* /RAS Only Refresh, /CAS before /RAS Refresh, Hidden Refresh Capability
* All inputs and outputs TTL Compatible
* 1024 Refresh Cycles/16ms
* 2 CAS byte Control

Pin Configuration

(Top View) 42 SOJ



Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	/WE	Read/Write Enable
A0-A9	Refresh Address Inputs	/OE	Output Enable
I/O0-I/O15	Data-In/Out	V_{CC}	Power (+3.3V)
/RAS	Row Address Strobe	V_{SS}	Ground
/UCAS, /LCAS	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71V18163CJ –6E	60ns	400 Mil 42 Pin Plastic SOJ

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	-30 ~ 85	C
T_{STG}	Storage Temperature	-55 ~ 125	C
$V_{IN/OUT}$	Voltage on any Pin Relative to V_{SS}	-0.5 ~ Vcc+0.5 (<=4.6V(MAX))	V
V_{CC}	Supply Voltage Relative to V_{SS}	-0.5 ~ 4.6	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (TA = -30 ~ 85C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

Note: All voltage referred to Vss.
The supply voltage with all VCC pins must be on the same level. The supply voltage with all VSS pins must be on the same level.

Truth Table

/RAS	/LCAS	/UCAS	/WE	/OE	Output	Operation		Notes
H	D	D	D	D	Open	Standby		1,3
L	L	H	H	L	Valid	Lower byte	Read cycle	1,3
L	H	L	H	L	Valid	Upper byte		
L	L	L	H	L	Valid	Word		
L	L	H	L	D	Open	Lower byte	Early write cycle	1,2,3
L	H	L	L	D	Open	Upper byte		
L	L	L	L	D	Open	Word		
L	L	H	L	H	Undefined	Lower byte	Delayed Write cycle	1,2,3
L	H	L	L	H	Undefined	Upper byte		
L	L	L	L	H	Undefined	Word		
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify -write cycle	1,3
L	H	L	H to L	L to H	Valid	Upper byte		
L	L	L	H to L	L to H	Valid	Word		
H to L	H	L	D	D	Open	Word	CBR Refresh or Self Refresh (L-series)	1,3
H to L	L	H	D	D	Open	Word		
H to L	L	L	D	D	Open	Word		
L	H	H	D	D	Open	Word	/RAS-only Refresh cycle	1,3
L	L	L	H	H	Open	Read cycle (Output disabled)		1,3

Notes: 1. H: High (inactive) L: Low(active) D: H or L
2. t_{WCS} >= 0ns Early write cycle
t_{WCS} <= 0ns Delayed write cycle
3. Mode is determined by the OR function of the /UCAS and /LCAS. (Mode is set by earliest of /UCAS and /LCAS active edge and reset by the latest of /UCAS and /LCAS inactive edge.) However write OPERATION and output High-Z control are done independently by each /UCAS, /LCAS.
ex) if /RAS = H to L, /UCAS = H, /LCAS = L, then /CAS-before-/RAS refresh cycle is selected.

DC Electrical Characteristics (VCC = 3.3V+/-0.3V, Vss = 0V, TA = -30 ~ 85C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current (/RAS, /UCAS or /LCAS Cycling: t_{RC} = t_{RC} min)	60ns	-	170	mA	1, 2
I_{CC2}	Standby Current (TTL) Power Supply Standby Current (/RAS, /UCAS, /LCAS = V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode (t_{RC} = t_{RC} min)	60ns	-	170	mA	2
I_{CC4}	EDO Page Mode Current Average Power Supply Current EDO Page Mode (t_{HPC} = t_{HPC} min)	60ns	-	165	mA	1, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current (/RAS, /UCAS or /LCAS >= V_{CC} - 0.2V, D_{OUT} = High-Z)		- -	1 150	mA uA	 5
I_{CC6}	/CAS-before-/RAS Refresh Current (t_{RC} = t_{RC} min)	60ns	-	170	mA	
I_{CC7}	Battery Back Up Operating Current(Standby with CBR Ref.) (CBR refresh, t_{RC}=125us, t_{RAS}<=0.3us, D_{OUT}=High-Z, CMOS interface)		-	400	uA	4,5
I_{CC8}	Standby Current /RAS = V_{IH} /UCAS, /LCAS = V_{IL} D_{OUT} = Enable		-	5	mA	1
I_{CC9}	Self-Refresh Mode Current (/RAS, /UCAS or /LCAS<=0.2V, D_{OUT}=High-Z)		-	250	uA	5
$I_{L(I)}$	Input Leakage Current Any Input (0V<=V_{IN}<= 4.6V)		-10	10	uA	
$I_{L(O)}$	Output Leakage Current (D_{OUT} is Disabled, 0V<=V_{OUT}<= 4.6V)		-10	10	uA	

Note: 1. I_{CC} depends on output load condition when the device is selected.
I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while /RAS = V_{IL}.
3. Address can be changed once or less while /LCAS and /UCAS = V_{IH}.
4. /UCAS = L (<=0.2) and /LCAS = L (<=0.2) while /RAS = L (<=0.2).

Capacitance (VCC = 3.3V+/-0.3V, TA = 25C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. /UCAS and /LCAS = V_{IH} to disable D_{OUT}.

AC Characteristics (VCC = 3.3V+/-0.3V, TA = -30 ~ +85C, Note 1, 2, 18, 19, 20)

Test Conditions

Input rise and fall times : 2 ns
Input levels : V_{IL} = 0V, V_{IH} = 3V
Input timing reference levels : 0.8V, 2.0V
Output timing reference levels : 0.8V, 2.0V
Output load : 1TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71V18163CJ-6E		Unit	Note
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	-	ns	
t_{RP}	/RAS Precharge Time	40	-	ns	
t_{CP}	/CAS Precharge Time	10	-	ns	
t_{RAS}	/RAS Pulse Width	60	10,000	ns	
t_{CAS}	/CAS Pulse Width	10	10,000	ns	
t_{ASR}	Row Address Set up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	ns	21
t_{CAH}	Column Address Hold Time	10	-	ns	21
t_{RCD}	/RAS to /CAS Delay Time	14	45	ns	3
t_{RAD}	/RAS to Column Address Delay Time	12	30	ns	4
t_{RSH}	/RAS Hold Time	13	-	ns	
t_{CSH}	/CAS Hold Time	40	-	ns	23
t_{CRP}	/CAS to /RAS Precharge Time	5	-	ns	22
t_{ODD}	/OE to D_{IN} Delay Time	15	-	ns	5
t_{DZO}	/OE Delay Time from D_{IN}	0	-	ns	6
t_{DZC}	/CAS Delay Time from D_{IN}	0	-	ns	6
t_T	Transition Time (Rise and Fall)	2	50	ns	7

Read Cycle

Symbol	Parameter	GM71V18163CJ-6E		Unit	Note
		Min	Max		
t_{RAC}	Access Time from /RAS	-	60	ns	8,9
t_{CAC}	Access Time from /CAS	-	15	ns	9,10,17
t_{AA}	Access Time from Address	-	30	ns	9,11,17
t_{OAC}	Access Time from /OE	-	15	ns	9
t_{RCS}	Read Command Setup Time	0	-	ns	21
t_{RCH}	Read Command Hold Time to /CAS	0	-	ns	12,22
t_{RRH}	Read Command Hold Time to /RAS	5	-	ns	12
t_{RAL}	Column Address to /RAS Lead Time	30	-	ns	
t_{CAL}	Column Address to /CAS Lead Time	18	-	ns	
t_{CLZ}	/CAS to Output in Low-Z	0	-	ns	
t_{OH}	Output Data Hold Time	3	-	ns	27
t_{OHO}	Output Data Hold Time from /OE	3	-	ns	
t_{OFF}	Output Buffer Turn-off Time	-	15	ns	13,27
t_{OEZ}	Output Buffer Turn-off Time to /OE	-	15	ns	13
t_{CDD}	/CAS to D_{IN} Delay Time	15	-	ns	5
t_{RCHR}	Read Command Hold Time from /RAS	60	-	ns	
t_{OHR}	Output Data hold Time from /RAS	3	-	ns	27
t_{OFR}	Output Buffer turn off to /RAS	-	15	ns	27
t_{WEZ}	Output Buffer turn off to /WE	-	15	ns	
t_{WDD}	/WE to D_{IN} Delay Time	15	-	ns	
t_{RDD}	/RAS to D_{IN} Delay Time	15	-	ns	

Write Cycle

Symbol	Parameter	GM71V18163CJ-6E		Unit	Note
		Min	Max		
t_{WCS}	Write Command Setup Time	0	-	ns	14,21
t_{WCH}	Write Command Hold Time	10	-	ns	21
t_{WP}	Write Command Pulse Width	10	-	ns	
t_{RWL}	Write Command to /RAS Lead Time	10	-	ns	
t_{CWL}	Write Command to /CAS Lead Time	10	-	ns	23
t_{DS}	Data-in Setup Time	0	-	ns	15,23
t_{DH}	Data-in Hold Time	10	-	ns	15,23

Read- Modify-Write Cycle

Symbol	Parameter	GM71V18163CJ-6E		Unit	Note
		Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	136	-	ns	
t_{RWD}	/RAS to /WE Delay Time	79	-	ns	14
t_{CWD}	/CAS to /WE Delay Time	34	-	ns	14
t_{AWD}	Column Address to /WE Delay Time	49	-	ns	14
t_{OEH}	/OE Hold Time from /WE	15	-	ns	

Refresh Cycle

Symbol	Parameter	GM71V18163CJ-6E		Unit	Note
		Min	Max		
t_{CSR}	/CAS Setup Time (/CAS-before-/RAS Refresh Cycle)	5	-	ns	21
t_{CHR}	/CAS Hold Time (/CAS-before-/RAS Refresh Cycle)	10	-	ns	22
t_{RPC}	/RAS Precharge to /CAS Hold Time	5	-	ns	21

EDO Page Mode Cycle

Symbol	Parameter	GM71V18163CJ-6E		Unit	Note
		Min	Max		
t_{HPC}	EDO Page Mode Cycle Time	25	-	ns	25
t_{RASP}	EDO Page Mode /RAS Pulse Width	-	100,000	ns	16
t_{ACP}	Access Time from /CAS Precharge	-	35	ns	9,17,22
t_{RHCP}	/RAS Hold Time from /CAS Precharge	35	-	ns	
t_{DOH}	Output data Hold Time from /CAS low	3	-	ns	9
t_{COL}	/CAS Hold Time referred /OE	10	-	ns	
t_{COP}	/CAS to OE Setup Time	5	-	ns	
t_{RCHP}	Read command Hold Time from /CAS Precharge	35	-	ns	

EDO Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71V18163CJ-6E		Unit	Note
		Min	Max		
t_{HPRWC}	EDO Page Mode Read-Modify-Write Cycle Time	68	-	ns	
t_{CPW}	/WE Delay Time from /CAS Precharge	54	-	ns	14,22

Refresh

Symbol	Parameter	GM71V18163CJ-6E		Unit	Note
		Min	Max		
t_{REF}	Refresh period	-	16	ms	1024 cycles

Notes :

1. AC measurements assume t_T = 2 ns.

2. An initial pause of 200us is required after power followed by a minimum of eight initialization cycles (any combination of cycles containing /RAS-only refresh or /CAS-before-/RAS refresh).

3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

5. Either t_{ODD} or t_{CDD} must be satisfied.

6. Either t_{DZO} or t_{DZC} must be satisfied.

7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

8. Assumes that t_{RCD} <= t_{RCD} (max) and t_{RAD} <= t_{RAD} (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

9. Measured with a load circuit equivalent to 1TTL loads and 100pF.

10. Assumes that t_{RCD} >= t_{RCD} (max) and t_{RAD} <= t_{RAD} (max).

11. Assumes that t_{RCD} <= t_{RCD} (max) and t_{RAD} >= t_{RAD} (max).

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.

13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t_{WCS} >= t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle; if t_{RWD}>=t_{RWD}(min), t_{CWD}>=t_{CWD}(min), and t_{AWD}>=t_{AWD}(min), or t_{CWD}>=t_{CWD}(min) t_{AWD} >= t_{AWD} (min) and t_{CPW} >= t_{CPW} (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

15. These parameters are referred to /UCAS and /LCAS leading edge in early write cycles and to /WE leading edge in delayed write or read-modify-write cycles.

16. t_{RASP} defines /RAS pulse width in EDO mode cycles.

17. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.

18. In delayed write or read-modify-write cycles, /OE must disable output buffer prior to applying data to the device. After /RAS is reset, if t_{OEH}>=t_{CWL}, the I/O pin will remain open circuit (high impedance): if t_{OEH}<=t_{CWL}, invalid data will be out at each I/O.

19. When both /LCAS and /UCAS go low at the same time, all 16-bits data are written into the device. /LCAS and /UCAS cannot be staggered within the same write/read cycles.

20. All the Vcc and Vss pins shall be supplied with the same voltages.

21. t_{ASC}, t_{CAH}, t_{RCS}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of /UCAS or /LCAS.

22. t_{CRP}, t_{CHR}, t_{RCH}, t_{ACP} and t_{CPW} are determined by the later rising edge of /UCAS or /LCAS.

23. t_{CWL}, t_{DH}, t_{DS} and t_{CHS} should be satisfied by both /UCAS and /LCAS.

24. t_{CP} is determined by the time that both /UCAS and /LCAS are high.

25. t_{HPC}(min) can be achieved during a series of EDO page made write cycles or EDO mode write cycles. It both write and read operation are mixed in a EDO mode RAS cycle(EDO mode mix cycle (1),(2)) minimum Value of CAS cycle (t_{CAS}+t_{CP}+2tT) becomes greater than the specified t_{HPC} (min) value. The value of CAS cycle time of mixed EDO mode is shown in EDO mode mix cycle (1) and (2).

26. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time , generally it causes large Vcc/Vss line noise, which causes to degrade V_{IH} min/V_{IL} max level.

27. Data output turns off and becomes high impedance from later rising edge of RAS and CAS. Hold time and turn off time are specified by the timing specification of later rising edge of RAS and CAS between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.

28. EDO Hi-Z control by OE or WE. OE rising edge disables data outputs.
When OE goes high during CAS high, the data will not come out until next CAS access.
When WE goes low during CAS high, the data will not come out until next CAS access.

29. Please do not use t_{RASS} timing, 10us<=t_{RASS}<=100us. During this period, the device is in transition state from normal operation mode to self refresh mode. If t_{RASS}>=100us, then RAS

30. H or L (H : V_{IH}(min) <= V_{IN} <= V_{IH}(max), L : V_{IL}(min) <= V_{IN} <= V_{IL}(max))

Package Dimension

42 SOJ

Unit: Inches (mm)