# CMOS 8-bit Single-chip Microcomputer

Description

The CXP85112B/85116B, CXP85220A/85224A/85228A/85232A is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, vector interruption, on-screen display function, I²C bus interface, PWM generator, remote control reception circuit, HSYNC counter, power source frequency counter and watch dog timer besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP85112B/85116B, CXP85220A/85224A/85228A/85232A also provides a power-on reset function and a sleep function that enables lower power consumption.

64 pin SDIP (Plastic)   64 pin QFP (Plastic)
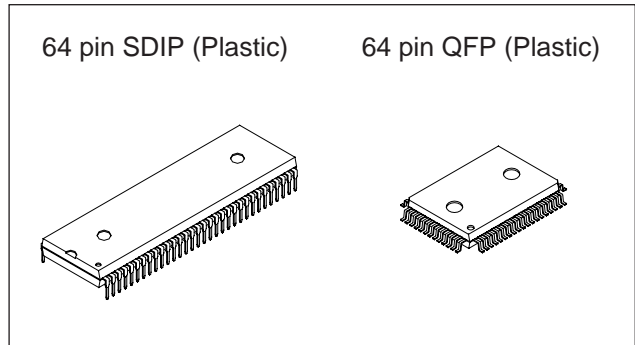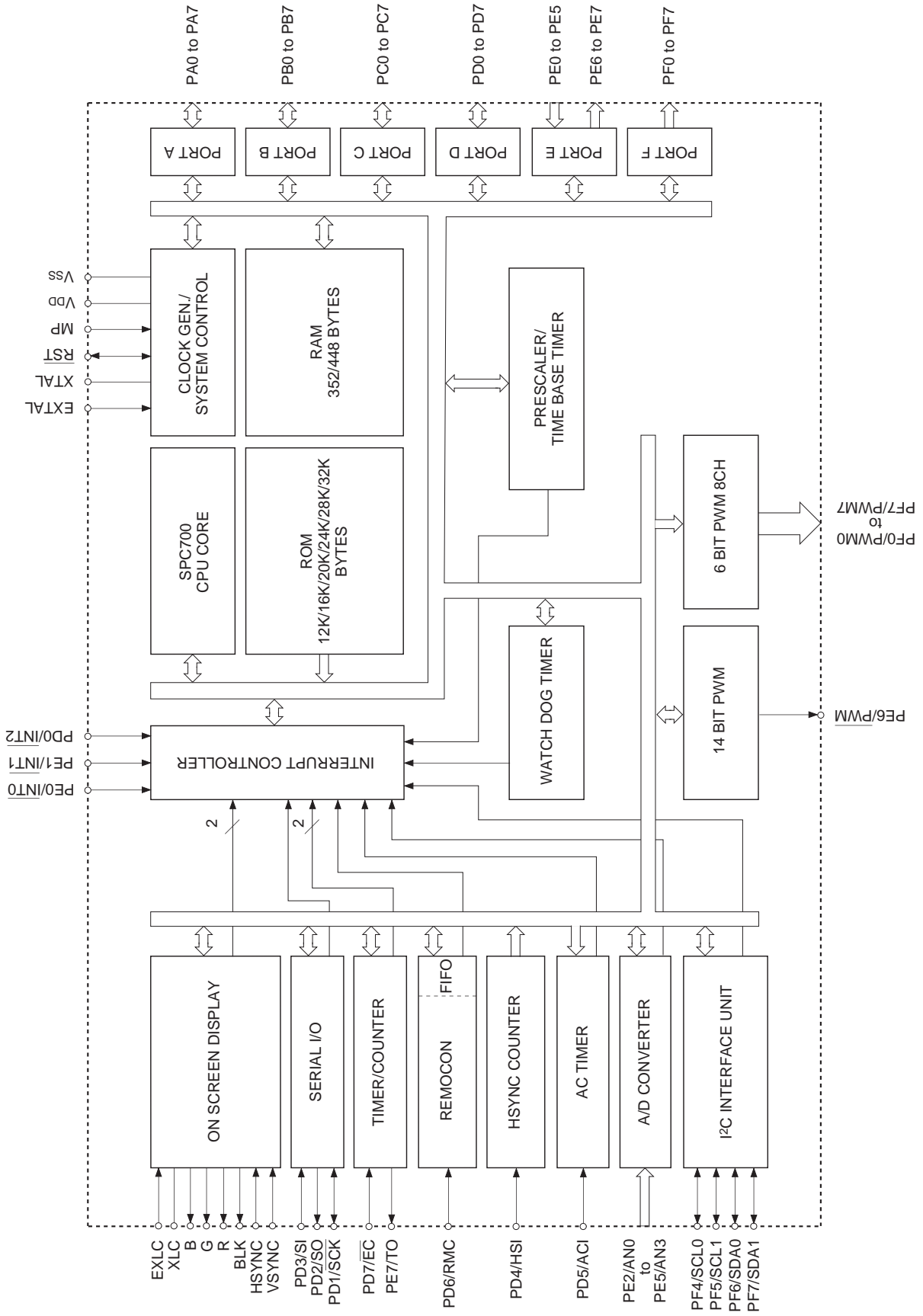
Structure
Silicon gate CMOS IC

Features

- Wide-range instruction system (213 instructions) to cover various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle   1µs at 4MHz operation
- Incorporated ROM capacity   12K bytes (CXP85112B)
                                        16K bytes (CXP85116B)
                                        20K bytes (CXP85220A)
                                        24K bytes (CXP85224A)
                                        28K bytes (CXP85228A)
                                        32K bytes (CXP85232A)
- Incorporated RAM capacity   352 bytes (CXP85112B/85116B)
                                        448 bytes (CXP85220A/85224A/85228A/85232A)
- Peripheral functions
  — On-screen display function 12×16 dots, 128 types
                                        21 words $\times$ 4 lines (more than 4 lines possible)
                                        Double scan mode compatible, jitter elimination circuit
  — I²C bus interface
  — PWM output   14 bits, 1 channel
                                        6 bits, 8 channels
  — Remote control reception circuit   8-bit pulse measurement counter with on-chip 6-stage FIFO
  — A/D converter   4 bits, 4channels, successive approximation method
                                        (Conversion time of 40µs/4MHz)
  — HSYNC counter
  — Power supply frequency counter
  — Watch dog timer
  — Serial I/O   8-bit clock synchronization
  — Timer   8-bit timer, 8-bit timer/counter, 19-bit time base timer
- Interruption   14 factors, 14 vectors, multi-interruption possible
- Standby mode   Sleep
- Package   64-pin plastic SDIP/QFP
- Piggyback/evaluation chip   CXP85100A, CXP85190 (Custom font compatible)
                                        CXP85200A, CXP85290 (Custom font compatible)
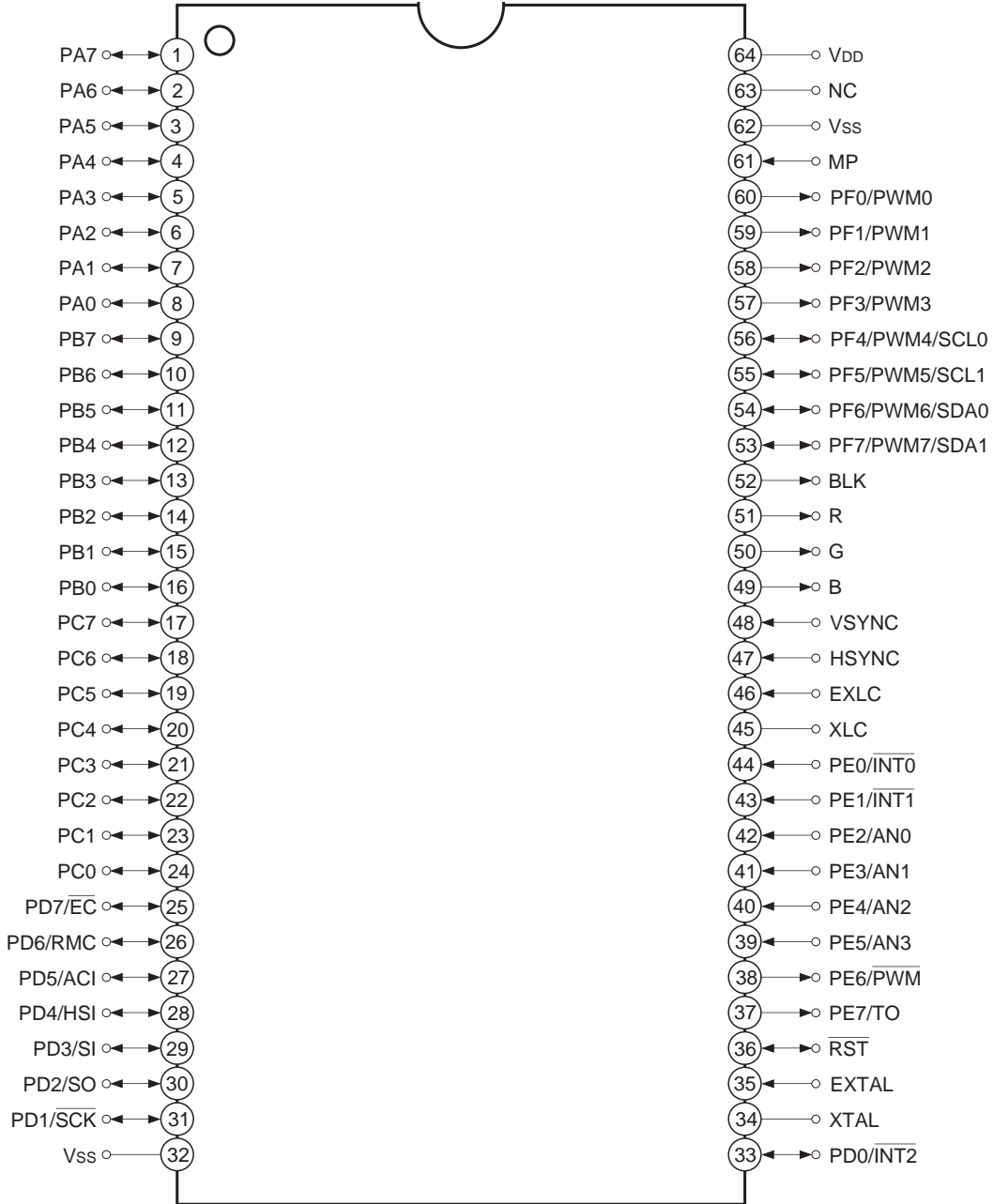
Purchase of Sony's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

E93Z17B86

Block Diagram

Pin Assignment 1 (Top View) 64 pin SDIP Package

Pin	Left		Pin	Right
1	PA7		64	VDD
2	PA6		63	NC
3	PA5		62	Vss
4	PA4		61	MP
5	PA3		60	PF0/PWM0
6	PA2		59	PF1/PWM1
7	PA1		58	PF2/PWM2
8	PA0		57	PF3/PWM3
9	PB7		56	PF4/PWM4/SCL0
10	PB6		55	PF5/PWM5/SCL1
11	PB5		54	PF6/PWM6/SDA0
12	PB4		53	PF7/PWM7/SDA1
13	PB3		52	BLK
14	PB2		51	R
15	PB1		50	G
16	PB0		49	B
17	PC7		48	VSYNC
18	PC6		47	HSYNC
19	PC5		46	EXLC
20	PC4		45	XLC
21	PC3		44	PE0/$\overline{\text{INT0}}$
22	PC2		43	PE1/$\overline{\text{INT1}}$
23	PC1		42	PE2/AN0
24	PC0		41	PE3/AN1
25	PD7/$\overline{\text{EC}}$		40	PE4/AN2
26	PD6/RMC		39	PE5/AN3
27	PD5/ACI		38	PE6/$\overline{\text{PWM}}$
28	PD4/HSI		37	PE7/TO
29	PD3/SI		36	$\overline{\text{RST}}$
30	PD2/SO		35	EXTAL
31	PD1/$\overline{\text{SCK}}$		34	XTAL
32	Vss		33	PD0/$\overline{\text{INT2}}$

Note) 1. NC (Pin 63) must be connected to VDD.

2. Vss for both Pins 32 and 62 must be grounded.

3. MP (Pin 61) must be connected to GND.
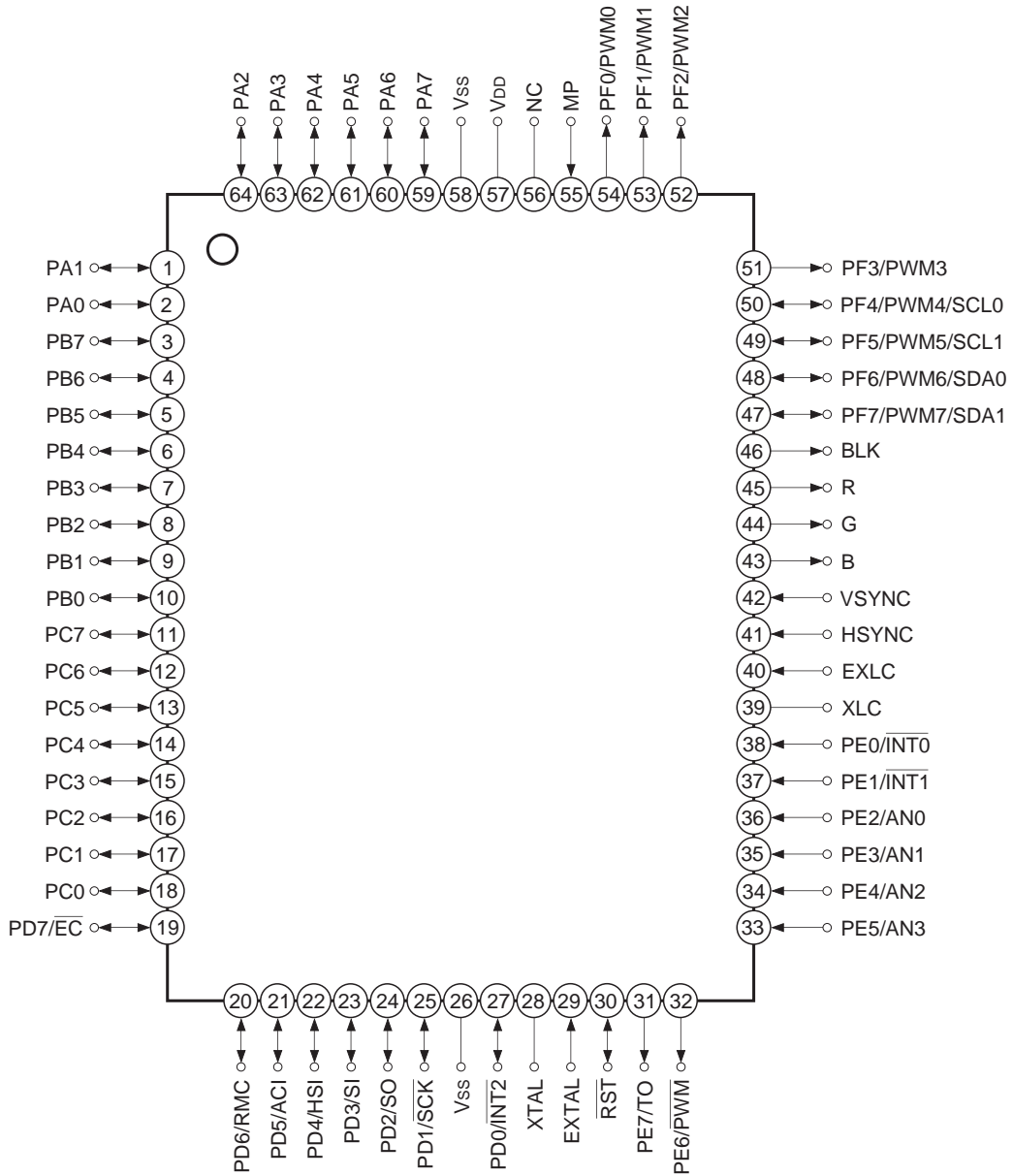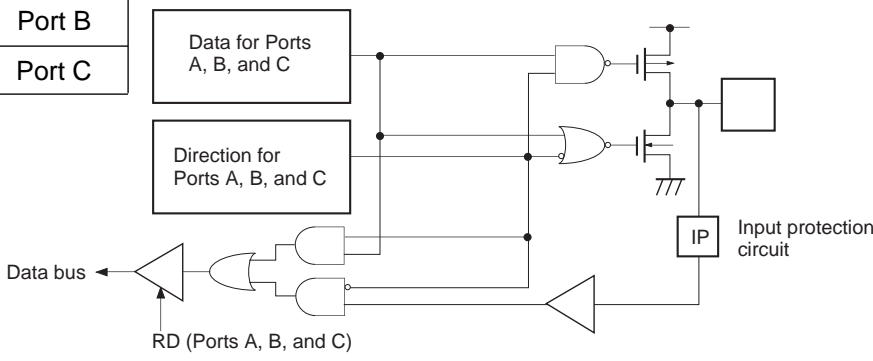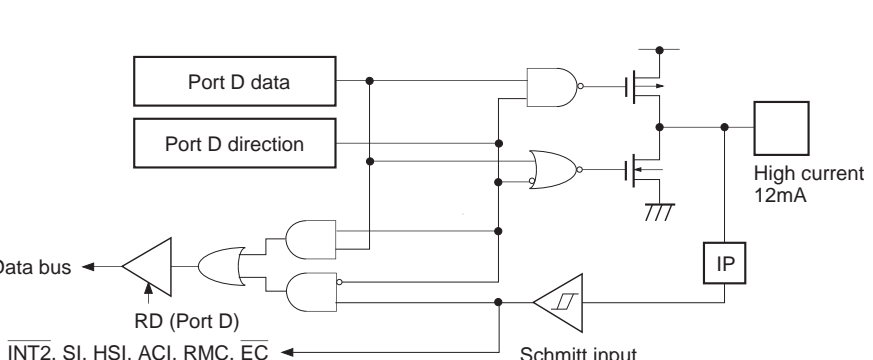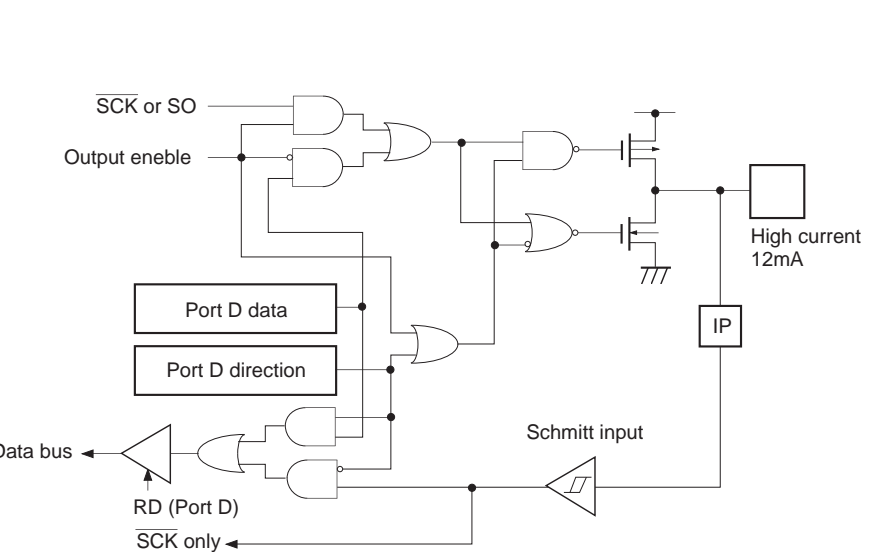
Pin Assignment 2 (Top View) 64 pin QFP Package

Note) 1. NC (Pin 56) must be connected to V_{DD}.

2. Vss for both Pins 26 and 58 must be grounded.
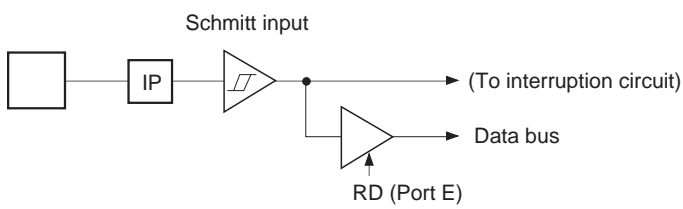
3. MP (Pin 55) must be connected to GND.
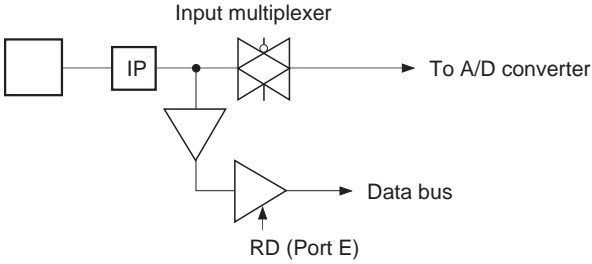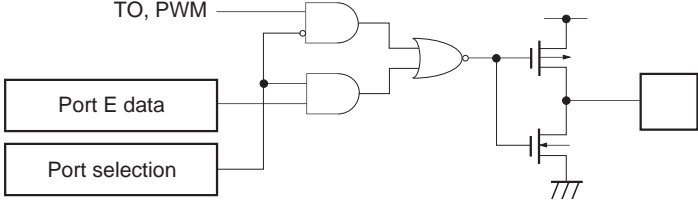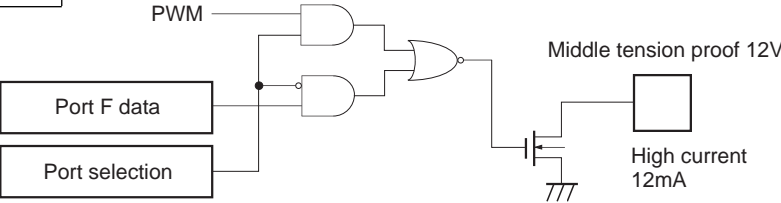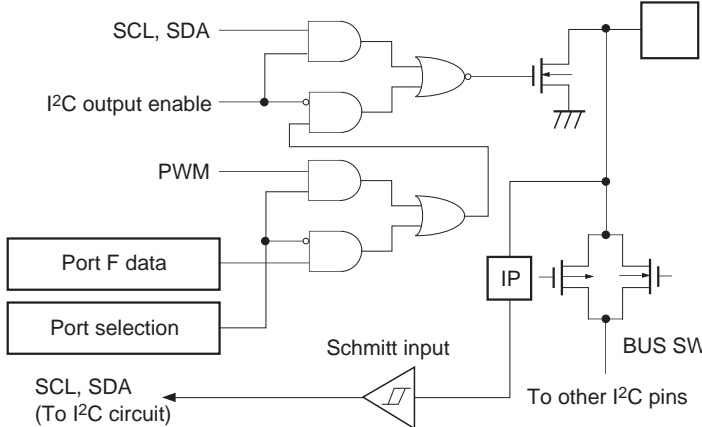
Pin Description
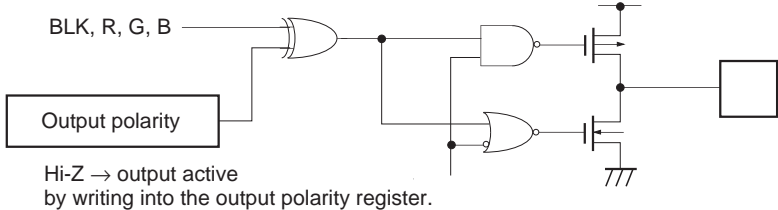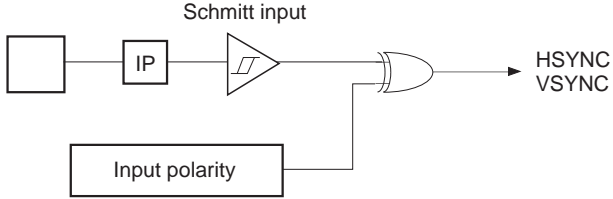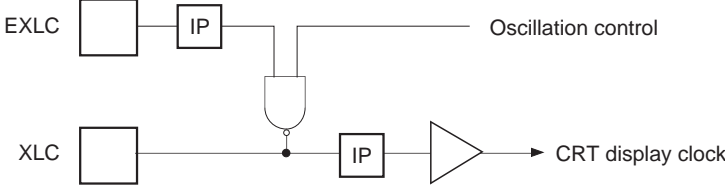
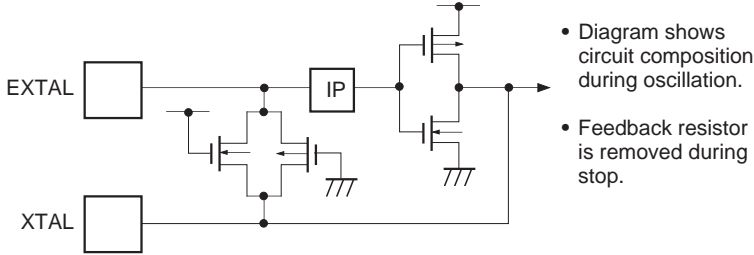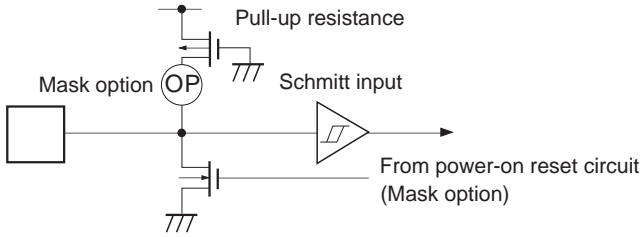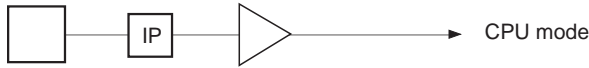| Symbol	I/O	Description	
PA0 to PA7	I/O	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PD0/$\overline{INT2}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set ina a unit of single bits. Capable of driving 12mA sink current. (8 pins)	External interruption request input. Active at falling edge.
PD1/$\overline{SCK}$	I/O/I/O		Serial clock I/O.
PD2/SO	I/O/Output		Serial data output.
PD3/SI	I/O/Input		Serial data input.
PD4/HSI	I/O/Input		HSYNC counter input.
PD5/ACI	I/O/Input		Input for power supply frequency counter.
PD6/RMC	I/O/Input		Input for remote control reception circuit.
PD7/$\overline{EC}$	I/O/Input		External event input for timer/counter.
PE0/$\overline{INT0}$ PE1/$\overline{INT1}$	Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs.	External interruption request inputs. Active at falling edge. (2 pins)
PE2/AN0 to PE5/AN3	Input/Input		Analog inputs for A/D converter. (4 pins)
PE6/$\overline{PWM}$	Output/Output		14-bit PWM output. (CMOS output)
PE7/TO	Output/Output		Rectangular waveform output for Timer 1. (Duty output 50%)
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port, operating as N-ch open drain output for high current (12mA). Lower 4 bits are medium voltage drive outputs (12V), upper 4bits are 5V drive outputs. (8 pins)	6-bit PWM outputs. (8 pins)
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1	Output/Output/I/O		Transfer clock I/Os for I^{2}C bus interface.
PF6/PWM6/ SDA0 PF7/PWM7/ SDA1	Output/Output/I/O		Transfer data I/Os for I^{2}C data bus.
R, G, B, BLK	Output	4-bit outputs for CRT display.	
HSYNC	Input	Horizontal synchronizing signal input for CRT display.	
VSYNC	Input	Vertical synchronizing signal input for CRT display.	

Symbol	I/O	Description
EXLC	Input	Clock oscillation I/Os for CRT display.
XLC	Output	Oscillation frequency is set using the external L and C.
EXTAL	Input	Crystai connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.
XTAL	Output	
$\overline{\text{RST}}$	I/O	Low-level active, system reset. $\overline{\text{RST}}$ is an I/O, from whlch Low level is output when the built-in power-on reset function is activated at the rise of power on. (Mask option)
MP	Input	Microprocessor mode input. For this device, this pin must be grounded.
V_{DD}		Vcc supply.
Vss		GND. Both Vss must be grounded.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0 to PA7 PB0 to PB7 PC0 to PC7 24 pins	**Port A** **Port B** **Port C** Data for Ports A, B, and C Direction for Ports A, B, and C Data bus RD (Ports A, B, and C) IP Input protection circuit	Hi-Z
PD0/$\overline{\text{INT2}}$ PD3/SI PD4/HSI PD5/ACI PD6/RMC PD7/$\overline{\text{EC}}$ 6 pins	**Port D** Port D data Port D direction Data bus RD (Port D) $\overline{\text{INT2}}$, SI, HSI, ACI, RMC, $\overline{\text{EC}}$ High current 12mA IP Schmitt input	Hi-Z
PD1/$\overline{\text{SCK}}$ PD2/SO 2 pins	**Port D** $\overline{\text{SCK}}$ or SO Output eneble Port D data Port D direction Data bus RD (Port D) $\overline{\text{SCK}}$ only High current 12mA IP Schmitt input	Hi-Z

Pin	Circuit format	When reset
PE0/$\overline{INT0}$ PE1/$\overline{INT1}$ 2 pins	**Port E** Schmitt input IP → (To interruption circuit) Data bus RD (Port E)	Hi-Z
PE2/AN0 to PE5/AN3 4 pins	**Port E** Input multiplexer IP → To A/D converter Data bus RD (Port E)	Hi-Z
PE6/$\overline{PWM}$ PE7/TO 2 pins	**Port E** TO, $\overline{PWM}$ Port E data Port selection	High level
PF0/PWM0 to PF3/PWM3 4 pins	**Port F** PWM Port F data Port selection Middle tension proof 12V High current 12mA	Hi-Z
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1 PF6/PWM6/ SDA0 PF7/PWM7/ SDA1 4 pins	**Port F** SCL, SDA I^{2}C output enable PWM Port F data Port selection Schmitt input SCL, SDA (To I^{2}C circuit) IP BUS SW To other I^{2}C pins	Hi-Z

Pin	Circuit format	When reset
BLK R G B 4 pins	BLK, R, G, B ──── [XOR] ──── [NAND] ──── Output polarity Hi-Z → output active by writing into the output polarity register.	Hi-Z
HSYNC VSYNC 2 pins	Schmitt input [ ]── IP ── [▷] ── [XOR] ──→ HSYNC VSYNC Input polarity	Hi-Z
EXLC XLC 2 pins	EXLC [ ]── IP ──── Oscillation control XLC [ ]──── IP ── [▷] ──→ CRT display clock	Oscillation terminated
EXTAL XTAL 2 pins	EXTAL [ ]──── IP ──── XTAL [ ]──── • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
$\overline{RST}$ 1 pin	Pull-up resistance Mask option (OP) Schmitt input [ ]──── [▷] ──→ From power-on reset circuit (Mask option)	Low level
MP 1 pin	[ ]── IP ── [▷] ──→ CPU mode	Hi-Z

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	−0.3 to +7.0	V	
Input voltage	V_{IN}	−0.3 to +7.0[*1]	V	
Output voltage	V_{OUT}	−0.3 to +7.0[*1]	V	
Medium voltage drive output voltage	V_{OUTP}	−0.3 to +15.0	V	Pins PF0 to PF3
High level output current	I_{OH}	−5	mA	
High level total output current	ΣI_{OH}	−50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	Excludes high current outputs
	I_{OLC}	20	mA	High current outputs[*2]
Low level total output current	ΣI_{OL}	130	mA	Total for all output pins
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +150	°C	
Allowable power dissipation	P_D	1000	mW	SDIP
		600	mW	QFP

[*1] V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

[*2] The high current operation transistor is the N-ch transistor of PD and PF0 to PF3.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions.

Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range
		3.5	5.5	V	Low-speed mode guaranteed operation range[*1]
		2.5	5.5	V	Guaranteed data hold range during stop
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	Includes I²C Schmitt input[*2]
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	CMOS Schmitt input[*3]
	V_{IHEX}	$V_{DD} − 0.4$	$V_{DD} + 0.3$	V	EXTAL[*4]
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	Includes I²C Schmitt input[*2]
	V_{ILS}	0	$0.2V_{DD}$	V	CMOS Schmitt input[*3]
	V_{ILEX}	−0.3	0.4	V	EXTAL[*4]
Operating temperature	T_{opr}	−20	+75	°C	

[*1] Specifies only for 1/16 frequency demultiplication mode and sleep mode.

[*2] Value for each pin of normal input ports (PA, PB, PC, PE2 to PE5), PF4 to PF7, and MP.

[*3] Value of the following pins: PD0/$\overline{INT2}$, PD1/$\overline{SCK}$, PD2, PD3/SI, PD4/HSI, PD5/ACI, PD6/RMC, PD7/$\overline{EC}$, PE0/$\overline{INT0}$, PE1/$\overline{INT1}$, HSYNC, VSYNC, $\overline{RST}$.

[*4] Specifies only during external clock input.

Electrical Characteristics

DC Characteristics (Ta = −20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V_{OH}	PA to PD, PE6, PE7, R, G, B, BLK	V_{DD} = 4.5V, I_{OH} = −0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = −1.2mA	3.5			V
Low level output current	V_{OL}	PA to PD, PE6, PE7, R, G, B, BLK, $\overline{PF0}$ to PF3, $\overline{RST}$[*1]	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PF0 to PF3	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{IHL}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.5		−40	µA
	I_{ILR}	$\overline{RST}$[*2]	V_{DD} = 5.5V, V_{IL} = 0.4V	−1.5		−400	µA
I/O leakage current	I_{IZ}	PA to PE, HSYNC, VSYNC, R, G, B, BLK, $\overline{RST}$[*2], MP	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-ch Tr in off state)	I_{LOH}	PF0 to PF3	V_{DD} = 5.5V, V_{OH} = 12.0V			50	µA
		PF4 to PF7	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
Impedance connected to I2C bus switch (output Tr in off state)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω
Power supply current	I_{DD}	V_{DD}[*3]	Operation mode[*3] (1/2 frequency demultiplier clock) 4MHz crystal oscillation (C_1 = C_2 = 22pF) All outputs open	8		20	mA
	I_{DDSL}		Sleep mode		0.5	2	mA
	I_{DDST}		Stop mode[*4]	—	—	—	µA
Input capacity	C_{IN}	Pins other than V_{DD} and Vss	Clock 1MHz 0V for all pins excluding		10	20	pF

[*1] $\overline{RST}$ specifies only when the power-on reset circuit has been selected throughn mask option.

[*2] $\overline{RST}$ specifies input current when the pull-up resistance has been selected; leakage current when no resistance has been selected.

[*3] Specifies only when the oscillatlon of OSD has been terminated.

[*4] This device does not enter the stop mode.

AC Characteristics

(1) Clock timing   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	3.5	4.5	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	100		ns
System clock input rise time, fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive		200	ns
Event clock input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	t_{sys} + 50[1]		ns
Event count input clock rise time, fall time	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3		20	ms

[1] t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FE$_H$).

t_{sys} [ns] = 2000/f_c (upper two bits = "00"), 4000/f_c (upper two bits = "01"), 16000/f_c (upper two bits = "11")
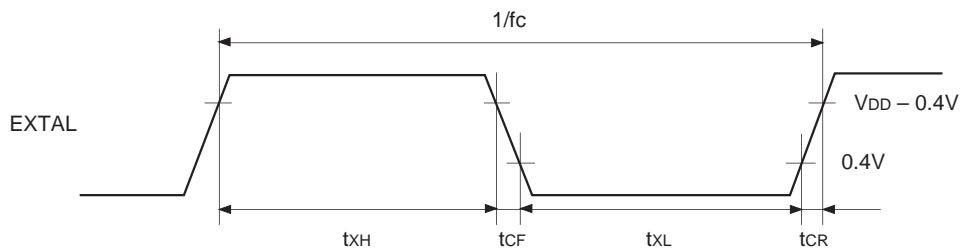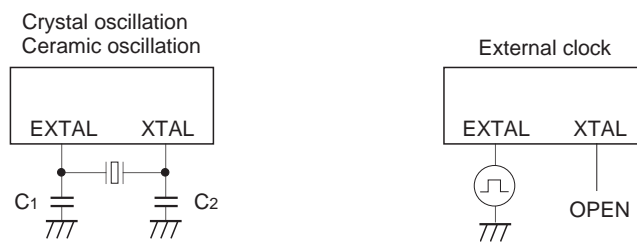

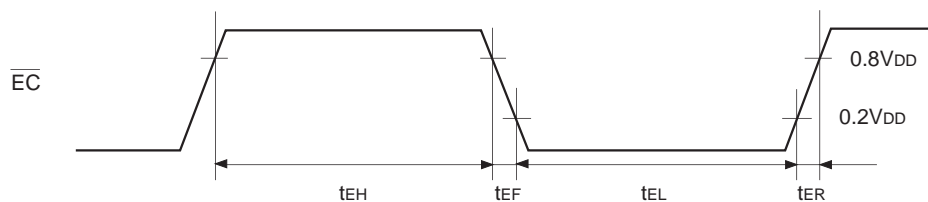**Fig. 1. Clock timing**

Fig. 2. Clock applying condition

Fig. 3. Event count clock timing

(2) Serial transfer   (Ta = −20 to +75°C, V$_{DD}$ = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t$_{KCY}$	$\overline{SCK}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level widths	t$_{KH}$ t$_{KL}$	$\overline{SCK}$	$\overline{SCK}$ input mode	400		ns
			$\overline{SCK}$ output mode	4000/fc − 50		ns
SI input setup time (for $\overline{SCK}$ ↑)	t$_{SIK}$	SI	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}$ ↑)	t$_{KSI}$	SI	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t$_{KSO}$	SO	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

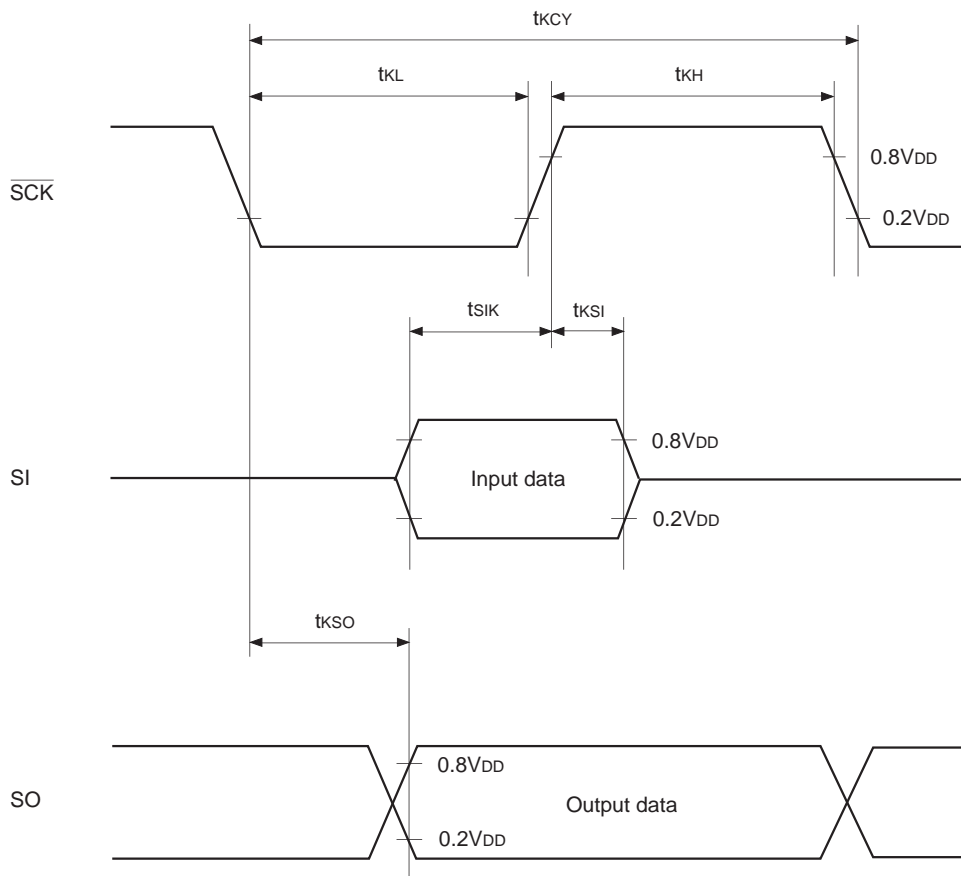**Note)** The load condition for the $\overline{SCK}$ output mode, SO output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing

(3) Interruption, reset input (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

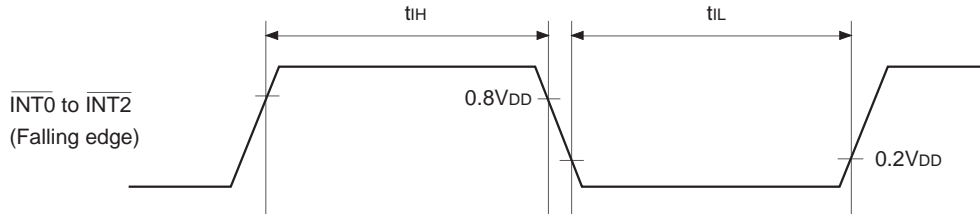| Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH} t_{IL}	$\overline{INT0}$ to $\overline{INT2}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		8/fc		µs

Fig. 5. Interruption input timing

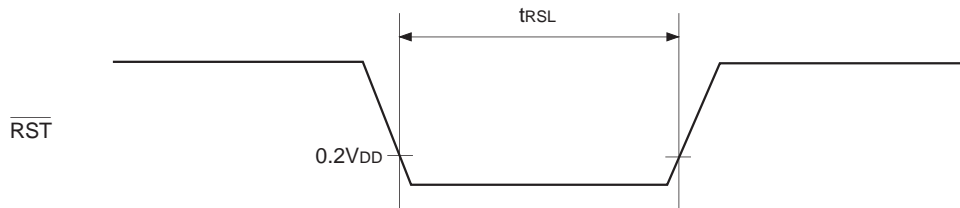**Fig. 6. $\overline{RST}$ input timing**

(4) Power on reset

Power on reset*   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on reset	1		ms

* Specifies only when the power-on reset function has been selected.
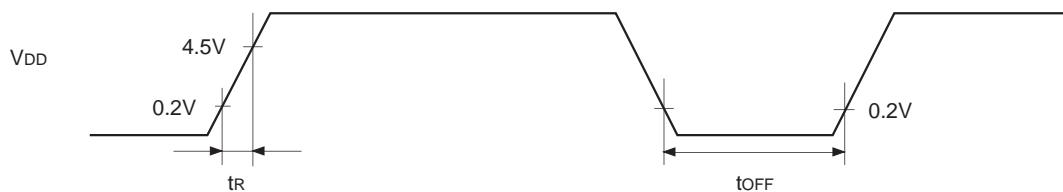
The power supply should be raised smoothly.

Fig. 7. Power-on reset

(5) A/D converter characteristics   (Ta = −20 to +75°C, V$_{DD}$ = 4.5 to 5.5V, V$_{ss}$ = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						4	Bits
Linearity error						±1	LSB
Zero transition voltage	V$_{ZT}$*1		Ta = 25°C V$_{DD}$ = 5.0V V$_{ss}$ = 0V	−10	160	320	mV
Full-scale transition voltage	V$_{FT}$*2			4370	4530	4690	mV
Conversion time	t$_{CONV}$			160/fc			µs
Sampling time	t$_{SAMP}$			12/fc			µs
Analog input voltage	V$_{IAN}$	AN0 to AN3		0		V$_{DD}$	V
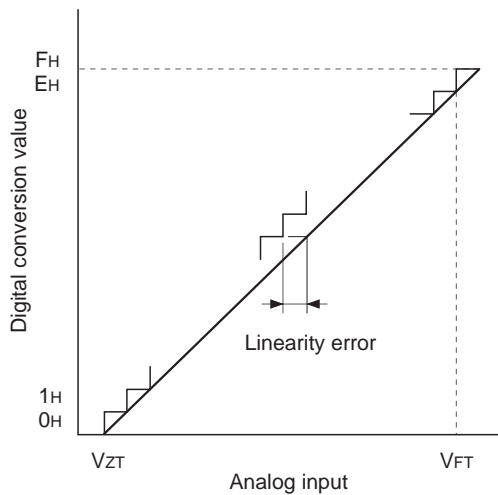
*1 V$_{ZT}$: Value at which the digital conversion value changes from 0$_H$ to 1$_H$ and vice versa.

*2 V$_{FT}$: Value at which the digital conversion value changes from E$_H$ to F$_H$ and vice versa.

Fig. 8. Definition of A/D converter terms

Note) The 4-bit conversion specifies values based on the upper 5 bits of the A/D data register (ADD: Address 00F5$_H$), compensated into 4-bit data. A program example is shown below:

(A/D converter program example)

```
          MOV      A, ADD       ; ACC ← conversion data
          LSR      A            ; Shift to the right (4 times)
          LSR      A            ;
          LSR      A            ;
          LSR      A            ;
          ADC      A, #00H      ; Addition with carry (data increment if AD3 = 1)
          CMP      A, #10H      ;
          BNE      ADC_SKIP     ;
          MOV      A, #0FH      ;
ADC_SKIP:
```

(6) I²C bus timing (Ta = –20 to +75°C, V$_{DD}$ = 4.5 to 5.5V, V$_{SS}$ = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f$_{SLC}$	SCL		0	100	kHz
Bus free time prior to transfer start	t$_{BUF}$	SDA, SCL		4.7		µs
Transfer start hold time	t$_{HD; STA}$	SDA, SCL		4.0		µs
Clock Low level width	t$_{LOW}$	SCL		4.7		µs
Clock High level width	t$_{HIGH}$	SCL		4.0		µs
Setup time during repetitive transfer	t$_{SU; STA}$	SDA, SCL		4.7		µs
Data hold time	t$_{HD; DAT}$	SDA, SCL		0[*1]		µs
Data setup time	t$_{SU; DAT}$	SDA, SCL		250		ns
SDA, SCL rise time	t$_R$	SDA, SCL			1	µs
SDA, SCL fall time	t$_F$	SDA, SCL			300	ns
Transfer end setup time	t$_{SU; STO}$	SDA, SCL		4.7		µs

[*1] The data hold time does not take into consideration SCL rise time (300ns max.). Ensure that the data hold time exceeds 300ns.
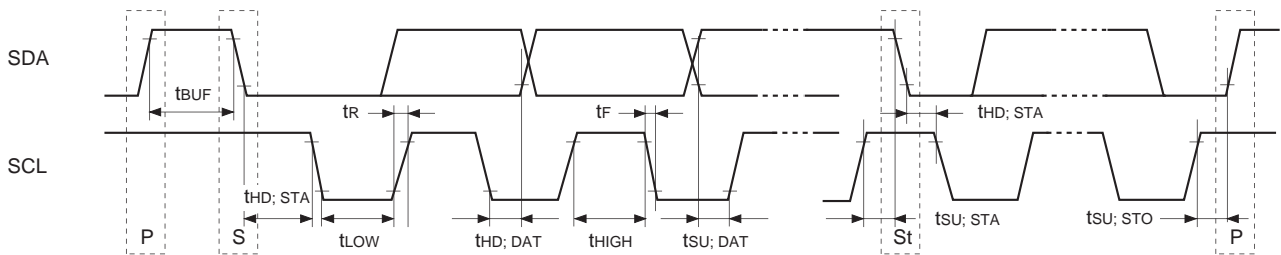

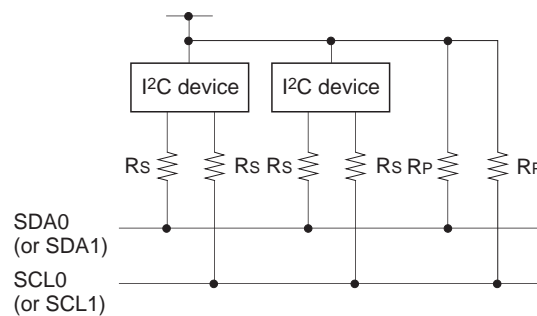**Fig. 9. I²C bus transfer timing**

Fig. 10. Recommended circuit example for I²C device

• Pull-up resistors (R$_P$) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).

• Serial resistance (R$_S$ = 300Ω and under) of SDA0 (or SDA1) and SCL0 (or SCL1) reduces spike noise caused by CRT flashover.

(7) OSD (On-Screen Display) timing (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Condition	Min.	Max.	Unit
OSD clock frequency	f_{OSC}	EXLC XLC	Fig. 12	4	13	MHz
HSYNC pulse width	t_{HWD}	HSYNC	Fig. 11	1.2		µs
VSYNC pulse width	t_{VWD}	VSYNC	Fig. 11	1.0		H*
HSYNC after-edge rise time/fall time	t_{HCG}	HSYNC	Fig. 11		200	ns
VSYNC after-edge rise time/fall time	t_{VCG}	VSYNC	Fig. 11		1.0	µs

* H indicates 1HSYNC period.

HSYNC
when Bit 5 of OPOL register
(01FBH) is set to "0"

t_{HWD} t_{HCG} 0.8V_{DD} 0.2V_{DD}

VSYNC
when Bit 4 of OPOL register
(01FBH) is set to "0"

t_{VWD} t_{VCG} 0.8V_{DD} 0.2V_{DD}

Fig. 11. OSC timing

EXLC   XLC

L

C_1 C_2
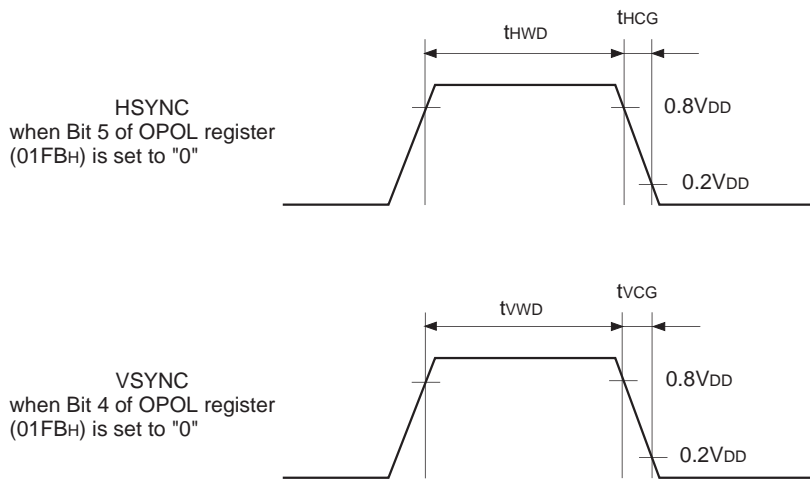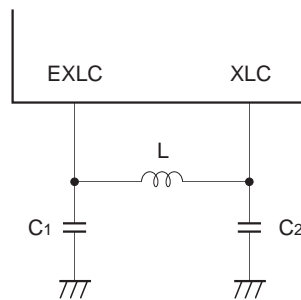
Fig. 12. LC oscillation circuit example

Supplement

(i)

(ii)

Fig. 13. Recommended Oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0	(i)
	CSA4.19MG	4.19				
	CST4.00MGW*	4.00				(ii)
	CST4.19MGW*	4.19				
RIVER ELETEC CORPORATION	HC-49/U03	4.00	10	10	0	(i)
		4.19				
KINSEKI LTD.	HC-49/U (-S)	4.00	18	18	0	
		4.19				

* Indicates types with on-chip grounding capacitance (C_1 and C_2).

Mask option table

Item	Content	
Reset pin pull-up resistance	Non-existent	Existent
Power-on reset circuit	Non-existent	Existent

I$_{DD}$ vs. V$_{DD}$
(fc = 4MHz, Ta = 25°C typical)

- 1/2 frequency demultiplication mode
- 1/4 frequency demultiplication mode
- 1/16 frequency demultiplication mode
- Sleep mode

I$_{DD}$ – Power supply current [mA]

V$_{DD}$ – Supply voltage [V]

I$_{DD}$ vs. fc
(V$_{DD}$ = 5V, Ta = 25°C typical)

- 1/2 frequency demultiplication mode
- 1/4 frequency demultiplication mode
- 1/16 frequency demultiplication mode
- Sleep mode

I$_{DD}$ – Power supply current [mA]

fc – System clock [MHz]

OSD oscillation vs. C
Calculated curves
(reference value by theoretical calculation)

- 5.0MHz
- 6.5MHz
- 13.0MHz

L – Inductasce [µH]

$$fosc = \frac{1}{2\pi\sqrt{LC}} \quad C = C_1 // C_2$$

C$_1$, C$_2$ – Capacitance [pF]

Fig. 14. Characteristics curves

Package Outline   Unit: mm

64PIN SDIP (PLASTIC)
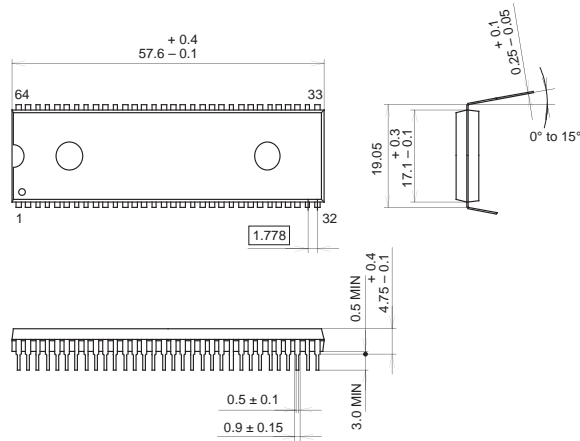
PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	8.6g

64PIN QFP(PLASTIC)
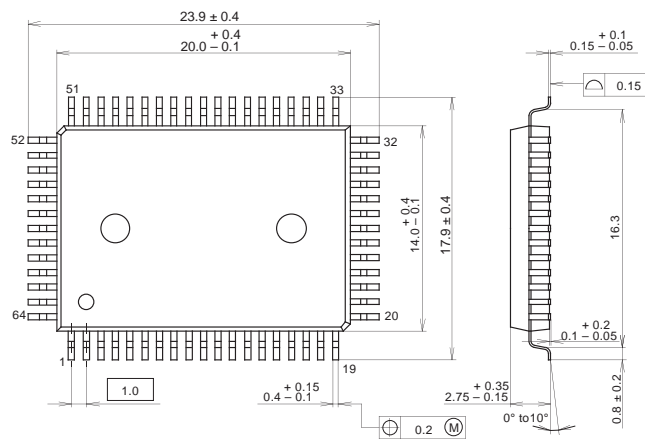
PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g