AN610

Using the 24LC21 Dual Mode Serial EEPROM

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INTRODUCTION

The Microchip Technology Inc. 24LC21 is a 1K-bit (128 x 8) dual mode serial EEPROM that was developed primarily for use in computer monitors. This part was developed with inputs from several computer monitor manufacturers, in accordance with the VESA® (Video Electronics Standards Association) monitor committee. This committee has developed a serial communication protocol called Data Display Channel (DDC™) which was created to eliminate the need to change dip switches when configuring a new system or adding a new monitor or video card. The 24LC21 device is used in the monitor to store and transmit the EDID (extended display ID) table which contains all set-up parameters needed by the video card to operate with a particular monitor. With this system, the user can now plug any compatible monitor into any compatible graphics board and the graphics board will automatically know what type of monitor is being used and configure itself accordingly. This automatic configuration is the cornerstone for Microsoft®'s 'Plug and Play' capability being built into the new 'Windows 95™' release.

DEVICE OPERATION

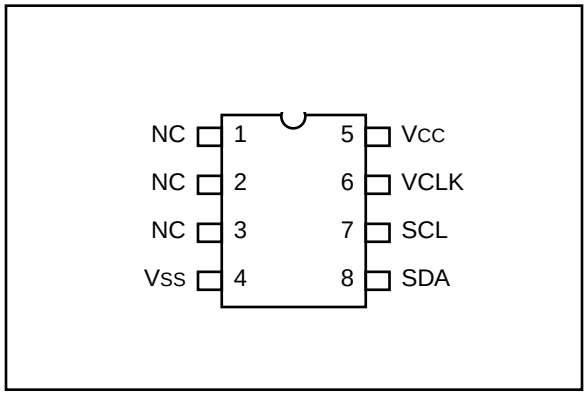
The 24LC21 can operate in two modes of operation. These two modes of operation are the transmit only mode and bi-directional mode. Upon power-up, the device will always be in the transmit-only mode. Transmit only mode is also referred to as DDC1 mode. The transmit only mode only allows the video card to read the contents of the 24LC21 in a sequential manner, one bit at a time. Writing to the device is not possible in transmit only mode.

The device will automatically transition to the bi-directional mode whenever a falling edge is seen on the SCL pin. Bi-directional mode is also referred to as DDC2 mode, and is implemented as the standard I^2C™ protocol. This allows a controller to read and write specific addresses in the device like a standard I^2C Serial EEPROM device. Once the device has transitioned to the bi-directional mode, there is no way to return to transmit only mode other than to reset (power-down) the device.

TRANSMIT ONLY MODE (DDC1)

The 24LC21 will always power-up in the transmit only mode. In this mode, the 24LC21 will output one bit of data at the SDA pin for every rising edge on the VCLK pin. The data will be transmitted in 8-bit words, with each word followed by a 9th null bit. This null bit will always be high. A timing diagram for transmit only mode is shown in Figure 1. As long as VCLK is present and no falling edges on SCL are received, the 24LC21 will repeatedly cycle through the entire memory array.

PACKAGE TYPE



Upon power-up, the device will not output valid data until it has been initialized. This initialization procedure (Figure 1) data will not be available until after the first 9 clocks are sent to the device. The exact memory location that the 24LC21 begins to transmit data is unknown at power-up, and the initialization procedure only initializes the device, not the starting address or bit location. In order to for a controller to determine what address is being read, a 'framing' or 'syncing' procedure must be executed by the video card.

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A framing procedure involves looking for the header portion of the EDID table which is a byte of 00H followed by 6 bytes of FFH and another byte of 00H. A framing routine would continue to clock data from the 24LC21 until this unique header has been found. At this point, the current location in the EDID table has been determined and the controller has now synchronized itself with the device. Care must be taken while using the device in the transmit only mode to prevent noise on the SCL pin, as a falling edge seen on this pin will immediately send the part into the bi-directional mode. In a DDC1-only monitor, SCL is not connected to the VGA connector, but must still be terminated to VCC through a pullup resistor.

FIGURE 1: TRANSMIT ONLY MODE

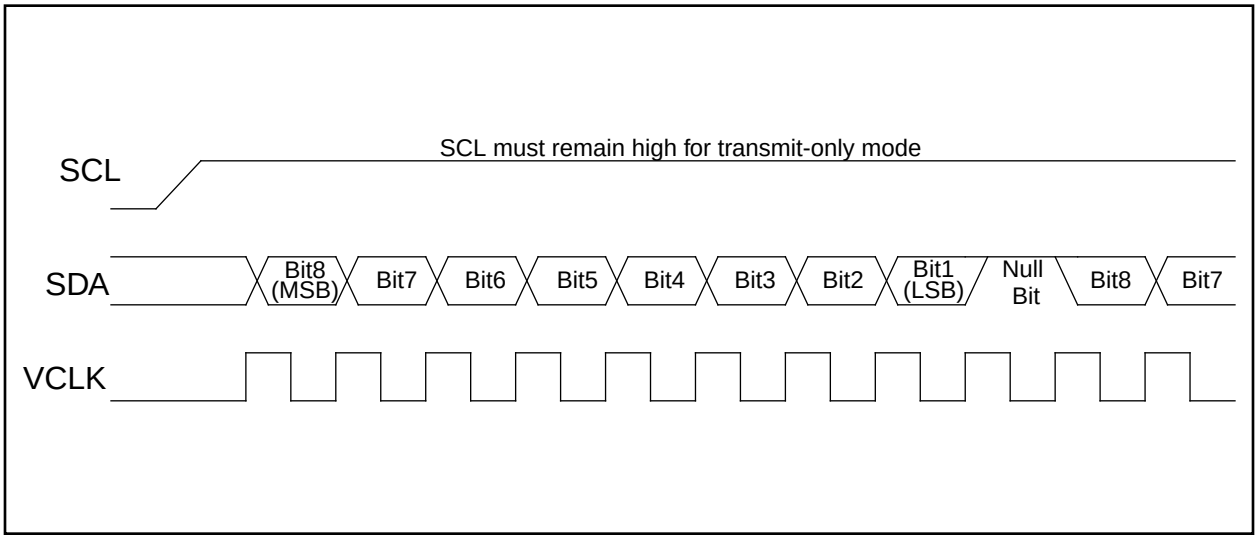
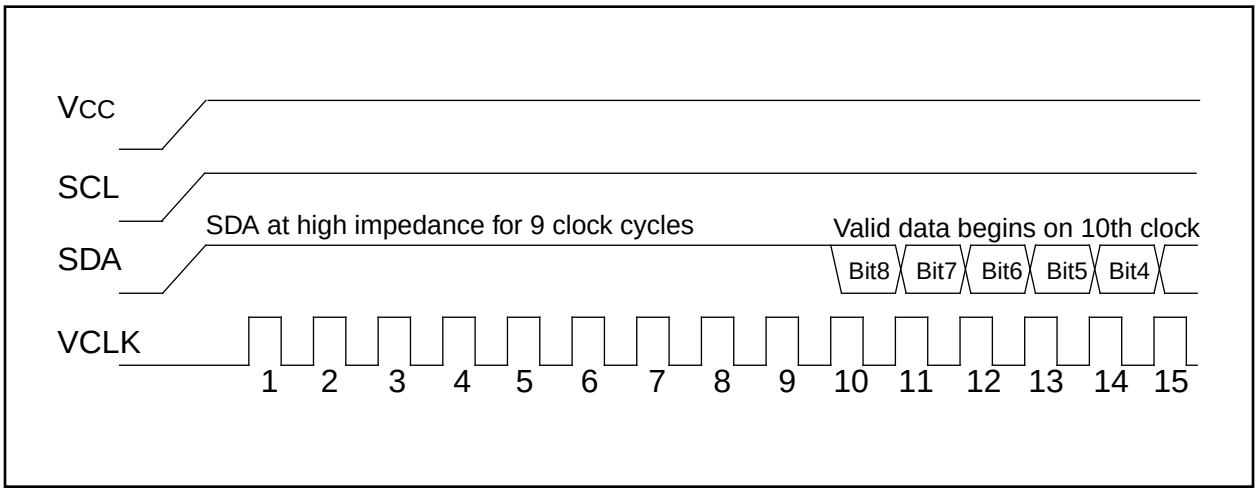


FIGURE 2: DEVICE INITIALIZATION FOR TRANSMIT-ONLY MODE



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BI-DIRECTIONAL MODE (DDC2)

Bi-directional mode is essentially the standard I^2C protocol and allows the controller to read and write to the device. The 24LC21 supports byte and page writes and byte and sequential reads in the bi-directional mode. This mode will be used primarily before the monitor leaves the factory to load the EDID table into the device, but it also provides a means of updating the table if necessary. It is also used for faster (up to 100 kHz) data transmission, or transmission of only specific requested data in a DDC2 system. (The I^2C protocol allows the host to request data from a specific portion of the EDID table rather than waiting for the entire table.) When writing to the device, the VCLK pin must be held high while the write command is being loaded or the write will be aborted and no data will be written. Note that this is the opposite of the 24LC01B, where the WP pin must be held low for the device to be written.

EDID TABLE

The EDID table is the Extended Display ID table, specified by VESA, that will be stored in the 24LC21 and contains information about what type of display it is and the capabilities of the display. The basic EDID table consists of 128 bytes of data. A breakdown of the table is shown below in Table 1. A complete description of the table can be found in the VESA DDC Specification.

TABLE 1: EDID TABLE DESCRIPTION

Bytes	Description
8	Header
10	Vendor/Product Description
2	EDID Version/Revision
15	Basic Display Parameters/Features
19	Established/Standard Timings
72	Detailed Timing Descriptions (18 bytes each)
1	Extension Flag
1	Checksum

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USING THE 24LC21 IN A SYSTEM

In order to use the 24LC21 in a monitor system, it must be programmed with a proper EDID table and then properly connected to the signals coming from the video controller card. The VESA committee has specified that the connections for DDC transmission can be part of the standard 15-pin VGA connector. A table of pinouts for this connector are shown in Table 2. Signals that pertain to the use of the 24LC21 are highlighted.

Programming of the 24LC21 can be accomplished via Microchip Technology's SEEVAL programming and evaluation system or by any final test system at the customer site which can communicate over the I^2C bus.

TABLE 2: VGA CONNECTOR DESCRIPTION

Pin	Standard VGA	DDC1 Host	DDC2 Host	DDC1.2 Display
1	Red Video	Red Video	Red Video	Red Video
2	Green Video	Green Video	Green Video	Green Video
3	Blue Video	Blue Video	Blue Video	Blue Video
4	Monitor ID Bit2	Monitor ID Bit2	Monitor ID Bit2	Return
5	Test (Ground)	Return	Return	Return
6	Red Video Return	Red Video Return	Red Video Return	Red Video Return
7	Green Video Return	Green Video Return	Green Video Return	Green Video Return
8	Blue Video Return	Blue Video Return	Blue Video Return	Blue Video Return
9	No Connection	+5V Supply (optional)	+5V Supply (optional)	+5V Supply (optional)
10	Sync Return	Sync Return	Sync Return	Sync Return
11	Monitor ID Bit0	Monitor ID Bit0	Monitor ID Bit0	Optional
12	Monitor ID Bit1	**Data from Display (SDA)**	**Bi-directional Data (SDA)**	**Bi-directional Data (SDA)**
13	Horizontal Sync	Horizontal Sync	Horizontal Sync	Horizontal Sync
14	Vertical Sync	**Vertical Sync (VCLK)**	Vertical Sync	**Vertical Sync (VCLK)**
15	Monitor ID Bit3	Monitor ID Bit3	**Data Clock (SCL)**	**Data Clock (SCL)**

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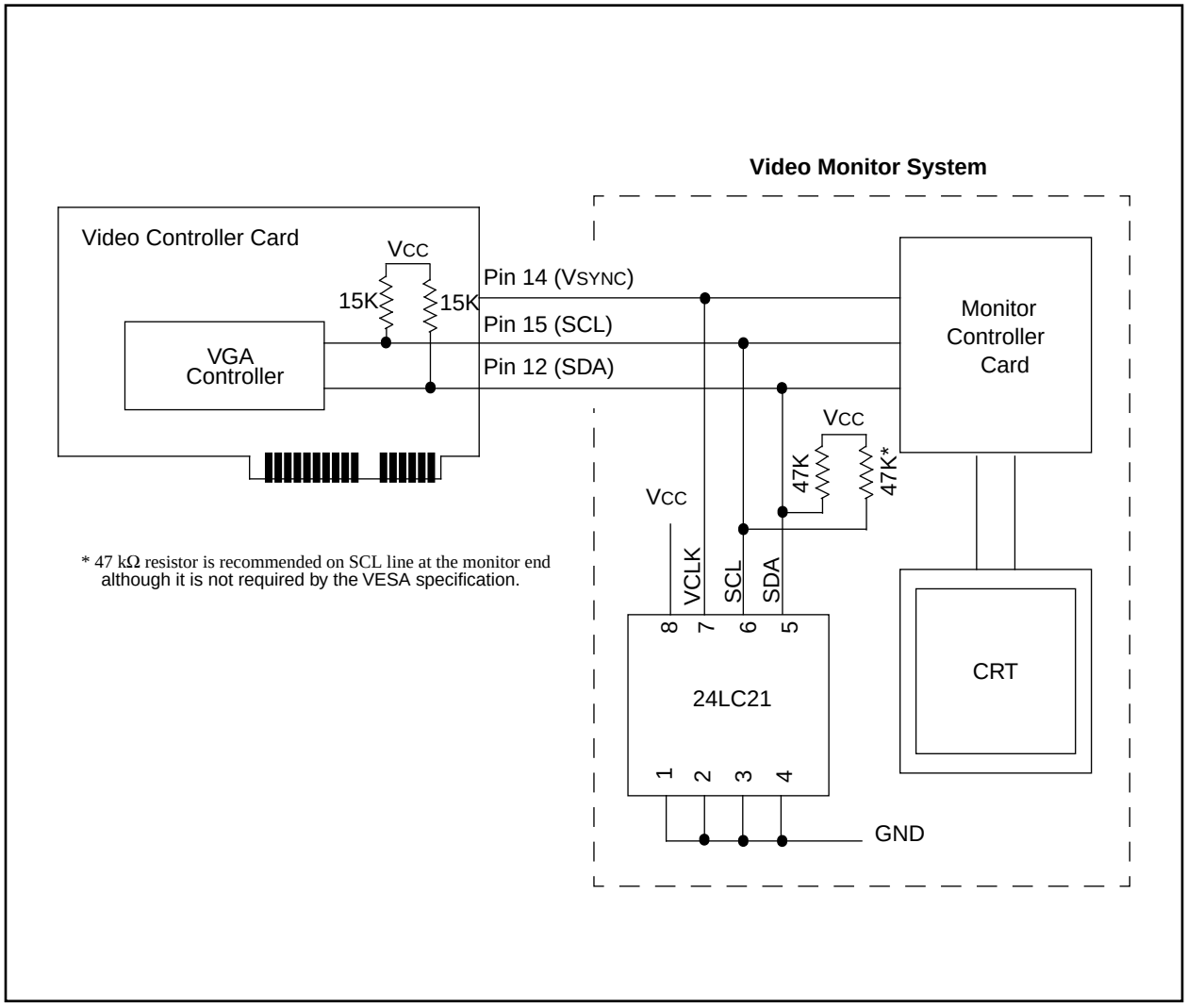
SYSTEM CONFIGURATION

A typical system configuration is shown below. The DDC specification states that a 47 kΩ pull-up resistor is required on the SDA line at the monitor end. It also states that a 15K pullup resistor is needed on both the SCL and SDA lines at the video controller end.

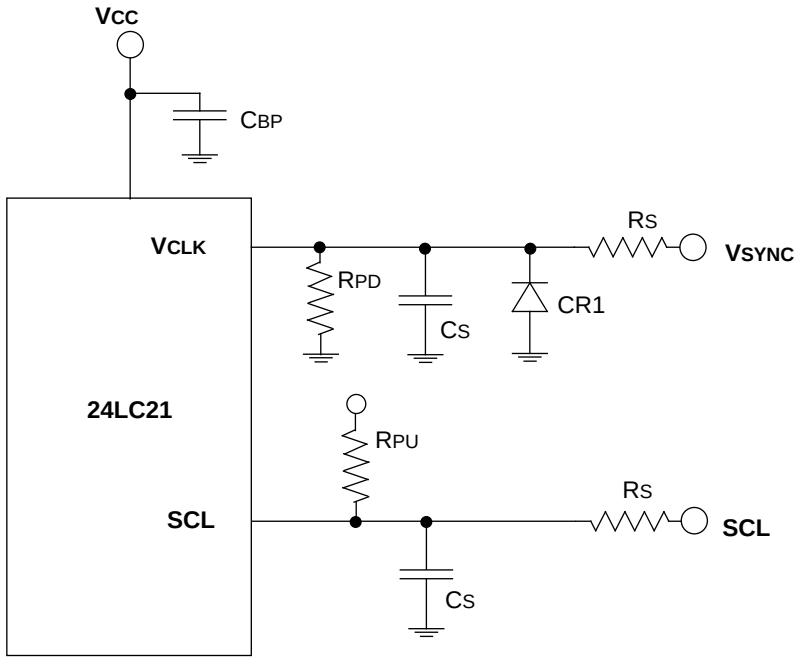
FIGURE 3: USE OF 24LC21 IN VIDEO SYSTEM



POTENTIAL PROBLEMS CAUSED BY NOISE IN A VIDEO SYSTEM

Because the typical application for the 24LC21 is in a computer monitor where electronic noise is prevalent, some precautions may need to be made in order for this device (or any other CMOS device) to work properly. The diagram below (Figure 4) shows a filter circuit that can be used to reduce the amount of noise seen by the device on the SCL and VCLK pins.

FIGURE 4: RECOMMENDED FILTER CIRCUIT FOR MONITOR APPLICATIONS



C_{BP} = 1 µF
R_S = 100 - 300 Ω
R_{PD} = 4.7 kΩ
C_S = 100 - 1000 pF
R_{PU} = 47 kΩ

C_{BP}	Bypass capacitor
R_{PD}	Can be as a termination resistor on VGA cable. Also will discharge the series capacitor going to the MCU and horizontal/Vertical processor.
C_S and R_S on V_{CLK}	Acts as low pass filter to clean-up noise on V_{SYNC} line
C_S and R_S on SCL	Acts as low pass filter to clean-up noise and dampen power transient spikes that may cause accidental mode switching from DDC1 to DDC2
R_{PU} on SCL	Keeps SCL pulled high, although a high enough value is used that the host will not power the 24LC21. Lets the 24LC21 reset when the monitor power is turned off
CR1	Eliminates undershoot on V_{SYNC}

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NOTES:

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