

AD7528 Dual 8-Bit CMOS DAC Application Note

by Paul Toomey and Bill Hunt

INTRODUCTION

The AD7528 is a monolithic dual 8-bit CMOS DAC packaged in a 20-pin DIP. Each DAC has its own 8-bit data latch which loads data from a common 8-bit data bus (see Figure 1). Since both DACs are fabricated on the same chip, precise matching and tracking between DACs is inherent. This property of the AD7528 dual DAC, along with the P.C. board space saving it allows, makes the AD7528 a unique and extremely useful device.

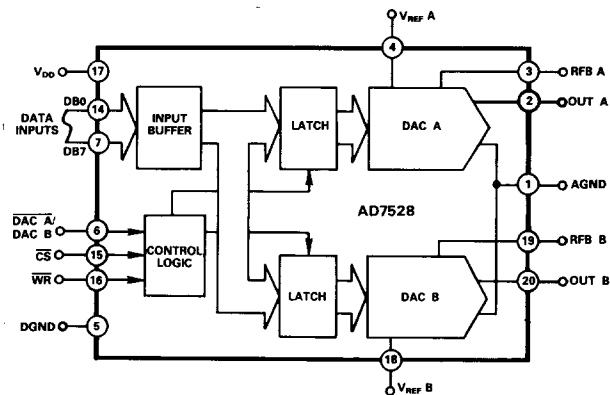


Figure 1. AD7528 Functional Diagram

This note discusses the AD7528 applications circuits listed below. Several of these circuits rely on the DAC to DAC matching provided by the AD7528. All of the circuits benefit from the high packing density the AD7528 allows, especially when used with dual and quad op-amps such as the AD644 or TL074. Not discussed in this note are basic details of AD7528 operation, consult the data sheet for this information.

AD7528 APPLICATIONS DISCUSSED IN THIS NOTE

1. State-variable filter (S.V.F.) with programmable center frequency, selectivity and gain.
2. Programmable sine wave oscillator with linear control.
3. Function fitting sine wave synthesizer with amplitude control facility and programmable phase shift.
4. Programmable voltage/current source, unipolar and bipolar circuits.

5. Programmable gain amplifier with no trim pots.
6. Programmable waveform generator for vector scan CRT displays.
7. AD7528 single-supply operation circuits for low budget applications requiring multiple analog outputs

STATE VARIABLE FILTER WITH PROGRAMMABLE CENTER FREQUENCY, SELECTIVITY (Q) AND GAIN

The state variable filter (or universal filter as it is often called) is a convenient 2nd order filter block. It provides simultaneous low-pass, high-pass and bandpass outputs. All filter parameters can be readily adjusted. Figure 2 shows a typical filter circuit with expressions for center frequency, Q and gain for the bandpass output.

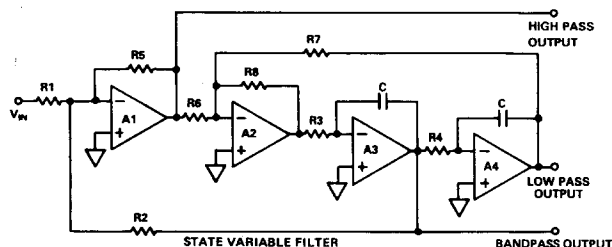


Figure 2. State Variable Filter

BANDPASS TRANSFER FUNCTION

$$\frac{V_{OUT}}{V_{IN}}(f) = \frac{A_0}{1 + jQ \left[\frac{f}{f_0} - \frac{f_0}{f} \right]}$$

$$f_0 = \frac{1}{2\pi R_3 C} \cdot \sqrt{\frac{R_8}{R_7}} \quad (\text{For } R_3 = R_4)$$

$$Q = \frac{R_6 \cdot R_2}{R_8 \cdot R_5} \cdot \sqrt{\frac{R_8}{R_7}}$$

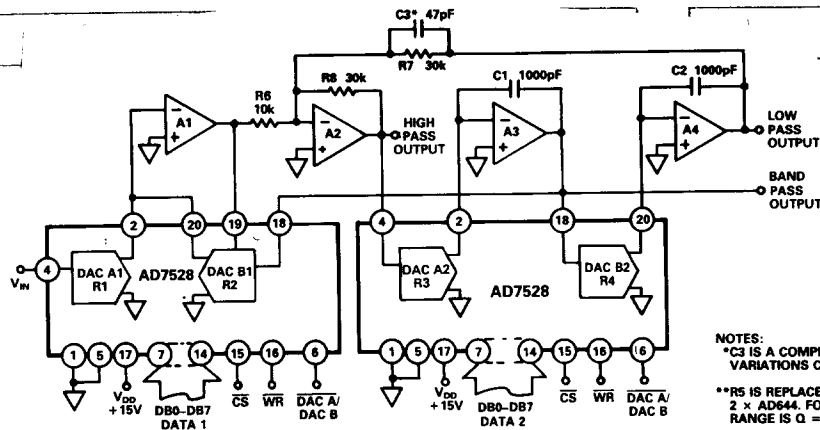
$$A_0 = -\frac{R_2}{R_1}$$

Where f = frequency of V_{IN}

A_0 = gain at $f = f_0$

Q = circuit Q factor, i.e., $\frac{f_0}{3\text{dB Bandwidth}}$

f_0 = resonant frequency.



CIRCUIT EQUATIONS:
 $C1 = C2, R3 = R4, R7 = R8$

$$f_o = \frac{1}{2\pi R3 C1}$$

$$Q = \frac{R6 \cdot R2}{R8 \cdot R5^{**}}$$

$$A_o = -\frac{R2}{R1} \text{ For Bandpass Output}$$

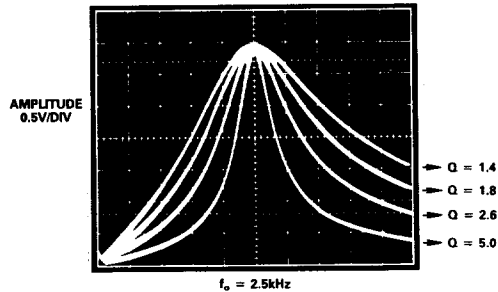
DAC EQUIVALENT RESISTANCE EQUALS
 $256 \times (\text{DAC LADDER RESISTANCE})$
DAC DIGITAL CODE (DECIMAL)

NOTES:
 *C3 IS A COMPENSATION CAPACITOR TO ELIMINATE Q AND GAIN VARIATIONS CAUSED BY AMPLIFIER GAIN BANDWIDTH LIMITATIONS
 **R5 IS REPLACED BY DAC B1 INTERNAL RFB = 11kΩ, OP-AMPS ARE 2 × AD644. FOR COMPONENT VALUES SHOWN PROGRAMMABLE RANGE IS Q = 0.3 TO 4.5, $f_o = 0$ TO 15kHz.

Figure 3. Digitally Controlled State Variable Filter

Introducing the DACs as Control Elements:

By replacing R1, R2 and R3, R4 with matched DAC pairs the filter parameters can be made programmable as shown in Figure 3. DAC A1 and DAC B1 control filter gain and Q, while DAC A2 and DAC B2 control center frequency (f_o). For the component values shown the programmable Q range is from 0.3 to 4.5 and is independent of f_o (see Figure 4). Center frequency (f_o) is programmable from 0 to 15kHz (see Figure 5) and is independent of Q.



Filter 4. Filter Q Variation

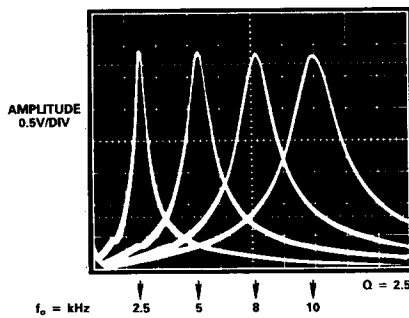


Figure 5. Filter f_o Variation

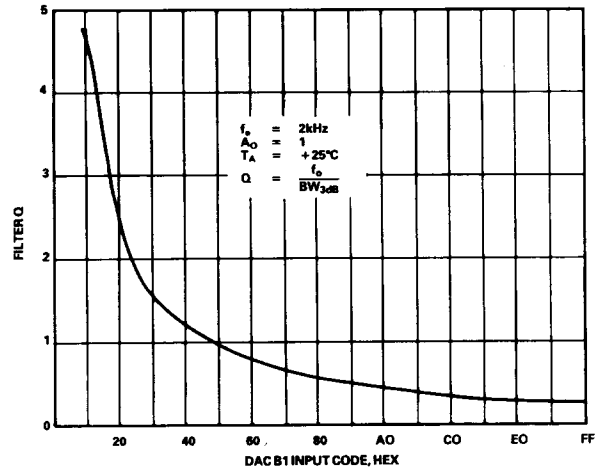


Figure 6. Filter Q Variation with Code

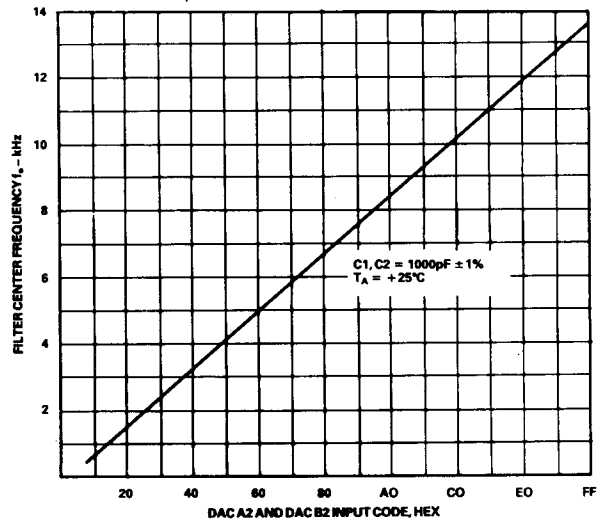


Figure 7. Filter f_o Variation with Code

Programming

The graph in Figure 6 shows how the circuit Q varies with DAC B1 code and Figure 7 shows how the center frequency varies with DAC 2 (A and B) code for the component values given in Figure 3. Gain variation alone is accomplished by changing DAC A1 code. Unity gain occurs when the data in DAC A1 and DAC B1 latches is identical. Since the AD7528's logic inputs are TTL or CMOS compatible, the DACs are readily interfaced to most microprocessors, (see data sheet for hookups) thus providing an ideal microprocessor-to-filter interface.

PROGRAMMABLE SINE WAVE OSCILLATOR WITH LINEAR CONTROL

Frequency control of many oscillator circuits can be accomplished using two ganged potentiometers. However, the two potentiometers must track precisely over their full temperature range if a linear response is required. Figure 8 shows a high performance sine-wave oscillator realized using a state-variable filter. The frequency of oscillation is set by ganged potentiometers P1 and P2.

Figure 9 shows the same circuit with P1 and P2 replaced by the AD7528 matched pairs.

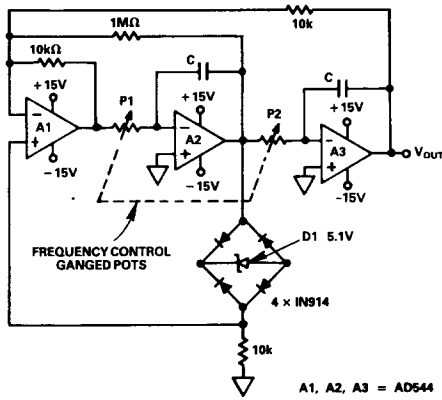


Figure 8. Sine Wave Oscillator Using a State Variable Filter

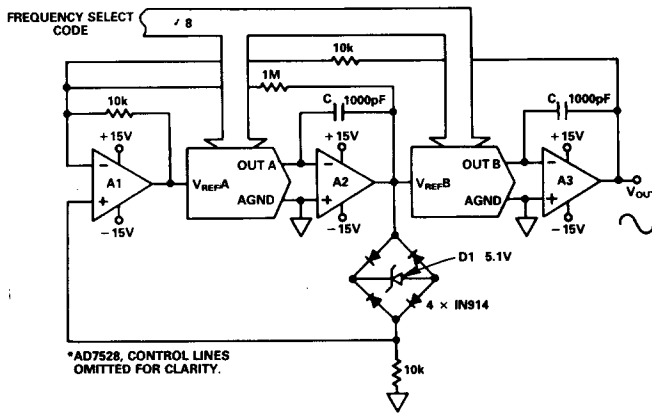


Figure 9. Programmable Sine Wave Oscillator Using a State Variable Filter and a Dual DAC

The equivalent resistance of each DAC, as seen by op-amps A2 and A3 varies with input code from infinity at code 00 Hex (0000 0000) to a minimum of $\approx 11k\Omega$ (DAC ladder resistance) at code FF HEX (1111 1111).

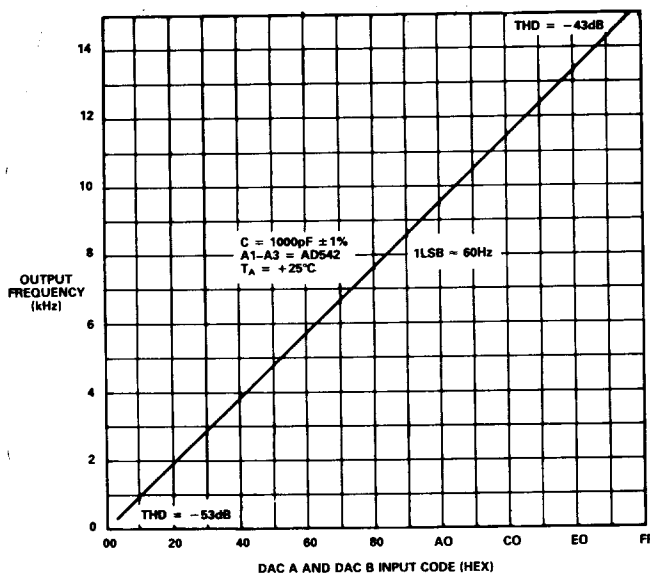


Figure 10. Frequency vs. DAC Code for Programmable Sine Wave Oscillator (Figure 9)

Loading each DAC latch with the same code provides a linear code versus frequency relationship as shown in Figure 10. The frequency of oscillation can be expressed as:

$$\text{Output Frequency} = \frac{N}{256(2\pi RC)} \text{ Hz}$$

Where R = DAC ladder resistance i.e. V_{REF} input resistance.

C = is as shown in Figure 9.

N = decimal representation of digital input code. For example, N = 128 for input code 10000000.

For the component values given in Figure 9, output frequency is variable from 0 to 15kHz. Output amplitude is controlled by the zener diode D1. Total harmonic distortion for the circuit shown is -53dB at low frequencies (1kHz) and -43dB at higher frequencies (14kHz). Note that a cosine output is also available at the output of op-amp A2.

FUNCTION FITTING SINE WAVE SYNTHESIZER

In this application the multiplying capabilities of the two CMOS DACs are used to synthesize a sine wave based on a function fitting technique. This allows very low frequency, highly stable sine waves to be generated.

Function Fitting:

Function fitting is a technique for translating a mathematical or empirical relationship from one medium (such as a mathematical formula) to another medium (usually a physically realizable device or system). This application uses the dual DAC to implement a one quadrant sin X approximation in the form of the quadratic polynomial.

$$Y = 1.828N - 0.828N^2 \text{ where } 0 \leq N \leq 1 \text{ and } N = \frac{2}{\pi} X$$

The graph of Figure 11 shows the relationship between sin X and its quadratic approximation given above. The

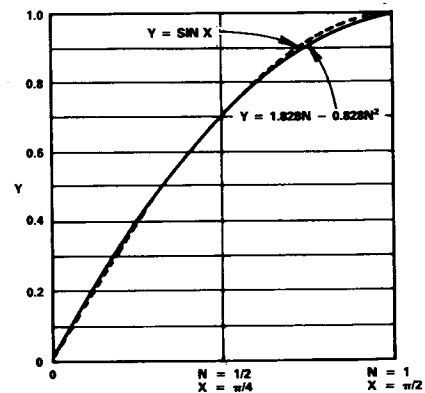


Figure 11. Relationship Between Sin X and its Quadratic Approximation

circuit of Figure 12 implements the function by ramping N up and down using an up/down counter, and switching the circuit output polarity. This generates sin X in four stages (see Figure 13).

Circuit Operation: (Figure 12)

An input clock drives the up/down counter in real time. The counter is connected so that it counts up and down continuously, providing an output pulse at "borrow" every time it reaches the all zeros count.

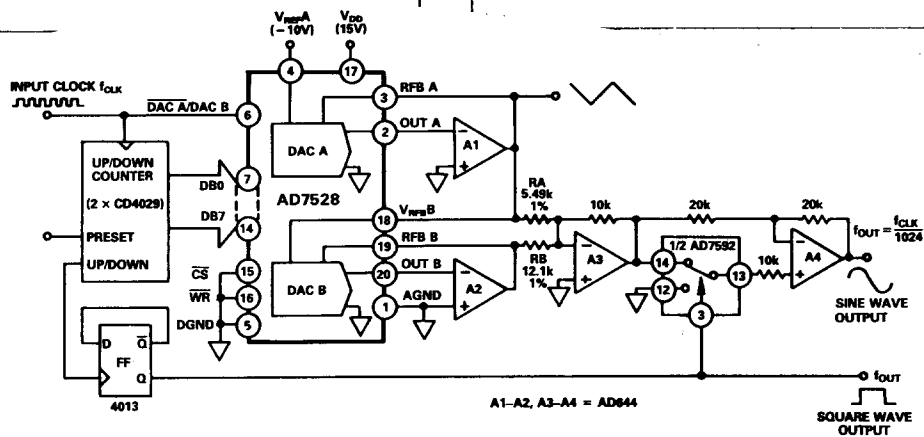


Figure 12. Function Fitting Sine Wave Generator

DAC A produces a triangle waveform consisting of two ramps of opposite slope, each generated in 256 steps at op-amp A1 output. This is the N variable.

DAC B is driven with the same digital word as DAC A. Its reference input is driven by op-amp A1, thus DAC B multiplies the digital version of N by the analog version of N to produce an output from op-amp A2 of $-N^2$ (negative sign is due to inversion through A2).

Since the N and $-N^2$ signals are of opposite polarity, the $Y = 1.828N - 0.828N^2$ expression is implemented by summing N and $-N^2$ signals in the correct ratios determined by R_A and R_B .

The analog switch, in conjunction with op-amp A4, changes the circuit's output polarity at one-half the triangle wave frequency, thus producing both positive and negative halves of the sine wave.

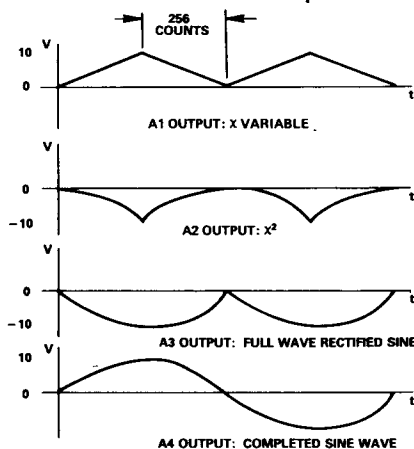


Figure 13. Sine Wave Synthesis Using Function Fitting

Distortion:

Distortion in the output sine wave is a function of the quadratic approximation fit to the sine curve. Errors in the values of R_A and R_B will, therefore, contribute directly to distortion. If R_A is made adjustable over a small range, it can be trimmed to minimize distortion. Distortion was measured for the circuit of Figure 12 at -33 dB and was constant over sine-wave frequency 0 – 2.5 kHz.

The circuit of Figure 12 generates constant amplitude sine waves in the 0 – 2.5 kHz frequency range. Output frequency is given by

$$f_{\text{OUT}} = \frac{f_{\text{CLK}}}{1024}$$

It is possible to obtain rapid frequency sweeping by varying the input clock rate. The counter up/down output provides a useful zero crossing pulse. By applying an ac signal to the DAC A reference input, the output sine wave can be amplitude-modulated as shown in Figure 14.

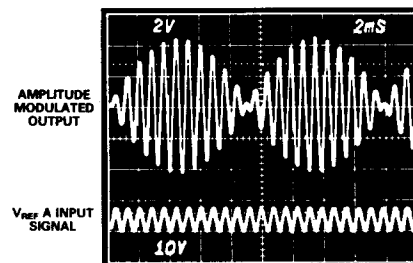


Figure 14. Amplitude Control Using DAC A Reference Input

Output amplitude is directly controlled by the voltage level on DAC A reference input. Ac or dc signals may be used within the range ± 10 volts, 0 to 10 kHz. Figure 14 shows the amplitude of a 1 kHz sine wave being controlled by a 55 Hz sine wave.

Programmable Phase

Two sine waves with 0 to 360° programmable phase relationship can be generated by running two of the circuits, shown in Figure 12, from the same input clock source. By allowing one circuit to start running from zero count a preset number of clock cycles before the other, a phase difference between their output sine waves is introduced (see Figure 15).

Since each complete cycle is generated by 1024 clock cycles, phase steps of $360/1024$ degrees are programmable. Note also that the phase difference is independent of output frequency.

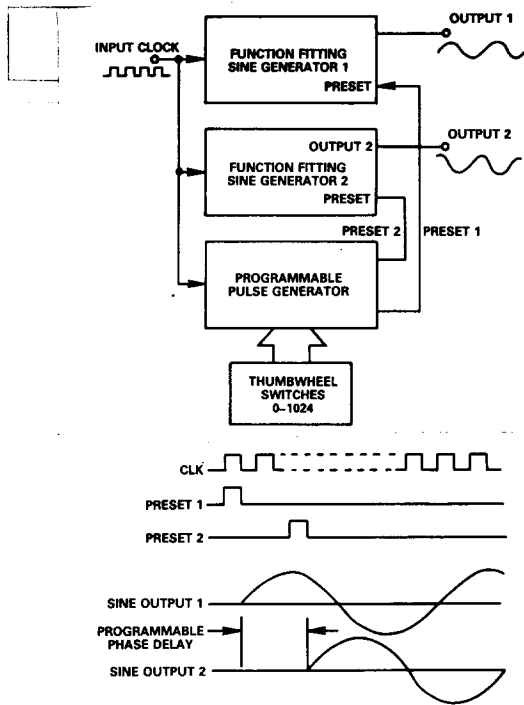


Figure 15. Programmable Phase Relationship

PROGRAMMABLE VOLTAGE/CURRENT SOURCE USING DUAL DAC AD7528

The circuit in Figure 16 is that of a unipolar V/I source. A negative reference is required for a positive output voltage.

The circuit provides;

- (a) A programmable output voltage

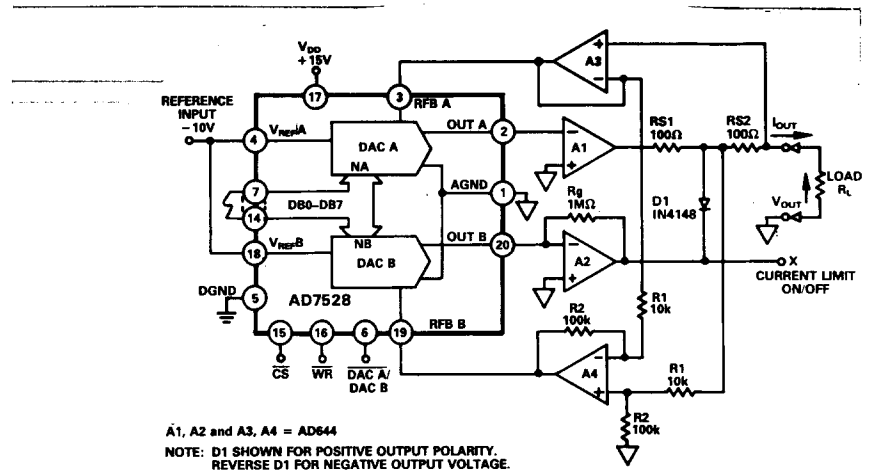
$$V_{OUT} = +V_{REFA} \frac{N_A}{256}, \text{ for } N_A = 0 \text{ to } 255.$$

provided the current limit is not exceeded.

- (b) In the voltage mode, a programmable load current limit given by:

$$I_{OUT(max)} = V_{REFB} \cdot \frac{R_1}{R_2} \cdot \frac{1}{R_{S2}} \cdot \frac{N_B}{256}$$

for $N_B = 0$ to 255.



A1, A2 and A3, A4 = AD644
NOTE: D1 SHOWN FOR POSITIVE OUTPUT POLARITY. REVERSE D1 FOR NEGATIVE OUTPUT VOLTAGE.

Figure 16. Programmable Voltage/Current Source $V_{OUT} = 0$ to $+10V$, $I_{OUT} = 0$ to $+10mA$

- (c) A constant current feature by setting $N_A = 255$ i.e., maximum output voltage capability, and limiting the load resistance value R_L such that

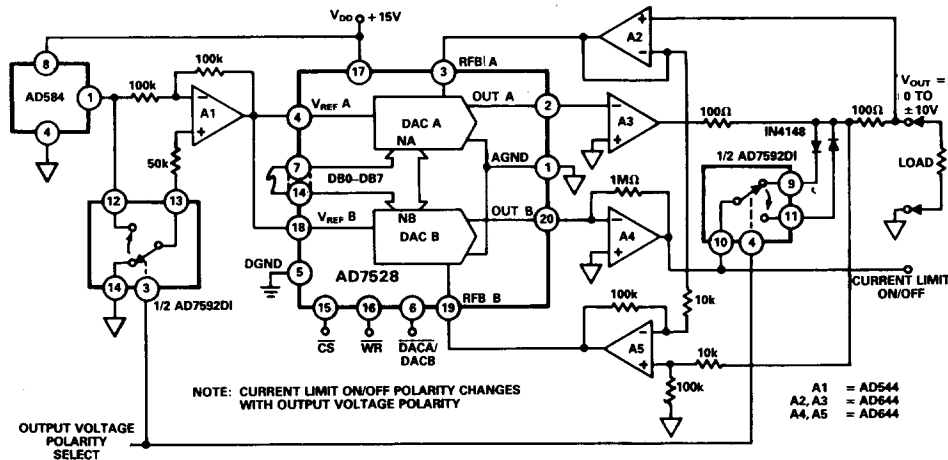
$$I_{OUT(max)} \cdot R_L < \frac{255}{256} V_{REFA}$$

$$\text{with } I_{OUT(max)} = V_{REFB} \cdot \frac{R_1}{R_2} \cdot \frac{1}{R_{S2}} \cdot \frac{N_B}{256}$$

as in (b).

A useful feature of the circuit is the possibility of load current "readback" in the voltage mode (or load voltage readback in the current mode). By monitoring point X in Figure 16, as the current limit value is reduced, a state change will take place when current limit is attained. The set current limit value will correspond to the load current.

In the circuit DAC A with amplifier A1 and buffer A3 acts as a standard programmable voltage source when V_{REFA} is held constant. The voltage drop across resistor R_{S2} provides a voltage proportional to load current with R_{S1} acting as a current limit on amplifier A2. Amplifier A4 with resistors R_1 and R_2 references the voltage across R_{S2} to ground and also provides gain $\left(\frac{R_2}{R_1}\right)$. The output of A4



NOTE: CURRENT LIMIT ON/OFF POLARITY CHANGES WITH OUTPUT VOLTAGE POLARITY

A1 = AD584
A2, A3 = AD644
A4, A5 = AD644

Figure 17. Programmable Voltage/Current Source with Bipolar Output

is compared with a proportion $\frac{N_B}{256}$ of V_{REFB} (usually $V_{REFA} = V_{REFB}$) by amplifier A2. If $V_{OUT4} > V_{REFB} \frac{N_B}{256}$

then current limit is required and the output of A2 via diode D1 draws load current to maintain a constant load current.

If $V_{OUT4} < V_{REFB} \frac{N_B}{256}$ then the current limit is not required and amplifier A2 output is disconnected as diode D1 is reversed biased.

Figure 17 shows a similar circuit for bipolar operation, i.e., 0 to $\pm 10V$ at 0 to $\pm 10mA$.

DUAL DAC PROGRAMMABLE GAIN AMPLIFIER WITH NO TRIMPOTS

A unique advantage of the matched DACs available in the AD7528 is utilized in the programmable gain/attenuation circuit shown in Figure 18. The equivalent resistance of each DAC from its reference input to its output is used to replace the input and feedback resistors in the standard inverting amplifier circuit. By loading DAC's A and B with suitable codes, programmable gain/attenuation over the range $-48dB$ to $+48dB$ can be achieved.

In the circuit of Figure 18, the DAC equivalent resistances are given by:

$$R_{DAC A} = \frac{256 R_{LDA}}{N_A} \text{ and } R_{DAC B} = \frac{256 R_{LDB}}{N_B}$$

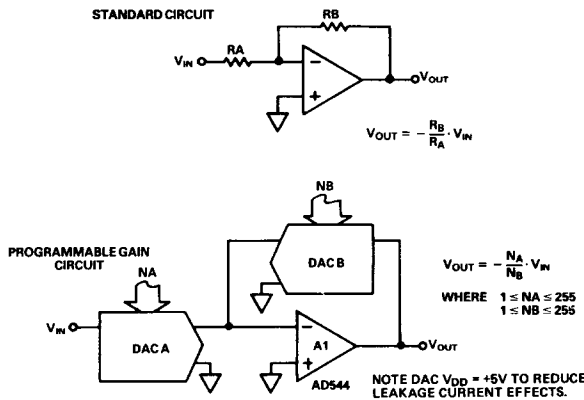


Figure 18. Dual DAC Programmable Gain Amplifier

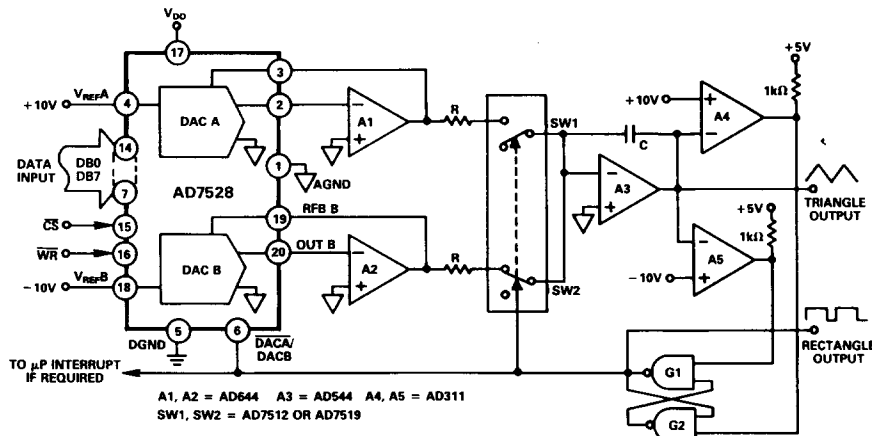


Figure 19. Digitally Programmable Waveform Generator

Where: R_{LDA} and R_{LDB} are DAC A and DAC B R-2R ladder resistances respectively, N_A and N_B are the DAC codes in decimal (1-255).

The resultant gain expression for the circuit is

$$\frac{V_{OUT}}{V_{IN}} = - \frac{256 R_{LDB}}{N_B} \cdot \frac{N_A}{256 R_{LDA}}$$

This simplifies to:

$$\frac{V_{OUT}}{V_{IN}} = - \frac{R_{LDB} \cdot N_A}{R_{LDA} \cdot N_B}$$

But since DAC A and DAC B are a matched pair, $R_{LDA} = R_{LDB}$. This simplifies the expression even further to give:

$$\frac{V_{OUT}}{V_{IN}} = - \frac{N_A}{N_B} \quad \begin{matrix} 1 \leq N_A \leq 255 \\ 1 \leq N_B \leq 255 \end{matrix}$$

Notice that DAC ladder resistance does not appear in the expression. Previous PGA circuits using DACs have always had to be trimmed to accommodate the DAC ladder resistance which usually has a wide tolerance (typically 8k to 20k). This circuit does not suffer from this problem since R_{LDA} and R_{LDB} are matched to better than 1%. Notice also that the circuit has a constant input resistance of R_{LDA} . The two unused feedback resistors, R_{FBA} and R_{FBB} are also precisely matched and could be used to provide other DAC code vs. gain relationships.

PROGRAMMABLE WAVEFORM GENERATOR FOR VECTOR SCAN CRT DISPLAYS

Figure 19 shows the dual DAC in a triangle/rectangle wave generator in which the period of each half cycle can be programmed. Such a circuit is useful for vector scan CRT displays to generate variable rate sweep signals (depending upon whether a long or short vector is to be drawn). DAC A determines the ramp rate for the positive going ramp of the triangle while DAC B determines the ramp rate for the negative going ramp. The integrator output voltage is sensed by comparators A4 and A5. When this voltage reaches $+10V$ or $-10V$ the comparators drive the R-S flip-flop G1 and G2 which selects the output of the appropriate DAC via the double-pole ganged analog switch SW1, SW2.

The switching arrangement shown has the advantage that high speed switches (such as CD 4016 or AD7519) can be used to change between the two DACs without introducing significant output glitches at the changeover.

Furthermore, one DAC can be updated from the data bus and allowed to settle while the output of the other DAC is being used to generate the ramp signal. The output of flip-flop G1 and G2 automatically connects the "unused DAC" to the data bus for further data update if necessary. The output of the flip-flop can be used to drive the interrupts of a microprocessor if required.

Selecting Waveform Parameters:

The period (t) of the waveforms generated by the circuit is given by:

$$t = 512 RC \left[\frac{1}{N_A} + \frac{1}{N_B} \right]$$

where N_A and N_B are the DAC A, DAC B codes in decimal (1–255) respectively.

If DAC A and DAC B latches contain the same codes, the expression simplifies to:

$$t = \frac{1024 RC}{N_A} \text{ i.e., output frequency } f = \frac{N_A}{1024 RC} \text{ Hz}$$

The mark-to-space ratio of the rectangle wave output is dependent on the ratio of N_B to N_A

$$\text{Mark to Space Ratio} = \frac{N_A}{N_B}$$

A special case, exists when the code in either DAC is zero. In this case the circuit will stop oscillating as the integrator input voltage will be zero. If the all zeros condition can occur, it is advisable to connect a $10M\Omega$ resistor from the V_{REF} terminal to the output terminal of each DAC, i.e., V_{REFA} to OUT A and V_{REFB} to OUT B. This provides sufficient bias current to keep the circuit oscillating, and does not affect frequency calculations significantly as the $10M$ resistor introduces only 1/4 LSB of additional error into each DAC output.

AD7528 SINGLE SUPPLY OPERATION

In low budget digital designs requiring analog outputs, the cost of adding an extra power supply rail for the DAC circuits can be a limiting factor. The AD7528 in the single supply configurations shown below provides an ideal cost effective solution for such applications (especially where multiple analog outputs are required).

Single Supply, Voltage Switching Mode:

In this mode, the normal DAC R-2R ladder is inverted. The reference voltage is applied to the DAC OUT A or OUT B terminal and the output voltage is taken from the DAC V_{REFA} or V_{REFB} terminal. For the DACs to retain their specified linearity, the reference voltage range must be restricted as follows:

$$\text{For } V_{DD} = +15V, V_{REF \max} = +2.5V$$

$$\text{For } V_{DD} = +5V, V_{REF \max} = +0.5V$$

Figure 20 shows a circuit for use with a +15 volt power supply giving four separate 0 to +10V outputs. The op-amps used have a Class A output configuration for small signal levels, thus allowing their outputs to go to zero volts for zero volts input. At higher signal levels, the outputs convert to Class B.

Single Supply, Current Steering Mode:

This mode of operation is described in the AD7528 data sheet, and is suitable for single +10 volt to +15 volt supply operation. This is achieved by biasing the AD7528 analog ground (AGND) +5 volts above the power supply ground. Unlike the previous circuits the available drive for the DAC switches is now $V_{DD} - 5$ volts so the 5 volt specifications apply for linearity. Figure 21 shows how a +2 volt to +8 volt analog output may be obtained using two op-amps per DAC. The two DAC reference inputs are tied

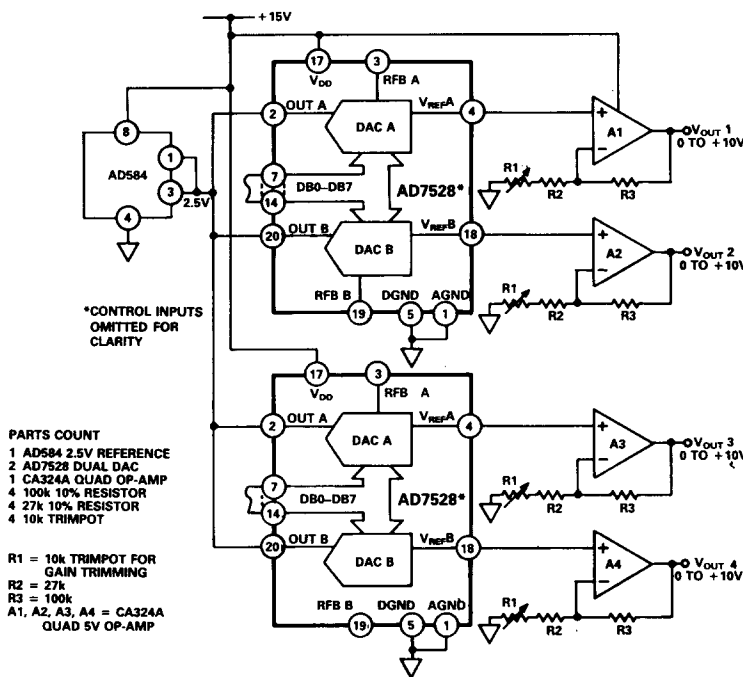


Figure 20. Four Channel Analog Output Circuit

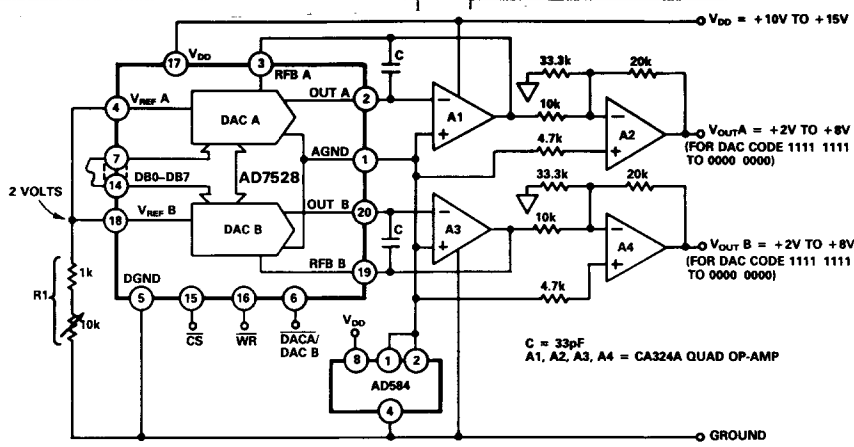


Figure 21. AD7528 Single Supply Operation with AGND Biased to +5 Volts

together and a reference input voltage is obtained without a buffer amplifier by making use of the constant and matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1; R1 is adjusted until V_{REFA} and V_{REFB} inputs are at +2 volts. The adjustment is independent of either DAC code.

Each analog output channel has a +2 to +8 volt range for DAC codes 1111 1111 to 0000 0000.

Reference

Dan H. Sheingold, "Nonlinear Circuits Handbook," available from Analog Devices.

D. P. Burton, Application Note "Methods For Generating Complex Waveforms And Vectors Using Multiplying D/A Converters" Analog Devices Publication Number: E671-15-9/81.

Application Guide to CMOS Multiplying D/A Converters, Analog Devices Publication Number: G479-15-8/78.