

Power-Down Circuit Cuts Power to AD7769 and AD7774

by John Wynne

Both the AD7769 and the AD7774, I/O ports intended for HDD servo applications, operate off of +5 V and +12 V supply voltages. Although neither of these devices offer power-down as a standard feature, implementing such a function external to the devices is simple and inexpensive. Figure 1 shows the suggested circuit. The +5 V and +12 V supplies are switched off by means of MOSFETs, Q1 and Q2, in series with the supplies; however, the sequencing of these supplies going into power-down and coming out of power-down is also important, and this is handled by the cross-coupled NOR gates and their output delays. The diode protection schemes recommended in the AD7769 and AD7774 data sheets to protect against power supply mis-sequencing are now redundant when this power-down circuit is used.

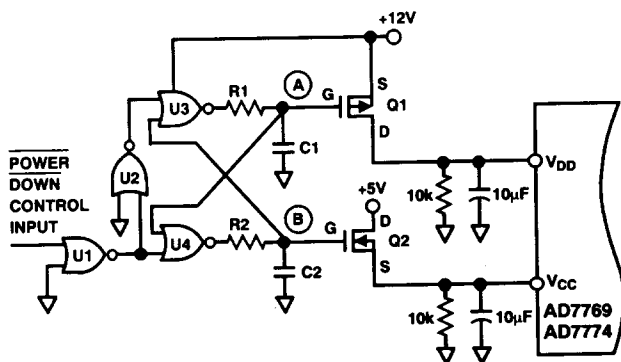


Figure 1. Power-Down Circuit with Correct Power Supply Sequencing

Figure 2 shows the power on/off control input and the resulting gate voltages, A and B. The P-channel Q1 is ON for a negative gate-source voltage while the N-channel Q2 is ON for a positive gate-source voltage.

In the power-down mode (POWER DOWN control input low) the output of U4 is low giving a Q2 gate-source voltage of V_{OL} , typically 50 mV with $V_{CC} = 12$ V on a CD4001, which is too small to turn on Q2. Similarly, the output of U3 is high giving a Q1 gate-source voltage of $V_{OH} - 12$ V, typically -50 mV, again too small to turn on Q1.

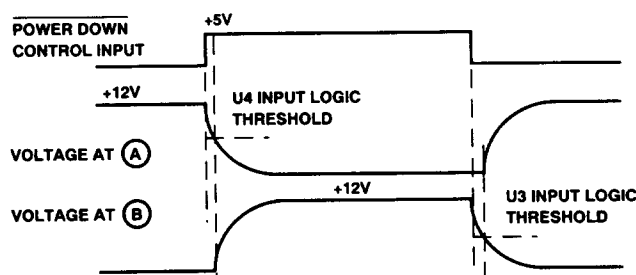


Figure 2. Typical Voltage Waveforms for Figure 1

Coming out of the power-down mode (POWER DOWN control input brought high) the output of U3 goes low and capacitor C1 discharges exponentially to V_{OL} with time constant $R1C1$ to turn Q1 ON. When the voltage level across C1 drops to the logic input threshold of gate U4, the output of U4 goes high and capacitor C2 charges exponentially to V_{OH} , approximately 12 V, to turn Q2 ON. Thus Q1 turns ON before Q2 turns ON.

Going into the power-down mode (POWER DOWN control input brought low) the RC delays work in reverse, capacitor C2 being discharged to the logic input threshold voltage of U3 before capacitor C1 is allowed to charge. Hence, Q2 turns OFF before Q1 turns OFF.

Power supply decoupling capacitors for the AD7769 and AD7774 should remain on the V_{DD} and V_{CC} pins of the devices. The 10 kΩ resistors from V_{DD} and V_{CC} to ground are not vital to the performance of the circuit but simply act to weakly pull the V_{DD} and V_{CC} pins to ground in order to discharge the decoupling capacitors. The CD4001 quad NOR gate must be powered from a 12 V supply which remains alive during power-down of the I/O port.

Figures 3 and 4 show actual V_{DD} and V_{CC} waveforms for the AD7769 when powering up (Figure 3) and powering down (Figure 4) using the circuit of Figure 1. For these photographs, $R_1 = R_2 = 1\text{ k}\Omega$, $C_1 = C_2 = 150\text{ pF}$, $Q_1 = \text{VP0300M}$ and $Q_2 = \text{VN0300M}$.

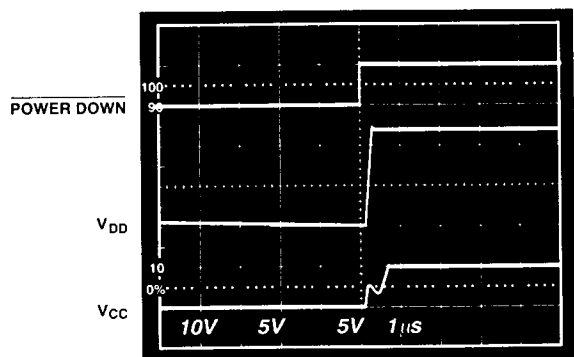


Figure 3. V_{DD} & V_{CC} Waveforms on Power-Up

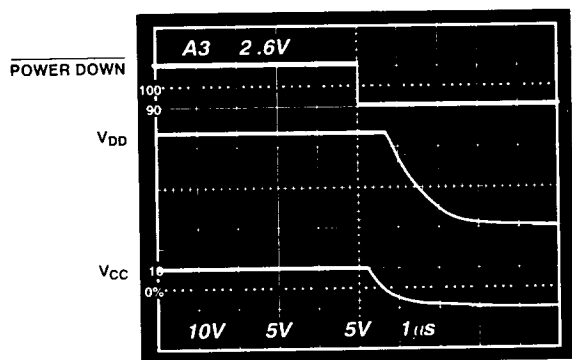


Figure 4. V_{DD} & V_{CC} Waveforms on Power-Down

Tables I and II demonstrate the effectiveness of the circuit in shutting off all power to the AD7769 and AD7774 I/O ports.

Table I. Effectiveness of Power-Down Circuit with AD7769

Control Input	I_{DD}	I_{CC}
High (Power On)	17.5 mA	1.94 mA
Low (Power Off)	3 μA	0

Table II. Effectiveness of Power-Down Circuit with AD7774

Control Input	I_{DD}	I_{CC}
High (Power On)	20.5 mA	3.24 mA
Low (Power Off)	3 μA	0

Additionally, under normal operating conditions, small voltage drops occur across the ON-resistance, $R_{DS(ON)}$, of transistors Q1 and Q2. Table III compares the voltage drops generated across two popular types of N-channel and P-channel MOSFETs measured using the AD7769.

Table III. Comparison of MOSFET Performance for Q1, Q2

Transistor	V_{DS}	Effective $R_{DS(ON)}$
Q1, VP0300M*	28 mV	1.6 Ω
Q2, VN0300M*	2 mV	1.03 Ω
Q1, ZVP2106A**	46.9 mV	2.28 Ω
Q2, ZVN3306A**	7.3 mV	3.76 Ω

*Siliconix Inc.

**Zetex, Inc.