

### Features

The TDA 6611 represents a complete TV stereo system controlled by the I<sup>2</sup>C bus.

- All functions inclusive matrix adjustment are I<sup>2</sup>C bus controlled
- SCART-Interface
- Independent headphones
- Higher signal noise ratio
- Extremely low distortion
- High security rate against mis-switching of the decoder performed by the digital interference suppression and the very narrow bandwidth

Type	Ordering Code	Package
TDA 6611	Q67000-A8260	P-DIP-28

The IC is divided into three functional blocks

#### 1) Stereo sound processing with high quality (exceeds DIN 45500; suitable for NI-CAM and CD)

- a) matrix for G standard with crosstalk compensation controlled via the I<sup>2</sup>C Bus
- b) additional single-channel AF input (for e.g. AF signal accord. L standard)
- c) stereo SCART interface in accordance with FTZ official brochure
- d) stereo loudspeaker signal section with Ch1/Ch2 switch, high/low regulation, quasi-stereo/stereo basic processing and separate loudspeaker regulation for left and right
- e) signal section with Ch1/Ch2 switch and loudspeaker regulation for stereo headphones

#### 2) TV sound identification signal decoder consisting of:

- a) active pilot signal filter
- b) phase-independent rectifier with very narrow bandwidth for evaluation of the identification signal
- c) digital integrator to reduce interference
- d) multiplexer for cyclical switch over between "stereo" or "dual" evaluation
- e) PLL for the generation of the reference signal. External synchronization with either the flyback pulse or external reference clock signals of 62.5 kHz or 4 MHz can also be generated using the internal crystal generator with an external crystal.

### 3) Control section for:

- a) I<sup>2</sup>C bus interface with listener/talker function
- b) control of the complete AF sound processing
- c) control of the identification signal decoder
- d) reading of the identification signal decoder
- e) test modes

## Circuit Description

### Signal Section

The audio signal processing in the matrix and the switch-over for multichannel TV sound signals according to the two-carrier system used in Germany takes place in the matrix and switching sections. Crosstalk compensation is carried out in the Sound 1 input. The compensation range has an adjustment range of  $\pm 3$  dB with a minimum step of 0.2 dB. In addition to the two inputs for the demodulated sound carrier, a two-channel scart input and an additional mono input (e.g. for demodulated L-standard sound) are provided. The two AF inputs can be bypassed internally in such a way that decoded stereo sound signals of other audio systems (NICAM) can be processed. The switching section is terminated with the SCART output and an independently switchable Ch1/Ch2 switch for the loudspeaker and headphone outputs.

In the loudspeaker signal path a switchable quasi-stereo section follows the Ch1/Ch2 switch. This section gives a special audio effect with mono signals due to a 180° phase shift at medium frequencies (about 1 kHz) in one channel. The following base control exhibits a step of 3 dB with an adjustment range of +15/-12 dB. The cutoff frequency is set for each channel with an external capacitor. The circuit for stereo basewidth expansion, which, with switchable stereo signals, provides a more special audio effect due to 50 % of frequency dependent crosstalk in opposing phases, operates with the same cutoff frequency as the base control, but the function is largely independent. The treble control, whose cutoff frequency is also controlled by a capacitor in each channel, also has a step of 3 dB with an adjustment range of  $\pm 12$  dB. The loudspeaker signal path is terminated with a loudspeaker control, independently adjustable for left and right. With 57 steps of 1.25 dB the adjustment range is 70 dB, where step 57 activates the "MUTE" function. Functions such as "balance" or "loudness" are realized by software adjustment of the appropriate tone and volume controls.

The signal path for the headphones contains a volume control after the Ch1/Ch2 switch with a common adjustment for left and right. Thirty-two steps of 2 dB give an adjustment range of 62 dB ( $31 \times 2$  dB = 62 dB, the 32nd step is MUTE).

### Identification Signal Decoder

The input of the identification signal decoder consists of an op-amp for the pilot signal with its sidebands. An external LC circuit is used. The signal is then passed to a phase-independent active bandpass filter with a very narrow bandwidth (adjustable externally). This filter detects whether the lower sideband of the pilot carrier, which is modulated with the identification signal, is present. The center frequency of the filter is switched between "dual" and "stereo" by a multiplexer. The multiplexing frequency is adjustable by software. If a sideband is detected, the multiplexer stops. The first "detected" criterion is rendered free from interference by a digital integrator with a following comparator and can be read out via I<sup>2</sup>C bus (talk mode) as the "stereo" or "dual" mode. The control of the corresponding signal can be either directly internally or through the  $\mu$ C. All the necessary clock signals are derived from a fast settling PLL which is synchronized by a reference frequency. This reference frequency must be sufficiently close to the horizontal frequency, but a **rigid phase coupling is not required**. Therefore, alternatively the use of a crystal-controlled 62.5-kHz frequency commonly found in PLL tuning systems is possible.

## Control Section

All functions are controlled via I<sup>2</sup>C bus interface with listen/talk functions. The current applicable data are stored in a block of latches.

The telegram structure is formed in the following manner:

start condition – chip address – any number of bytes – stop condition

The following conditions apply to the data bytes:

Before the actual data byte (with the adjustment information), a subaddress by the I<sup>2</sup>C bus byte must **always** be transmitted. This byte is however interpreted by the I<sup>2</sup>C bus as a data byte interface.

Example: The headphone volume is to be increased in a number of steps.

### Right

start condition  
chip address 84 (hex)  
subaddr. vol. HP 03 (hex)  
vol. step 8 08 (hex)  
subaddr. vol. HP 03 (hex)  
vol. step 9 09 (hex)  
subaddr. HP 03 (hex)  
vol. step 10 0A (hex)  
stop condition

### Wrong

start condition  
chip address 84 (hex)  
subaddr. vol HP 03 (hex)  
vol. step 8 08 (hex)  
vol. step 9.09 (hex)  
vol. step 10 0A (hex)  
stop condition

Within a telegram (i.e. without a new start condition) any different subaddresses can be accessed. The changeover between "listen" and "talk" must however always occur via the sequence stop condition – start condition – chip address. Before each readout always a start condition and chip address (talk) must be transmitted. The data to be read out are loaded into the I<sup>2</sup>C bus interface and can be transferred to the  $\mu$ C.

## Chip Address

MSB	.	.	.	.	.	.	LSB
1	0	0	0	0	1	0	R/W

R/W = 0 → read (listen)

R/W = 1 → write (talk)

## Subaddress Bytes

	MSB	.	.	.	.	.	LSB	
Vol. of left speaker	X	X	X	X	X	0	0	1
Vol. of right speaker	X	X	X	X	X	0	1	0
Vol. of headphones	X	X	X	X	X	0	1	1
Treble/bases	X	X	X	X	X	1	0	1
Switch byte I	X	X	X	X	X	1	1	1
Switch byte II	X	X	X	X	X	0	0	0
Crosstalk compensation	X	X	X	X	X	1	1	0

**Setting Bytes****a) Volume of left/right loudspeaker**

	MSB	.	.	.	.	.	.	LSB
Maximum volume	X	X	1	1	1	1	1	1
Max - 1	X	X	1	1	1	1	1	0
Max - 15	X	X	1	1	0	0	0	0
Max - 55	X	X	0	0	1	0	0	0
MUTE	X	X	0	0	0	1	1	1
MUTE	X	X	0	0	0	0	0	0
MUTE	X	X	0	0	0	X	X	X
Power on	0	0	0	0	0	0	0	1

**b) Volume of headphones**

	MSB	.	.	.	.	.	.	LSB
Max. volume	T2	T1	T0	1	1	1	1	1
Max - 1	T2	T1	T0	1	1	1	1	0
Max - 15	T2	T1	T0	1	0	0	0	0
Max - 31	T2	T1	T0	0	0	0	0	1
MUTE	T2	T1	T0	0	0	0	0	0
Power on	0	0	0	0	0	0	0	1

T0-T2 are test bits; these must be set to 0 for normal operation

**c) Crosstalk compensation matrix (sound 1)**

	MSB	.	.	.	.	.	.	LSB
Max. amplification	X	X	X	1	1	1	1	1
Max - 1	X	X	X	1	1	1	1	0
Gain 0 dB	X	X	X	1	0	0	0	0
Min. gain	X	X	X	0	0	0	0	1
Min. gain	X	X	X	0	0	0	0	X
Power on	0	0	0	0	0	0	0	1

**d) Treble/bass**

	MSB	.	.	.	.	.	.	LSB
Linear	1	0	0	0	1	0	0	0
Max. treble, lin. bass	1	1	0	0	1	0	0	0
Max. treble, lin. bass	1	1	X	X	1	0	0	0
Min. treble, lin. bass	0	1	0	0	1	0	0	0
Min. treble, lin. bass	0	0	X	X	1	0	0	0
Lin. treble, max. bass	1	0	0	0	1	1	0	1
Lin. treble, max. bass	1	0	0	0	1	1	X	1
Lin. treble, max. bass	1	0	0	0	1	1	1	X
Lin. treble, min. bass	1	0	0	0	0	1	0	0
Lin. treble, min. bass	1	0	0	0	0	0	X	X
Max. treble, max. bass	1	1	X	X	1	1	X	1
Min. treble, min. bass	0	0	X	X	0	0	X	X
Power on	0	0	0	0	0	0	0	1
	MSB			LSB	MSB			LSB
	treble			treble	bass			bass

**e) Switch byte I**

MSB

LSB

MUTE I MUTE II < Ch1/Ch2<sub>vol</sub> Ch1/Ch2<sub>HP</sub> Mono SCART SCART-D AM  
 MUTE I = 0 All AF outputs are muted (speakers, headphones, SCART); power on  
 MUTE I = 1 All AF outputs on  
 MUTE II = 0 Loudspeaker outputs muted; power on  
 MUTE II = 1 Loudspeaker outputs on  
 MUTE I and MUTE II are OR gated with respect to the loudspeaker outputs

MUTE I	MUTE II	loudspeaker outputs	headphones, SCART o/p
0	0	muted	muted
0	1	muted	muted
1	0	muted	on
1	1	on	on

Ch1/Ch2<sub>vol</sub> = 0 Sound 1 on the loudspeaker outputs; power on  
 Ch1/Ch2<sub>vol</sub> = 1 Sound 2 on the loudspeaker outputs  
 Ch1/Ch2<sub>HP</sub> = 0 Sound 1 on the headphone outputs; power on  
 Ch1/Ch2<sub>HP</sub> = 1 Sound 2 on the headphone outputs

Ch1/Ch2<sub>vol</sub> and Ch1/Ch2<sub>HP</sub> are only effective if the matrix is set to the position "dual sound".

Mono = 0 identification signal decoder is set to the position mono and held; power on  
 Mono = 1 normal operation of ID signal decoder  
 SCART = 0 normal TV operation; power on  
 SCART = 1 SCART playback; connection of SCART inputs – AF outputs. SCART = 1 has priority over AM = 1 (loudspeaker and headphones)  
 SCART-D = 0 SCART playback stereo (mono); power on  
 SCART-D = 1 Enable for the Ch1/Ch2 switch during SCART playback (only effective when SCART = 1)  
 AM = 0 normal operation (G standard)  
 AM = 1 AM AF input is activated; power on  
 AM = 1 has priority over Bypass = 1

**f) Switch byte II**

MSB								LSB
MPX0	MPX1	quasi-st	Be	H pul	Matrix 0	Matrix 1	Bypass	
MPX0	MPX1	MPX period						recommended $C_{25,26}$
0	0	2 s					power on	1 $\mu$ F
0	1	4 s						2.2 $\mu$ F
1	0	8 s						4.7 $\mu$ F
1	1	1 s						470 nF

MPX period = 2 s signifies: ID signal decoder searches 1 second dual and 1 second stereo

Quasi-st	= 0	Quasi-stereo off; power on
Quasi-st	= 1	Quasi-stereo on
Be	= 0	stereo basewidth expansion off; power on
Bb	= 1	stereo basewidth expansion on;
H pul	= 0	ID signal decoder synchronization with $f_H = 15.625$ kHz; power on
H pul	= 1	ID synchronization with $4 \times f_H$
Matrix 0	Matrix 1	matrix status
0	0	mono power on
0	1	stereo
1	0	dual
1	1	automatic according to ID signal decoder
Bypass	= 0	normal operation (G standard)
Bypass	= 1	matrix is bridged so that left/right signals can be fed in; power on (AM = 1 has priority over Bypass = 1)

**Priority list of setting bits**

1. MUTE I
2. MUTE II (only with regard to the loudspeaker output)
3. SCART
4. AM
5. Bypass
6. Matrix 0, 1

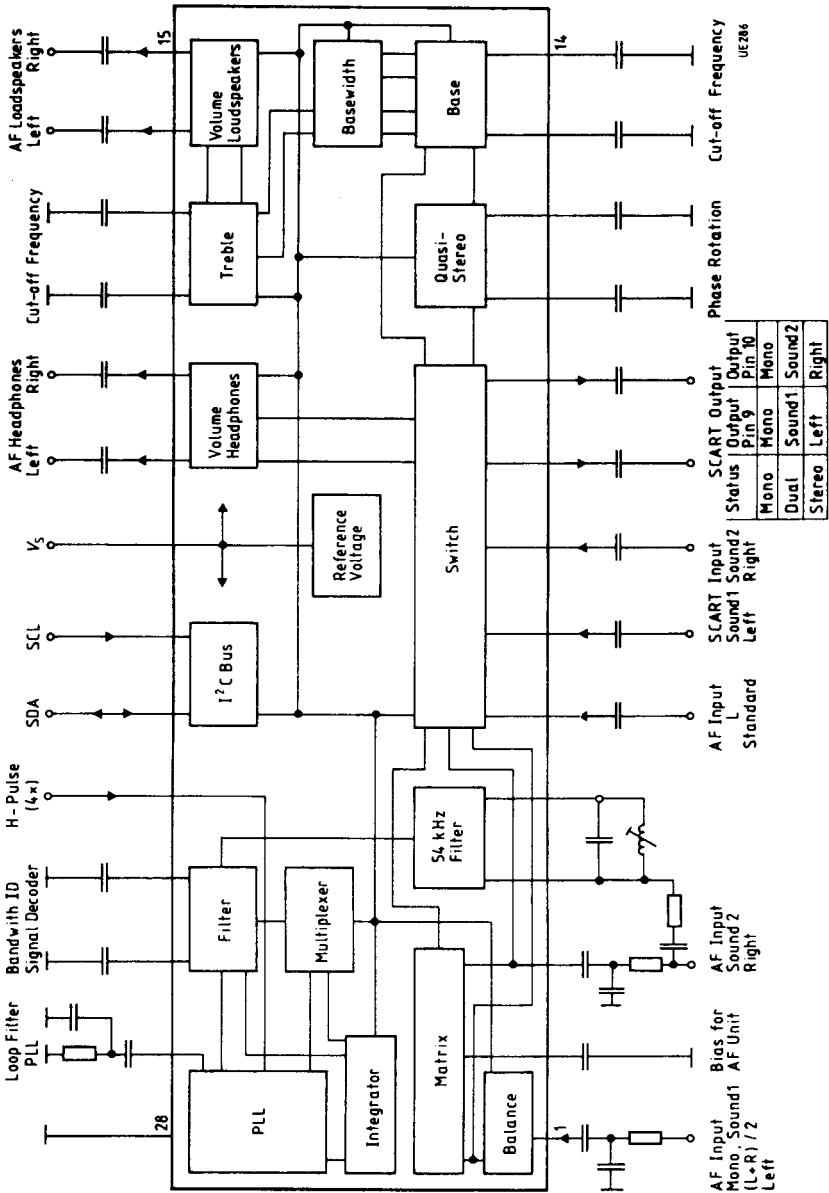
**g) Talk mode**

MSB							LSB
St	D	T5	T4	T3	X	X	X
0	0	decoder detects mono					
1	0	decoder detects stereo					
0	1	decoder detects dual					
1	1	internally inhibited					

T3 – T5 are test bits



Block Diagram

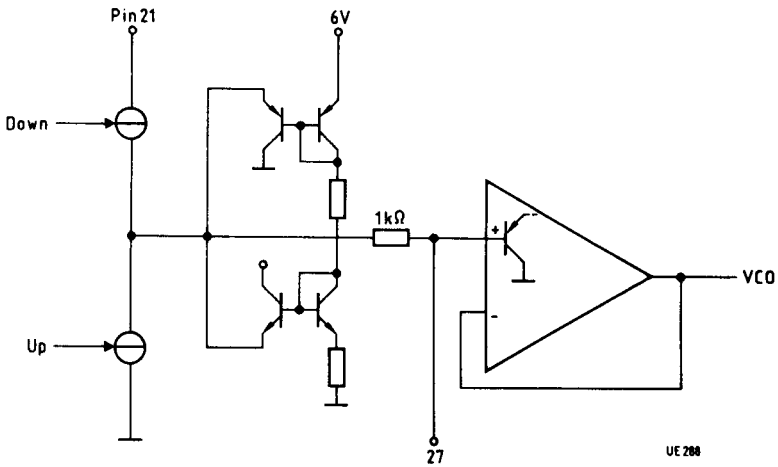


**Pin Functions**

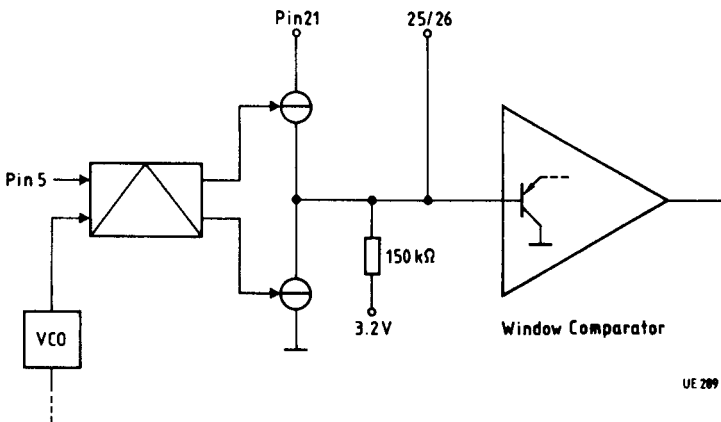
<b>Pin No.</b>	<b>Function</b>
1	AF input mono, left, sound 1 (may be balanced)
2	Bias for AF operating point
3	AF input right, sound 2
4	54-kHz input
5	54-kHz filter
6	AF input (L standard)
7	AF input SCART left (sound 1)
8	AF input SCART right (sound 2)
9	AF output SCART (mono, sound 1, left)
10	AF output SCART (mono, sound 2, right)
11	Phase-shifter quasi-stereo
12	Phase-shifter quasi-stereo
13	Cutoff frequency base (basewidth) left
14	Cutoff frequency base (basewidth) right
15	AF output, loudspeaker left
16	AF output, loudspeaker right
17	Cutoff frequency treble left
18	Cutoff frequency treble right
19	AF output, headphones left
20	AF output, headphones right
21	Supply voltage
22	I <sup>2</sup> C bus SCL
23	I <sup>2</sup> C bus SDA
24	Input H pulse (4 × H pulse)
25	Filter ID signal decoder
26	Filter ID signal decoder
27	PLL filter ID signal decoder
28	Ground

**Pin Functions**

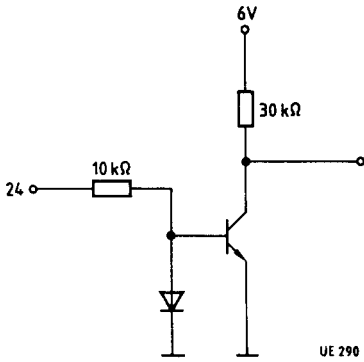
**PLL Filter ID Signal Decoder (Pin 27)**



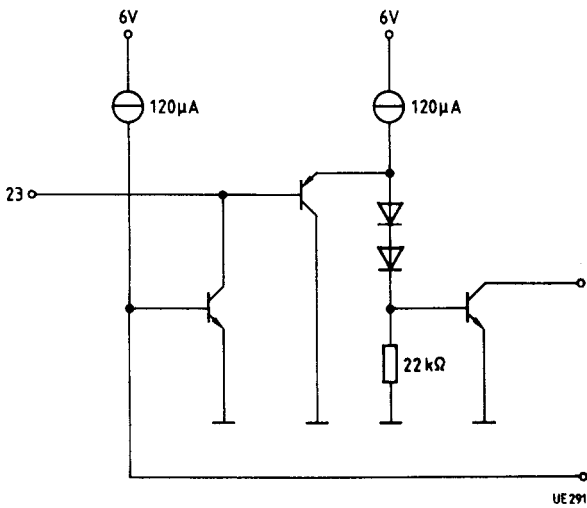
**Filter ID Signal Decoder (Pin 25/26)**



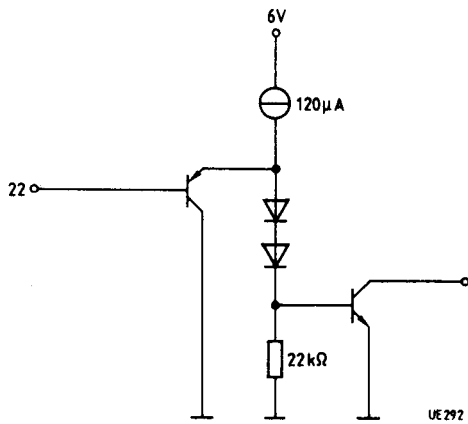
Input H Pulse (Pin 24)



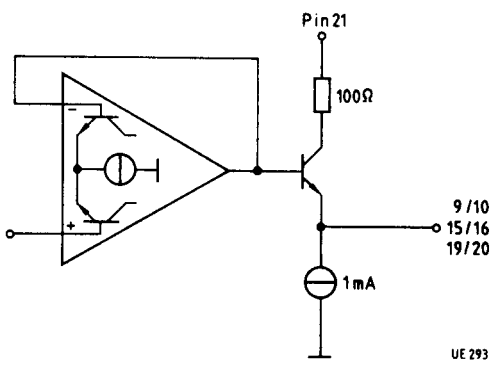
I<sup>2</sup>C Bus SDA (Pin 23)



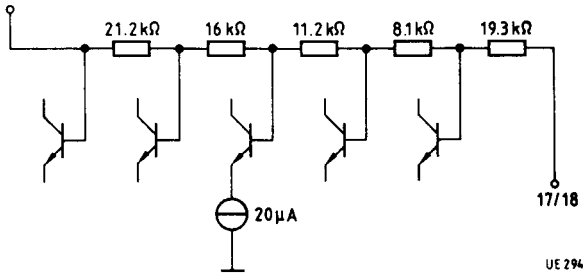
I<sup>2</sup>C Bus SCL (Pin 22)



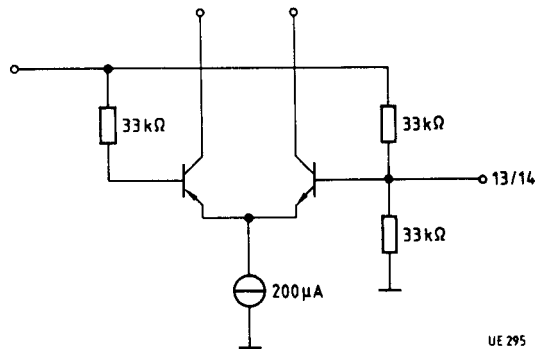
AF Outputs Headphones (Pin 19/20)  
Loudspeaker (Pin 15/16)  
SCART (Pin 9/10)



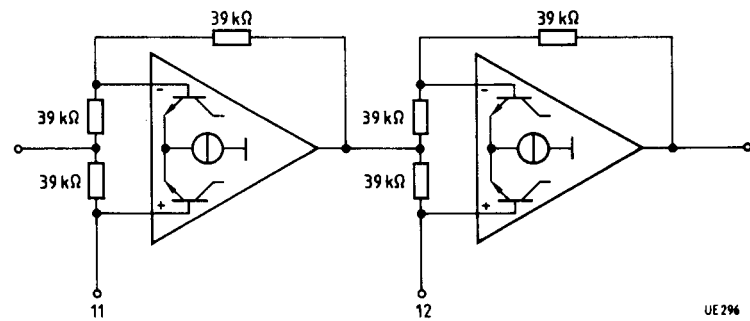
**Cutoff Frequency Treble (Pin 17/18)**



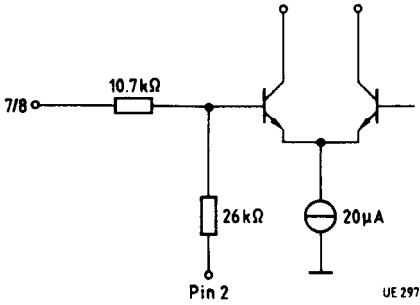
**Cutoff Frequency Bass (Pin 13/14)**



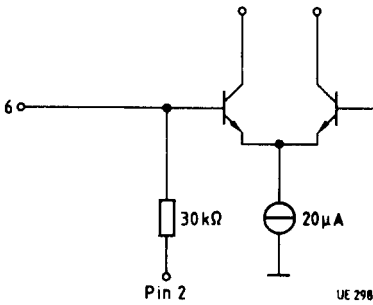
**Phase Advancer Quasi Stereo (Pin 11/12)**



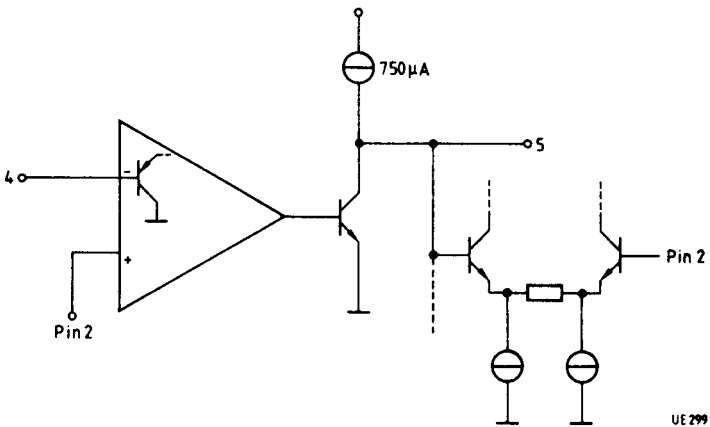
**AF Inputs SCART (Pin 7/8)**



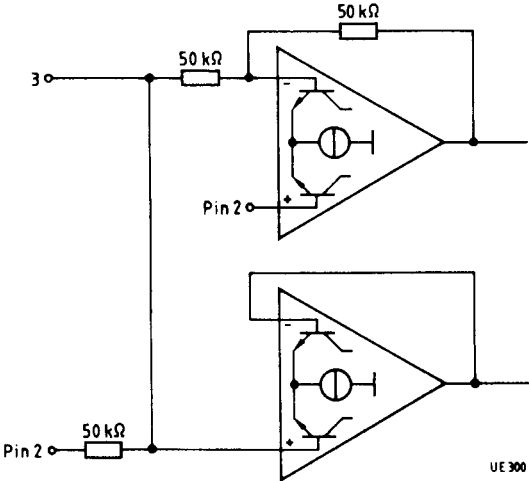
**AF Input AM (Pin 6)**



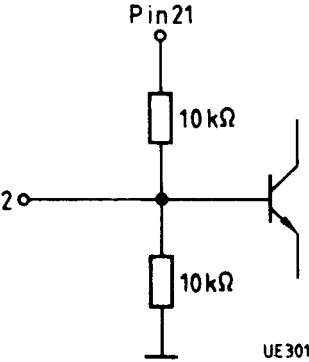
**54 – kHz Filter (Pin 4/5)**



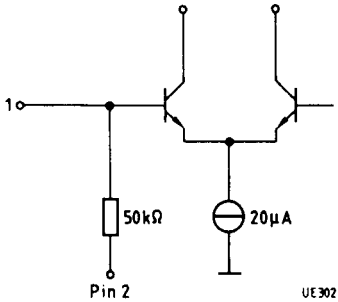
AF Input (Pin 3)



Input for AF Unit Bias Blocking Capacitor (Pin 2)



AF Input (Pin 1)





**Absolute Maximum Ratings** $T_A = 25\text{ °C}$ 

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$V_{21}$	0	14	V
Max. DC voltage	$V_1$	0	$V_{21}$	V
Max. DC voltage	$V_2$	0	$V_{21}$	V
Max. DC voltage	$V_3$	0	$V_{21}$	V
Max. DC voltage	$V_4$	0	$V_{21}$	V
Max. DC voltage	$V_6$	0	$V_{21}$	V
Max. DC voltage	$V_7$	0	$V_{21}$	V
Max. DC voltage	$V_8$	0	$V_{21}$	V
Max. DC voltage	$V_{11}$	0	$V_{21}$	V
Max. DC voltage	$V_{12}$	0	$V_{21}$	V
Max. DC voltage	$V_{12}$	0	$V_{21}$	V
Max. DC voltage	$V_{14}$	0	$V_{21}$	V
Max. DC voltage	$V_{17}$	0	$V_{21}$	V
Max. DC voltage	$V_{18}$	0	$V_{21}$	V
Max. DC voltage	$V_{22}$	0	$V_{21}$	V
Max. DC voltage	$V_{23}$	0	$V_{21}$	V
Max. DC voltage	$V_{24}$	0	$V_{21}$	V
Max. DC voltage	$V_{25}$	0	$V_{21}$	V
Max. DC voltage	$V_{26}$	0	$V_{21}$	V
Max. DC current	$I_5$	0	2	mA
Max. DC current	$I_9$	0	2	mA
Max. DC current	$I_{10}$	0	2	mA
Max. DC current	$I_{15}$	0	2	mA
Max. DC current	$I_{16}$	0	2	mA
Max. DC current	$I_{19}$	0	2	mA
Max. DC current	$I_{20}$	0	2	mA
Max. DC current	$I_{27}$	0	1	mA
Junction temperature	$T_j$		150	°C
Storage temperature	$T_{slg}$	- 40	125	°C
Thermal resistance (system-ambient)	$T_{th SA}$		53	K/W

**Operating Range**

Supply voltage	$V_6$	10	13.2	V
Ambient temperature	$T_A$	0	70	°C
Input frequency range	$f$	0.01	20	kHz

**Characteristics**

$V_S = 12\text{ V}$ ;  $T_A = 25\text{ }^\circ\text{C}$ , in accordance with test circuit 1

I<sup>2</sup>C bus present: start-84-01,3F-0 2,3F-0 3,1F-0 5,88-0 6,10-07,C8-00,01-stop

Chip address - Vol<sub>LS</sub>63-Vol<sub>LS</sub>63.-.Vol<sub>HP</sub>31 - tone lin - adj 0dB - MUTE I,MUTE II, mono-bypass

The basic setting for each point in the specification is always preset; only settings which deviate from this are given in the test conditions. Details in *italics* only provide explanation of the hexadecimal code and with switch bits on the set bits and features are stated.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	$I_{21}$		50		mA	

**Signal Section**

Max. gain	$V_{16-1}$	-2	0	2	dB	
Max. gain	$V_{15-3}$	-2	0	2	dB	
Max. gain	$V_{20-1}$	-2	0	2	dB	
Max. gain	$V_{19-3}$	-2	0	2	dB	
Max. gain	$V_{16-3}$	-2	0	2	dB	00,02; $V_1 = 01$ Matrix: stereo
Max. gain	$V_{15-3}$	-2	0	2	dB	00,02; $V_1 = 01$ Matrix: stereo
Max. gain	$V_{20-3}$	-2	0	2	dB	00,02; $V_1 = 0$ Matrix: stereo
Max. gain	$V_{19-3}$	-2	0	2	dB	00,02; $V_1 = 0$ Matrix: stereo
Max. gain	$V_{16-1}$	4	6	8	dB	00,02; $V_3 = 0$ Matrix: stereo
Max. gain	$V_{20-1}$	4	6	8	dB	00,02; $V_3 = 0$ Matrix: stereo
Max. gain	$V_{16-7}$	-5	-3	-1	dB	07,CC, SCART
Max. gain	$V_{15-8}$	-5	-3	-1	dB	07,CC, SCART
Max. gain	$V_{20-7}$	-5	-3	-1	dB	07,CC, SCART
Max. gain	$V_{19-8}$	-5	-3	-1	dB	07,CC, SCART
Max. gain	$V_{16-6}$	-2	0	2	dB	07,C9, AM
Max. gain	$V_{15-6}$	-2	0	2	dB	07,C9, AM
Max. gain	$V_{20-6}$	-2	0	2	dB	07,C9, AM
Max. gain	$V_{19-6}$	-2	0	2	dB	07,C9, AM
Gain	$V_{9-1}$	-2	0	2	dB	
Gain	$V_{10-3}$	-2	0	2	dB	
Gain	$V_{9-3}$	-2	0	2	dB	00,02; $V_1 = 0$ Matrix: stereo
Gain	$V_{10-3}$	-2	0	2	dB	00,02; $V_1 = 0$ Matrix: stereo
Gain	$V_{9-1}$	4	6	8	dB	00,02; $V_3 = 0$ Matrix: stereo

**Characteristics (cont'd)** $V_S = 12\text{ V}$ ;  $T_A = 25\text{ }^\circ\text{C}$ , in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Gain	$V_{10-6}$	-2	0	2	dB	07,C9, AM
Gain	$V_{9-6}$	-2	0	2	dB	07,C9, AM
Min. gain	$V_{16-1}$		-70		dB	01,08-02,08 VolLSI8-VolLSr8
Min. gain	$V_{15-3}$		-70		dB	01,08-02,08 VolLSI8-VolLSr8
Min. gain	$V_{20-1}$		-62		dB	01,08-02,08 03,01 Vol HP1
Min. gain	$V_{19-3}$		-62		dB	03,01 Vol HP1
Min. gain	$V_{16-7}$		-73		dB	07,CC-01,08-02,08 SCART-VolLSI8-VolLSr8
Min. gain	$V_{15-8}$		-73		dB	07,CC-01,08-02,08 SCART-VolLSI8-VolLSr8
Min. gain	$V_{20-7}$		-65		dB	07,CC-03,01 SCART-VolKH1
Min. gain	$V_{19-8}$		-65		dB	07,CC-03,01 SCART-VolKH1
Min. gain	$V_{16-6}$		-70		dB	07,C9-01,08-02,08 AM-VolLSI8-VolLSr8
Min. gain	$V_{15-6}$		-70		dB	07,C9-01,08-02,08 AM-VolLSI8-VolLSr8
Min. gain	$V_{20-6}$		-62		dB	07,C9-03,01 SCART-VolKH1
Min. gain	$V_{19-6}$		-62		dB	07,C9-03,01 SCART-VolKH1
Flutter and wow	$\Delta V_{15-16}$			$\pm 2$	dB	01,3F to 01,24 02,3F to 02,24 $Vol_{LSr}63-36 - Vol_{LSr}63-36$
Flutter and wow	$\Delta V_{19-20}$			$\pm 2$	dB	03,1F to 03,13 $Vol_{KH}31-19$
Step width Vol <sub>15</sub>	$\Delta V_{15}$	0	1.25	2.5	dB	01,X-01,(X $\pm$ 1) $Vol_{LSr}X - Vol_{LSr}(X\pm 1)$
Step width Vol <sub>16</sub>	$\Delta V_{16}$	0	1.25	2.5	dB	02,X-02,(X $\pm$ 1) $Vol_{LSr}X - Vol_{LSr}(X\pm 1)$
Step width Vol <sub>19</sub>	$\Delta V_{19}$	0	2	4	dB	03,X-03,(X $\pm$ 1) $Vol_{KH}X - Vol_{KH}(X\pm 1)$
Step width Vol <sub>20</sub>	$\Delta V_{20}$	0	2	4	dB	03,X-03,(X $\pm$ 1) $Vol_{KH}X - Vol_{KH}(X\pm 1)$

## Characteristics (cont'd)

 $V_S = 12\text{ V}$ ;  $T_A = 25\text{ }^\circ\text{C}$ , in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Matrix adjustment	$V_{16-1}$	2.5	3	3.5	dB	06, 1F, <i>Adjust. max</i>
Matrix adjustment	$V_{20-1}$	2.5	3	3.5	dB	06, 1F, <i>Adjust. max</i>
Matrix adjustment	$V_{9-1}$	2.5	3	3.5	dB	06, 1F, <i>Adjust. max</i>
Matrix adjustment	$V_{16-1}$	- 3.5	- 3	- 2.5	dB	06, 01, <i>Adjust. min</i>
Matrix adjustment	$V_{20-1}$	- 3.5	- 3	- 2.5	dB	06, 01, <i>Adjust. min</i>
Matrix adjustment	$V_{9-1}$	- 3.5	- 3	- 2.5	dB	06, 01, <i>Adjust. min</i>
Adjust. step wide	$\Delta V_{16}$	0.1	0.2	0.3	dB	06, X- 06( $X \pm 1$ ) <i>Adjust.X -Adjust.(X <math>\pm 1</math>)</i>
Adjust. step wide	$\Delta V_{20}$	0.1	0.2	0.3	dB	06, X- 06( $X \pm 1$ ) <i>Adjust.X -Adjust.(X <math>\pm 1</math>)</i>
Adjust. step wide	$\Delta V_9$	0.1	0.2	0.3	dB	06, X- 06( $X \pm 1$ ) <i>Adjust.X -Adjust.(X <math>\pm 1</math>)</i>
Bass boost	$V_{16-1}$	13	15		dB	05,8F; $f_i = 40\text{ Hz}$ <i>Bass max, treble lin.</i>
Bass boost	$V_{15-3}$	13	15		dB	05,8F; $f_i = 40\text{ Hz}$ <i>Bass max, treble lin.</i>
Bass boost	$V_{16-1}$		- 12		dB	05,8 0; $f_i = 40\text{ Hz}$ <i>Bass min, treble lin.</i>
Bass boost	$V_{15-3}$		- 12		dB	05,8 0; $f_i = 40\text{ Hz}$ <i>Bass min, treble lin.</i>
Step wide bass	$\Delta V_{15}$	1	3	5	dB	05,8X- 05,8( $X \pm 1$ ) <i>Bass X-bass(X <math>\pm 1</math>)</i>
Step wide bass	$\Delta V_{16}$	1	3	5	dB	05,8X- 05,8( $X \pm 1$ ) <i>Bass X-bass(X <math>\pm 1</math>)</i>
High-frequency emphasis	$V_{16-1}$	10	12		dB	05,8 $f_i = 15\text{ kHz}$ <i>Treble max, bass lin.</i>
High-frequency emphasis	$V_{15-3}$	10	12		dB	05,8 $f_i = 15\text{ kHz}$ <i>Treble max, bass lin.</i>
High-frequency emphasis	$V_{16-1}$		- 12		dB	05, 08 $f_i = 15\text{ kHz}$ <i>Treble min, bass lin.</i>
High-frequency emphasis	$V_{15-3}$		- 12		dB	05, 08 $f_i = 15\text{ kHz}$ <i>Treble min, bass lin.</i>
Step wide treble	$\Delta V_{15}$	1	3	5	dB	05,X8- 05,( $X \pm 1$ )8 <i>Treble X-treble(X <math>\pm 1</math>)</i>
Step wide treble	$\Delta V_{16}$	1	3	5	dB	05,X8- 05,( $X \pm 1$ )8 <i>Treble X-treble(X <math>\pm 1</math>)</i>
Linearity sound	$\Delta V_{15}$			$\pm 2$	dB	05,88; $f_i = 40\text{ Hz}$ -15 kHz <i>Treble, bass lin.</i>
Linearity sound	$\Delta V_{16}$			$\pm 2$	dB	05,88; $f_i = 40\text{ Hz}$ -15 kHz <i>Treble, bass lin.</i>

**Characteristics (cont'd)** $V_S = 12\text{ V}$ ;  $T_A = 25\text{ }^\circ\text{C}$ , in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Channel separation	$\Delta V_{15-16}$	50			dB	$V_3$ or $V_1 = 600\text{ mV}_{\text{rms}}$
Channel separation	$\Delta V_{19-20}$	50			dB	$V_3$ or $V_1 = 600\text{ mV}_{\text{rms}}$
Channel separation	$\Delta V_{9-10}$	50			dB	$V_3$ or $V_1 = 600\text{ mV}_{\text{rms}}$
Cross talk attenuation switch	$\alpha_{\text{Input interf/}} /$ Output rms	60			dB	$V_{\text{rms}} = 0$ $V_{1\text{Int}1,3,6} = 600\text{ mV}_{\text{rms}}$ $V_{1\text{Int}7,8} = 2\text{ V}_{\text{rms}}$
Attenuation MUTE	$\alpha_{1-16}$	80			dB	01, 0 0- 02, 0 0 $\text{Vol}_{\text{LSI}0} - \text{Vol}_{\text{LSr}0}$ $V_1 = 600\text{ mV}_{\text{rms}}$
Attenuation MUTE	$\alpha_{1-16}$	80			dB	07,48; $V_1 = 600\text{ mV}_{\text{rms}}$ MUTE I:0
Attenuation MUTE	$\alpha_{1-16}$	80			dB	07,88; $V_1 = 600\text{ mV}_{\text{rms}}$ MUTE II:0
Attenuation MUTE	$\alpha_{3-15}$	80			dB	01, 0 0- 02, 0 0 $\text{Vol}_{\text{LSI}0} - \text{Vol}_{\text{LSr}0}$ $V_3 = 600\text{ mV}_{\text{rms}}$
Attenuation MUTE	$\alpha_{3-15}$	80			dB	07,48; $V_3 = 600\text{ mV}_{\text{rms}}$ MUTE I:0
Attenuation MUTE	$\alpha_{3-15}$	80			dB	07,88; $V_3 = 600\text{ mV}_{\text{rms}}$ MUTE II:0
Attenuation MUTE	$\alpha_{1-20}$	80			dB	03, 0 0; $V_1 = 600\text{ mV}_{\text{rms}}$ $\text{Vol}_{\text{KH}0}$
Attenuation MUTE	$\alpha_{1-20}$	80			dB	07,48; $V_1 = 600\text{ mV}_{\text{rms}}$ MUTE I:0
Attenuation MUTE	$\alpha_{3-19}$	80			dB	03, 0 0; $V_3 = 600\text{ mV}_{\text{rms}}$ $\text{Vol}_{\text{KH}0}$
Attenuation MUTE	$\alpha_{3-19}$	80			dB	07,48; $V_3 = 600\text{ mV}_{\text{rms}}$ MUTE I:0

Analogous values are valid for feed-in at the pin 6, 7, 8;  $V_{7,8} = 2\text{ V}_{\text{rms}}$ ;  $V_6 = 600\text{ mV}_{\text{rms}}$ 

Attenuation MUTE	$\alpha_{3-10}$	80			dB	07,48; $V_3 = 600\text{ mV}_{\text{rms}}$ MUTE I:0
Attenuation MUTE	$\alpha_{1-9}$	80			dB	07,48; $V_1 = 600\text{ mV}_{\text{rms}}$ MUTE I:0
Attenuation MUTE	$\alpha_{6-10}$	80			dB	07,49; $V_6 = 600\text{ mV}_{\text{rms}}$ MUTE I:0, AM
Attenuation MUTE	$\alpha_{6-9}$	80			dB	07,49; $V_6 = 600\text{ mV}_{\text{rms}}$ MUTE I:0, AM

**Characteristics (cont'd)**

$V_S = 12\text{ V}$ ;  $T_A = 25\text{ }^\circ\text{C}$ , in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Max.input voltage	$V_6$	600			$\text{mV}_{\text{rms}}$	$THD_{15,16} = 1\%$
Max.input voltage	$V_3$	600			$\text{mV}_{\text{rms}}$	$THD_{15} = 1\%$
Max.input voltage	$V_1$	600			$\text{mV}_{\text{rms}}$	$THD_{16} = 1\%$
Max.input voltage	$V_1$	300			$\text{mV}_{\text{rms}}$	$THD_{16} = 1\%$ ; 00,02 <i>Matrix: Stereo</i>
Max.input voltage	$V_7$	2			$V_{\text{rms}}$	$THD_{16} = 3\%$ ; 07, CC, SCART
Max.input voltage	$V_8$	2			%	$THD_{15} = 3\%$ ; 07, CC, SCART
Distorsion	$THD_{19}$	0	0.01	0.1	%	$V_3 = 250\text{ mV}_{\text{rms}}$
Distorsion	$THD_{20}$		0.01	0.1	%	$V_1 = 250\text{ mV}_{\text{rms}}$
Distorsion	$THD_{19}$		0.01	0.1	%	$V_3 = 250\text{ mV}_{\text{rms}}$ ; 03,15 $Vol_{KH21}$
Distorsion	$THD_{20}$		0.01	0.1	%	$V_1 = 250\text{ mV}_{\text{rms}}$ ; 03,15 $Vol_{KH21}$

Analogous values are valid for feed-in at the pin 6, 7, 8 ;  $V_{7,8} = 400\text{ mV}_{\text{rms}}$ ;  $V_6 = 250\text{ mV}_{\text{rms}}$

Distorsion	$THD_{16}$		0.01	0.1	%	$V_1 = 250\text{ mV}_{\text{rms}}$
Distorsion	$THD_{15}$		0.01	0.1	%	$V_3 = 250\text{ mV}_{\text{rms}}$
Distorsion	$THD_{16}$		0.01	0.2	%	$V_1 = 250\text{ mV}_{\text{rms}}$ ; 01, 2 F-02,2F $Vol_{LSI47}$ - $Vol_{LSr47}$
Distorsion	$THD_{15}$		0.01	0.2	%	$V_3 = 250\text{ mV}_{\text{rms}}$ ; 01, 2 F-02,2F $Vol_{LSI47}$ - $Vol_{LSr47}$
Distorsion	$THD_{16}$		0.1	0.4	%	$V_1 = 250\text{ mV}_{\text{rms}}$ ; 05,XX <i>any sound</i>
Distorsion	$THD_{15}$		0.1	0.4	%	$V_3 = 250\text{ mV}_{\text{rms}}$ ; 05,XX <i>any sound</i>

Analogous values are valid for feed-in at the pin 6, 7, 8 ;  $V_{7,8} = 400\text{ mV}_{\text{rms}}$ ;  $V_6 = 250\text{ mV}_{\text{rms}}$

**Characteristics (cont'd)**

$V_S = 12\text{ V}$ ;  $T_A = 25\text{ }^\circ\text{C}$ , in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.0	typ.0	max.0		
Distorsion	$THD_{10}$		0.01	0.1	%	$V_3 = 250\text{ mV}_{rms}$
Distorsion	$THD_9$		0.01	0.1	%	$V_1 = 250\text{ mV}_{rms}$
Distorsion	$THD_{10}$		0.01	0.1	%	$V_6 = 250\text{ mV}_{rms}$ , 07,C9,AM
Distorsion	$THD_9$		0.01	0.1	%	$V_6 = 250\text{ mV}_{rms}$ ; 07,C9, AM
Antiphase Cross talk atten.	$\Delta V_{16-15}$					$V_3 = 600\text{ mV}_{rms}$
Base width		0.5	0.55			$f_i = 2\text{ kHz}$ ; 00,11, <i>Basis width</i>
Antiphase Cross talk atten.	$\Delta V_{15-16}$					$V_1 = 600\text{ mV}_{rms}$
Base width		0.5	0.55			$f_i = 2\text{ kHz}$ ; 0011, <i>Basis width</i>
Base width phase	$\Phi_{16-15}$	150	180	210	deg	$V_1 = 600\text{ mV}_{rms}$ ; 00,11 <i>Basis width</i> , $f = 2\text{ kHz}$
Base width phase	$\Phi_{15-16}$	150	180	210	deg	$V_3 = 600\text{ mV}_{rms}$ ; 0011 <i>Basis width</i> , $f = 2\text{ kHz}$
Phase rotation quasi-stereo	$\Phi_{16-15}$	0	10	40	deg	$V_{3,1} = 600\text{ mV}_{rms}$ ; 00,21 <i>Quasi-stereo</i> , $f = 40\text{ Hz}$

## Characteristics (cont'd)

 $V_S = 12\text{ V}$ ;  $T_A = 25\text{ }^\circ\text{C}$ , in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.0	typ.	max.		
Phase rotation quasi-stereo	$\Phi_{16-15}$	130	180	230	deg	$V_{3,1} = 600\text{ mV}_{\text{rms}}$ ; 0021 <i>Quasi-stereo</i> , $f = 1\text{ kHz}$
Phase rotation quasi-stereo	$\Phi_{16-15}$	-30	10	0	deg	$V_{3,1} = 600\text{ mV}_{\text{rms}}$ ; 00,21 <i>Quasi-stereo</i> , $f = 15\text{ kHz}$
Unweighted signal-to-noise ratio	$a_{S/N 16}$	1	90	97	dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_1 = 0,6\text{ V}_{\text{rms}}$
Unweighted signal-to-noise ratio	$a_{S/N 15}$	1	90	97	dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_3 = 0,6\text{ V}_{\text{rms}}$
Unweighted signal-to-noise ratio	$a_{S/N 16}$	70	80		dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_1 = 0,6\text{ V}_{\text{rms}}$ 01,27-02,27 <i>Vol<sub>LSI39</sub>-Vol<sub>LSr39</sub></i>
Unweighted signal-to-noise ratio	$a_{S/N 15}$	70	80		dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_3 = 0,6\text{ V}_{\text{rms}}$ 01,27-02,27 <i>Vol<sub>LSI39</sub>-Vol<sub>LSr39</sub></i>
External voltage	$V_{N15}$		2	10	$\mu\text{V}_{\text{rms}}$	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ 01,00-02,00 <i>Vol<sub>LSI0</sub>-Vol<sub>LSr0</sub></i>
External voltage	$V_{N16}$		2	10	$\mu\text{V}_{\text{rms}}$	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ 01,00-02,00 <i>Vol<sub>LSI0</sub>-Vol<sub>LSr0</sub></i>
Unweighted signal-to-noise ratio	$a_{S/N 20}$	90	97		dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_1 = 0,6\text{ V}_{\text{rms}}$
Unweighted signal-to-noise ratio	$a_{S/N 19}$	1	90	97	dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_3 = 0,6\text{ V}_{\text{rms}}$
Unweighted signal-to-noise ratio	$a_{S/N 20}$	70	80		dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_1 = 0,6\text{ V}_{\text{rms}}$ 03, 10, <i>Vol<sub>KH16</sub></i>
Unweighted signal-to-noise ratio	$a_{S/N 19}$	70	80		dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_3 = 0,6\text{ V}_{\text{rms}}$ 03, 10, <i>Vol<sub>KH16</sub></i>
External voltage	$V_{N20}$		2	10	$\mu\text{V}_{\text{rms}}$	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; 03,00 <i>Vol<sub>KH0</sub></i>
External voltage	$V_{N19}$		2	10	$\mu\text{V}_{\text{rms}}$	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; 03,00 <i>Vol<sub>KH0</sub></i>
Unweighted signal-to-noise ratio	$a_{S/N 9}$	1	90	97	dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_1 = 0,6\text{ V}_{\text{rms}}$
Unweighted signal-to-noise ratio	$a_{S/N 10}$	1	90	97	dB	$V_{N\text{ rms } 20\text{ Hz-20 kHz}}$ ; $V_3 = 0,6\text{ V}_{\text{rms}}$



**Characteristics** (cont'd)

$V_S = 12\text{ V}$ ;  $T_A = 25\text{ °C}$ , in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Change of DC-switch $\Delta 1$ Bit	$\Delta V_{16}$			$\pm 10$	mV	01,X-01,X $\pm 1$ $Vol_{LSI}X - Vol_{LSI}(X \pm 1)$
Change of DC-switch $\Delta 1$ Bit	$\Delta V_{15}$			$\pm 10$	mV	02,X-02,X $\pm 1$ $Vol_{LSr}X - Vol_{LSr}(X \pm 1)$
Change of DC-switch $\Delta 1$ Bit	$\Delta V_{16}$			$\pm 10$	mV	05,X-05,X 1 <i>Sound X-Sound</i> (X $\pm 1$ )
Change of DC-switch $\Delta 1$ Bit	$\Delta V_{15}$			$\pm 10$	mV	0,X-05,X $\pm 1$ <i>Sound X-Sound</i> (X $\pm 1$ )
Change of DC-switch $\Delta 1$ Bit	$\Delta V_{19}$			$\pm 10$	mV	03,X-03,X $\pm 1$ $Vol_{KH}X - Vol_{KH}(X \pm 1)$
Change of DC-switch $\Delta 1$ Bit	$\Delta V_{20}$			$\pm 10$	mV	03,X-03,X $\pm 1$ $Vol_{KH}X - Vol_{KH}(X \pm 1)$

**Design-Related Data**

Input resistance	$R_7$	35			k $\Omega$	
Input resistance	$R_8$	35			k $\Omega$	
Input resistance	$R_6$	20			k $\Omega$	
Input resistance	$R_3$	20			k $\Omega$	
Input resistance	$R_1$	20			k $\Omega$	
Output resistance	$R_{19}$			200	$\Omega$	
Output resistance	$R_{20}$			200	$\Omega$	
Output resistance	$R_{15}$			200	$\Omega$	
Output resistance	$R_{16}$			200	$\Omega$	
Output resistance	$R_9$			200	$\Omega$	
Output resistance	$R_{10}$			200	$\Omega$	

**Characteristics (cont'd)** $V_S = 12\text{ V}; T_A = 25\text{ }^\circ\text{C}$ 

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

**ID Signal Decoder**

Gain Filter OP-amp	$V_5$	13	14	15	dB	$V_{IF} = 80\text{ mV}_{pp}$	1
Max. input voltage	$V_5$	600			mV <sub>pp</sub>	Function	2
VCO voltage PLL	$V_{27}$	tbf			V	$f_{24} = 14.6\text{ kHz};$ $V_{24} = 2.5\text{ V}_{os}$	2
VCO voltage PLL	$V_{27}$	tbf	3	tbf	V	$f_{24} = 15.625\text{ kHz};$ $V_{24} = 2.5\text{ V}_{os}$	2
VCO voltage PLL	$V_{27}$			tbf	V	$f_{24} = 16.6\text{ kHz};$ $V_{24} = 2.5\text{ V}_{os}$	2
VCO voltage PLL	$V_{27}$				V	$f_{24} = 58.4\text{ kHz};$ $V_{24} = 2.5\text{ V}_{os}$	2
VCO voltage PLL	$V_{27}$	tbf			V	00,09, H-lmp $f_{24} = 66.4\text{ kHz};$ $V_{24} = 2.5\text{ V}_{os}$	2
VCO voltage PLL	$V_{27}$			tbf	V	00,09, H-lmp	2

$$V_{KT\text{ Filter}} = \frac{\sqrt{(V_{25} - V_{25}^*)^2 + (V_{26} - V_{26}^*)^2}}{V_5}$$

$V_{25}$  or  $V_{26}$  when  $V_5 = 0$   
 $V_{25}^*$  or  $V_{26}^*$  when  $V_5 = 400\text{ mV}_{pp}$

ID filter gain		tbf		tbf		$V_{KT\text{ Filter}}$ $f_5 = 54.962\text{ kHz}$ I <sup>2</sup> C talk: Dual	2
ID filter gain		tbf		tbf		$V_{KT\text{ Filter}}$ $f_5 = 54.805\text{ kHz}$ I <sup>2</sup> C talk: Stereo	2

$$V_{25\text{ test}} = V_{25}(V_5 = 0) \pm \Delta V_{25}; V_{26\text{ test}} = V_{26}(V_5 = 0) \pm \Delta V_{26}$$

**Characteristics (cont'd)** $V_s = 12\text{ V}; T_A = 25\text{ °C}$ 

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Detection threshold	$\Delta V_{25}$	tbf			mV	I <sup>2</sup> C talk: Stereo o. Dual	3
Detection threshold	$-\Delta V_{25}$	tbf			mV	I <sup>2</sup> C talk: Stereo o. Dual	3
Detection threshold	$\Delta V_{26}$	tbf			mV	I <sup>2</sup> C talk: Stereo o. Dual	3
Detection threshold	$-\Delta V_{26}$	tbf			mV	I <sup>2</sup> C talk: Stereo o. Dual	3
Mono threshold	$\Delta V_{25}$	0		tbf	mV	I <sup>2</sup> C talk: Mono	3
Mono threshold	$-\Delta V_{25}$	0		tbf	mV	I <sup>2</sup> C talk: Mono	3
Mono threshold	$\Delta V_{26}$	0		tbf	mV	I <sup>2</sup> C talk: Mono	3
Mono threshold	$-\Delta V_{26}$	0		tbf	mV	I <sup>2</sup> C talk: Mono	3
Response of detection	$t_{det}$					I <sup>2</sup> C talk: Stereo o Dual $\pm \Delta V_{25} = 1\text{ V}$	3
Response of detection	$t_{det}$	1/4		1/2	$t_{MPX}$	I <sup>2</sup> C talk: Stereo o Dual $\pm \Delta V_{26} = 1\text{ V}$	3
Switching threshold $f_{REF}$ -input	$V_{24L}$	0		1.5	V		2
Switching threshold $f_{REF}$ -input	$V_{24H}$	3.5		$V_{21}$	V		2
Multiplexer takt	$t_{MPX}$		1.08		s	00,C0, MPX = 1 s	
Multiplexer takt	$t_{MPX}$		2.17		s	00,00, MPX = 2 s	
Multiplexer takt	$t_{MPX}$		4.34		s	00,40, MPX = 4 s	
Multiplexer takt	$t_{MPX}$		8.68		s	00,80, MPX = 8 s	

**Design-Related Data**

Filter output resistance	$R_{25,26}$	110			k $\Omega$	
$f_{REF}$ input resistance	$R_{24}$	7			k $\Omega$	

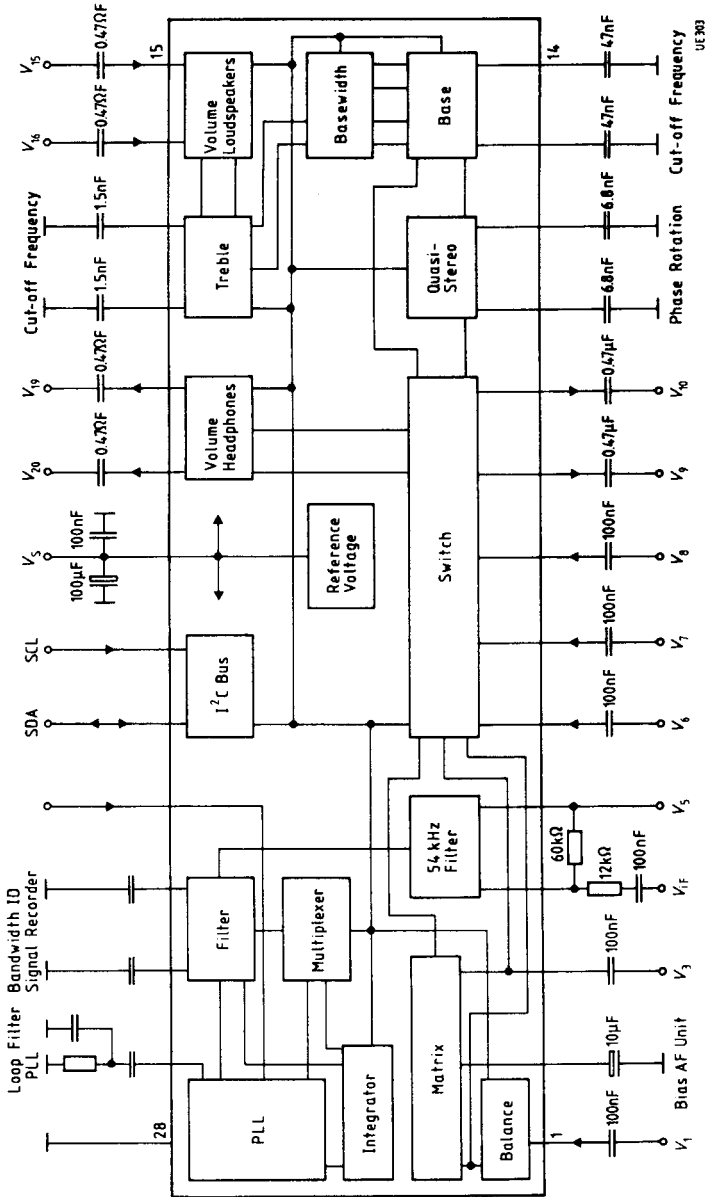
**Characteristics (cont'd)** $V_S = 12\text{ V}; T_A = 25\text{ }^\circ\text{C}$ 

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	

**I<sup>2</sup>C-B Bus (SCL, SDA)**

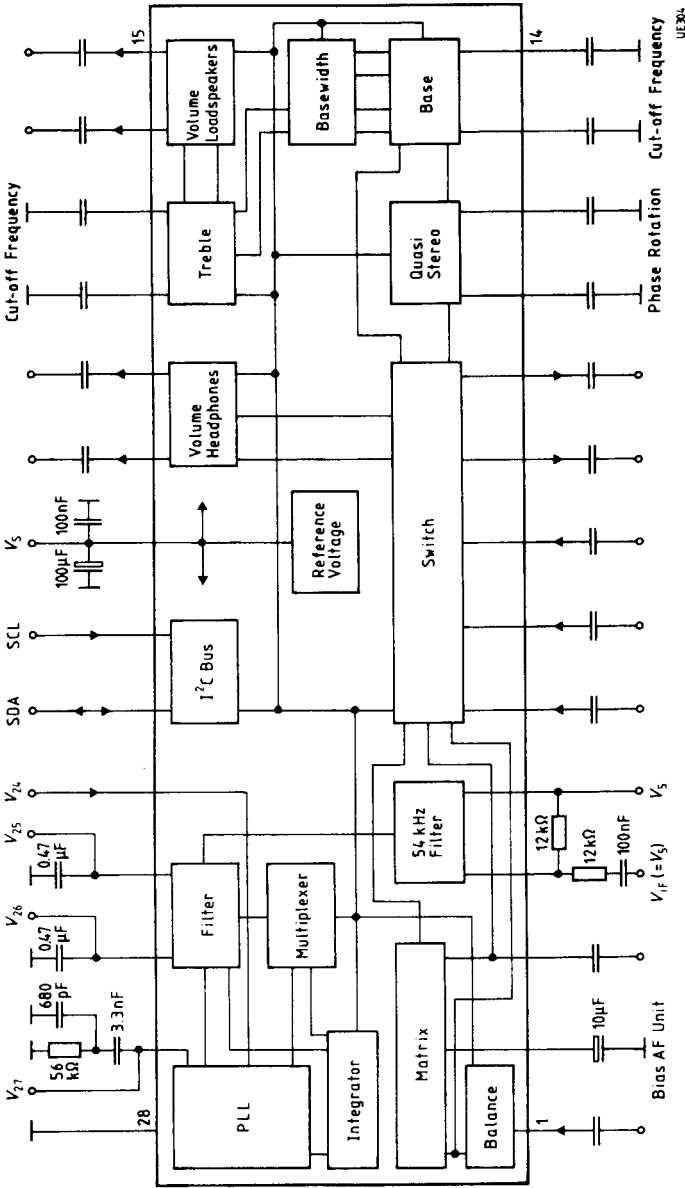
SCL, SDA edges					
Rise time	$t_R$			1	$\mu\text{s}$
Fall time	$t_F$			300	$\text{ns}$
Shift register clock pulse SCL					
Frequency	$f_{\text{SCL}}$	0		100	$\text{kHz}$
H-pulse width	$t_{\text{HIGH}}$	4			$\mu\text{s}$
L-pulse width	$t_{\text{LOW}}$	4			$\mu\text{s}$
Start					
Set-up time	$t_{\text{SUSTA}}$	4			$\mu\text{s}$
Hold time	$t_{\text{HDSTA}}$	4			$\mu\text{s}$
Stop					
Set-up time	$t_{\text{SUSTO}}$	4			$\mu\text{s}$
Bus free time	$t_{\text{BUF}}$	4			$\mu\text{s}$
Data transfer					
Set-up time	$t_{\text{SUDAT}}$	1			$\mu\text{s}$
Hold time	$t_{\text{HDDAT}}$	1			$\mu\text{s}$
Input SCL, SDA					
Input voltage	$V_{\text{QH}}$ $V_{\text{QL}}$	2.4		5.5 1	$\text{V}$ $\text{V}$
Input current	$I_{\text{QH}}$ $I_{\text{QL}}$			50 100	$\mu\text{A}$ $\mu\text{A}$
Output SDA (open collector)					
Output voltage	$V_{\text{QH}}$ $V_{\text{QL}}$	5.4		0.4	$\text{V}$ $\text{V}$
$R_L = 2.5\text{ k}\Omega$					
$I_{\text{OL}} = 3\text{ mA}$					

Test Circuit 1

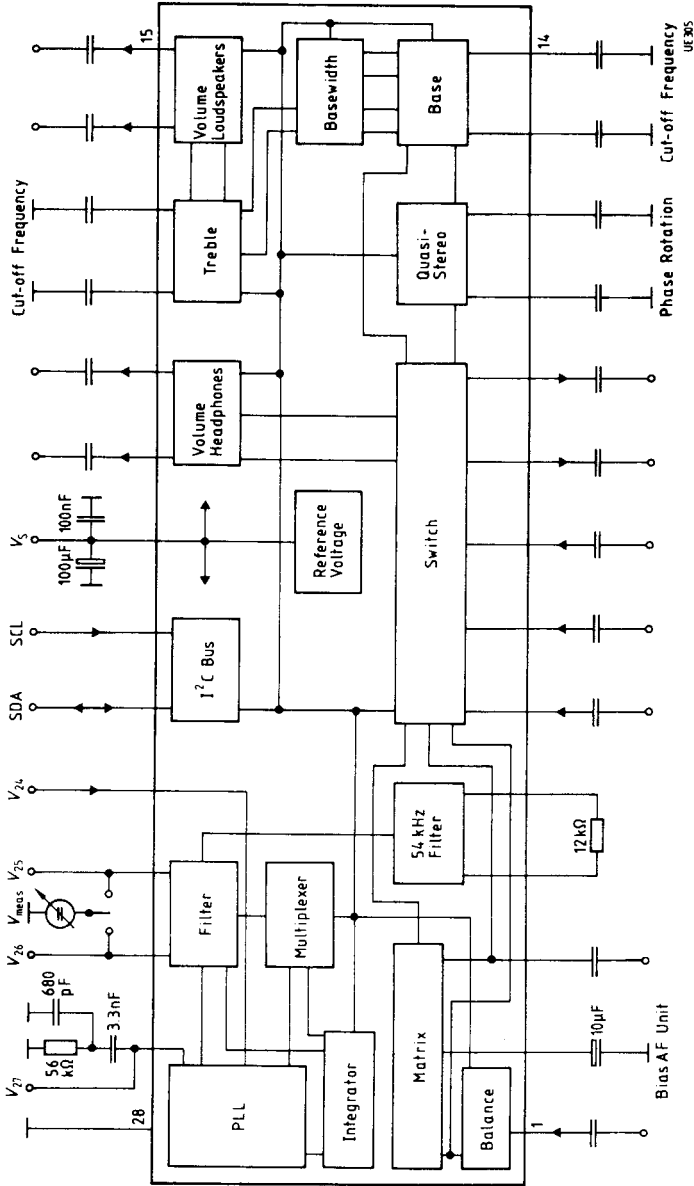


AF Generator resistance for V<sub>1</sub>, V<sub>3</sub>, V<sub>6</sub>, V<sub>7</sub>, V<sub>8</sub>, V<sub>9</sub>, V<sub>10</sub> = 50Ω  
 Terminating impedance at the AF inputs for noise and cross-talk measurement = 1kΩ

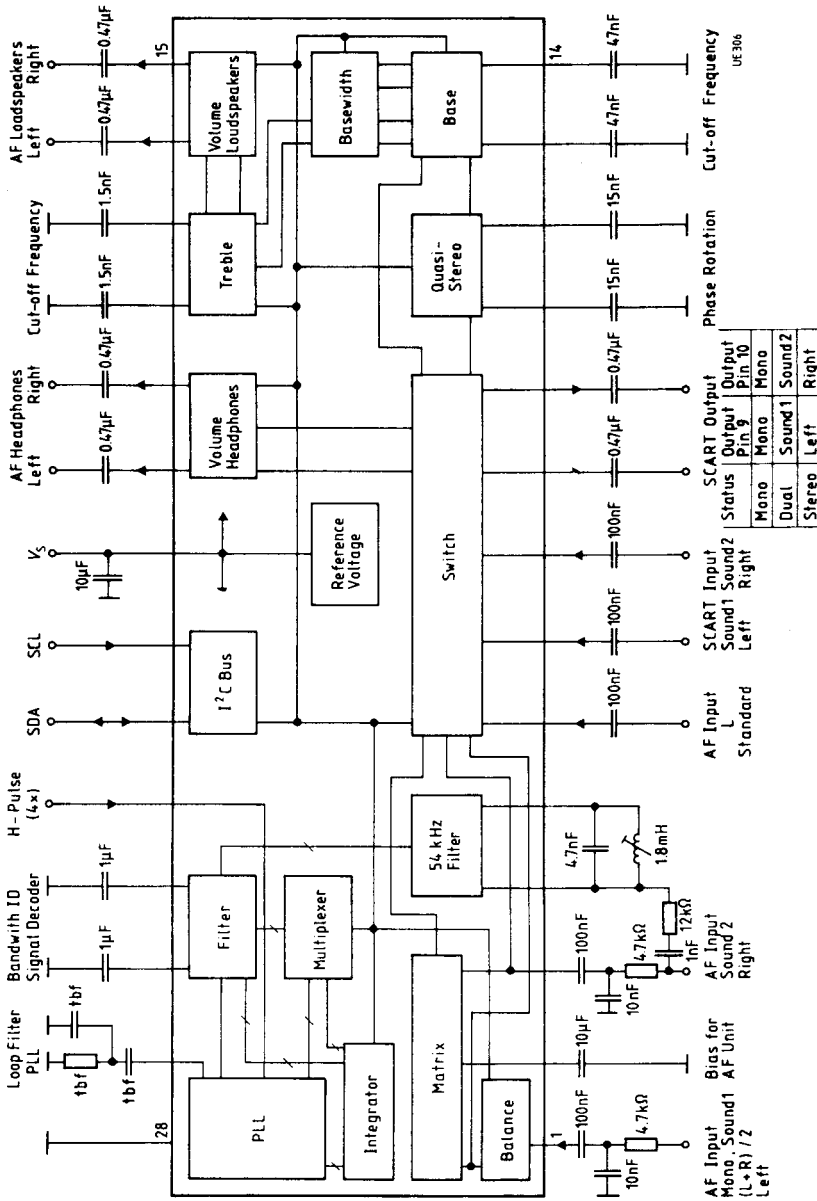
Test Circuit 2



Test Circuit 3

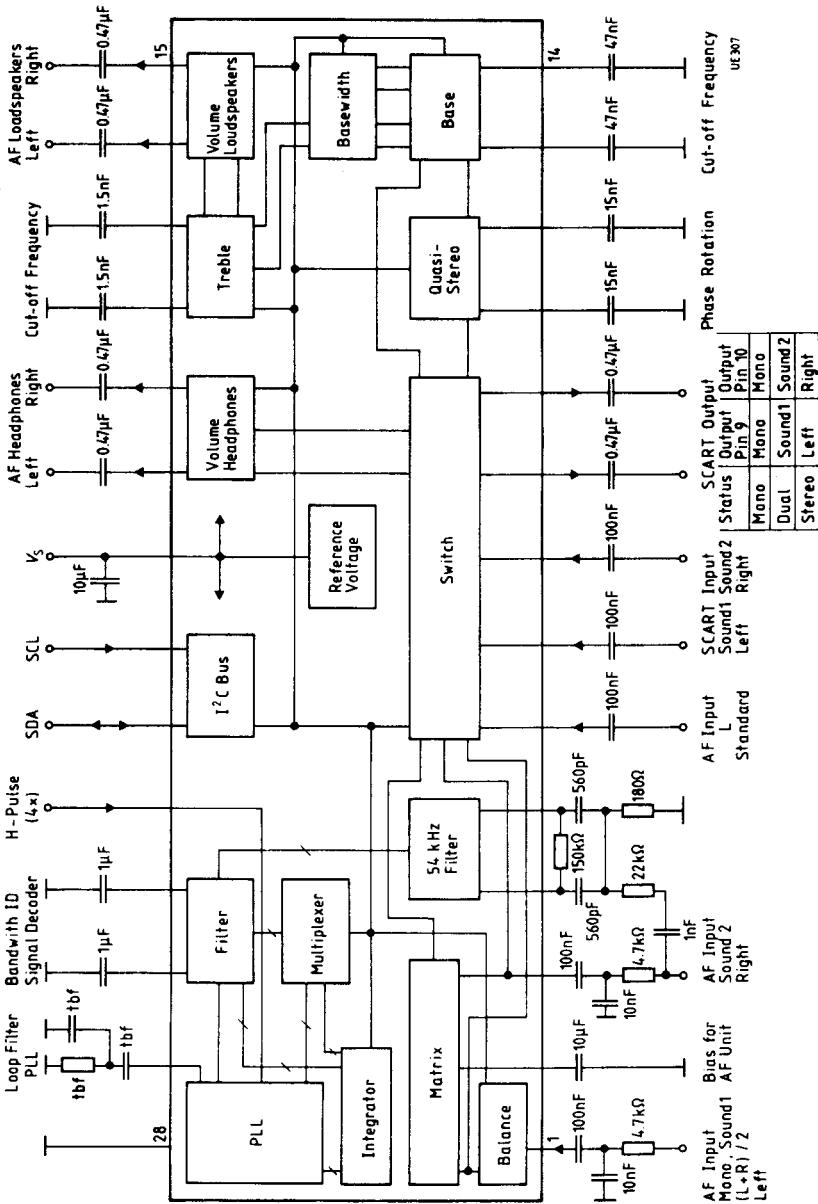


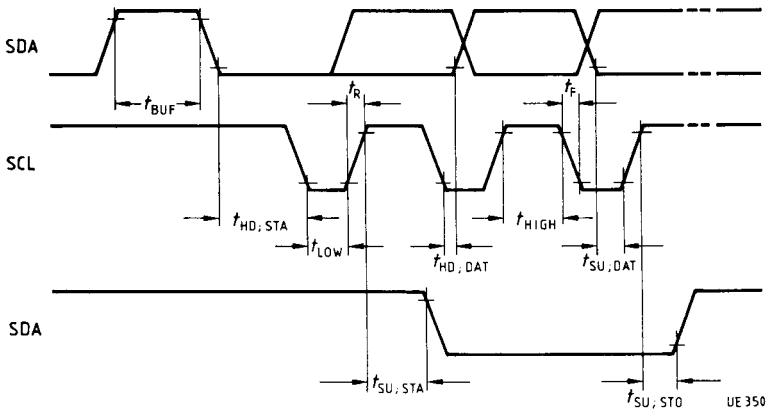
Application Circuit 1





Application Circuit 2



I<sup>2</sup>C Bus Timing Diagram

$t_{\text{SUSTA}}$	Set-up time (start)
$t_{\text{HDSTA}}$	Hold time (start)
$t_{\text{HIGH}}$	HIGH pulse width (clock)
$t_{\text{LOW}}$	LOW pulse width (clock)
$t_{\text{SUDAT}}$	Set-up time (data transfer)
$t_{\text{HDDAT}}$	Hold time (data transfer)
$t_{\text{SUSTO}}$	Set-up time (stop)
$t_{\text{BUF}}$	Bus free time
$t_{\text{F}}$	Fall time
$t_{\text{R}}$	Rise time

All times are referenced to the  $V_{\text{IH}}$  and  $V_{\text{IL}}$  values