

# LINEAR INTEGRATED CIRCUITS

## PREAMPLIFIER WITH ALC FOR CASSETTE RECORDERS

- EXCELLENT VERSATILITY in USE ( $V_s$  from 4 to 20V)
- HIGH OPEN LOOP GAIN
- LOW DISTORTION
- LOW NOISE
- LARGE AUTOMATIC LEVEL CONTROL RANGE
- GOOD SUPPLY RIPPLE REJECTION
- STEREO MATCHING BETTER THAN 3 dB

The TDA 1054M is a monolithic integrated circuit in a 16-lead dual in-line plastic package. The functions incorporated are:

- Low noise preamplifier
- Automatic level control system (ALC)
- High gain equalization amplifier
- Supply voltage rejection facility (SVRF).

It is intended as preamplifier in cassette tape recorders and players, dictaphones, compressor and expander in industrial equipments, Hi-Fi preamplifiers and in wire diffusion receivers; for stereo applications the ALC matching is better than 3 dB.

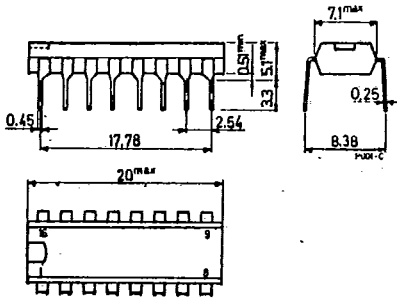
## ABSOLUTE MAXIMUM RATINGS

$V_s$	Supply voltage	20	V
$P_{tot}$	Total power dissipation at $T_{amb} \leq 50^\circ\text{C}$	500	mW
$T_{stg}, T_j$	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

ORDERING NUMBERS: TDA 1054M mono applications  
 2 TDA 1054M stereo applications

## MECHANICAL DATA

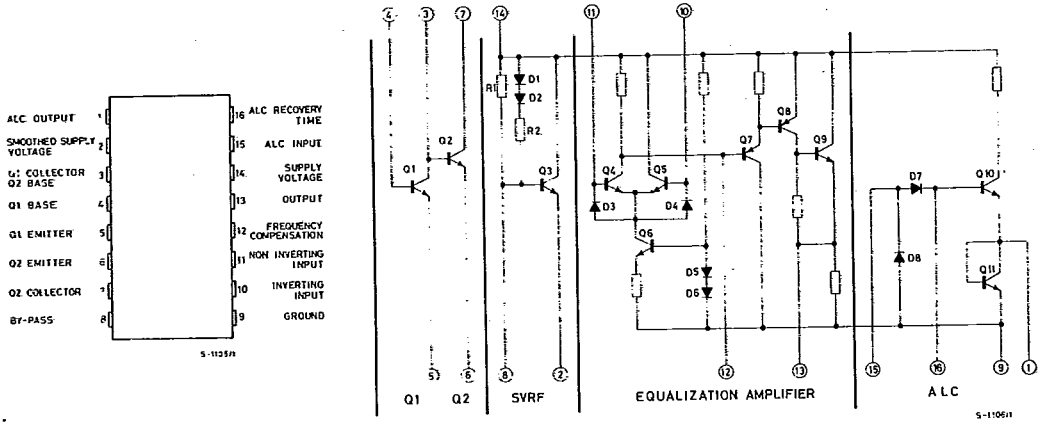
Dimensions in mm



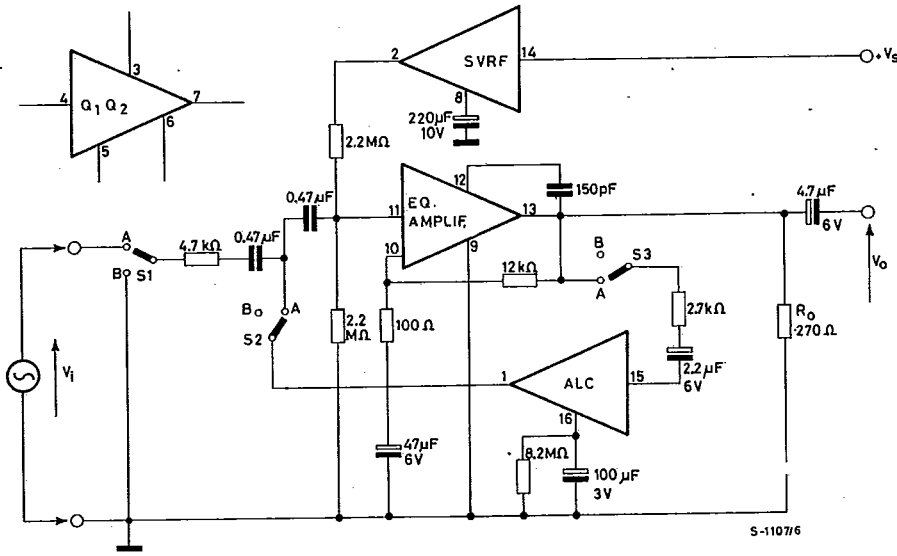
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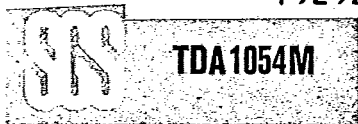


CONNECTION AND SCHEMATIC DIAGRAMS  
(top view)



TEST CIRCUIT





**THERMAL DATA**

$R_{thj-amb}$	Thermal resistance junction-ambient	max	200	°C/W
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**ELECTRICAL CHARACTERISTICS**

(Refer to the test circuit,  $T_{amb} = 25^{\circ}C$ )

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_s$	Supply voltage	4		20	V
$I_d$	Quiescent drain current $V_s = 9V$ $R_L = \infty$ $S1 = S2 = S3 = B$		6		mA
$h_{FE}$	DC current gain $I_C = 0.1 mA$ $V_{CE} = 5V$	300	500		-
$e_N$	Input noise voltage (Q1) $I_C = 0.1 mA$ $V_{CE} = 5V$ $f = 1 kHz$		2		$\frac{nV}{\sqrt{Hz}}$
$i_N$	Input noise current (Q1)		0.5		$\frac{pA}{\sqrt{Hz}}$
NF	Noise figure (Q1) $I_C = 0.1 mA$ $V_{CE} = 5V$ $R_g = 4.7 k\Omega$ $B (-3 dB) = 20$ to $10,000 Hz$		0.5	4	dB
$G_V$	Open loop voltage gain (for equalization amplifier) $V_s = 9V$ $f = 1 kHz$		60		dB
$V_o$	Output voltage with A.L.C. $V_s = 9V$ $V_i = 100mV$ $f = 1 kHz$ $S1 = S2 = S3 = A$		1.1		V
R1	(for SVRF system)	see schematic diagram		7.5	k $\Omega$
R2	(for SVRF system)	see schematic diagram		120	$\Omega$
$e_N$	Input noise voltage (for equalization amplifier pin 11) $V_s = 9V$ $R_g = 4.7 k\Omega$ $G_V = 40 dB$ $S1 = B$ $B (-3 dB) = 22 Hz$ to $22 KHz$		1.3		$\mu V$
$V_{DR}$	Drop-out (between pins 14 and 2) $V_s = 9V$ $I_d = 6 mA$		0.8		V

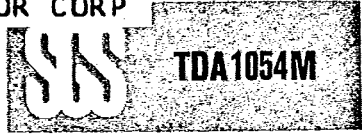


Fig. 1 - Equivalent input spot voltage and noise current vs. bias current (input transistor  $Q_1$ )

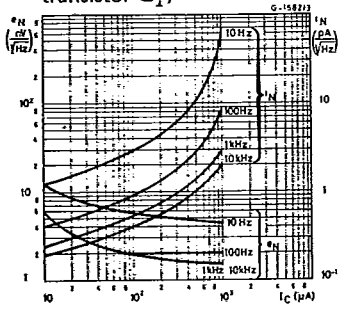


Fig. 2 - Equivalent input noise current vs. frequency (input transistor  $Q_1$ )

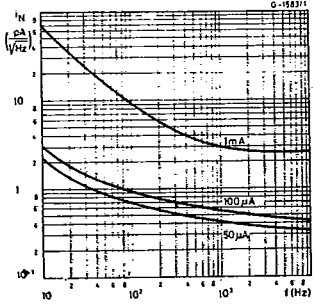


Fig. 3 - Equivalent input noise voltage vs. frequency (input transistor  $Q_1$ )

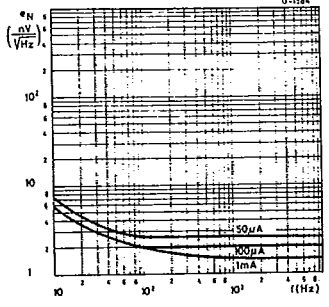


Fig. 4 - Noise figure vs. bias current (input transistor  $Q_1$ )

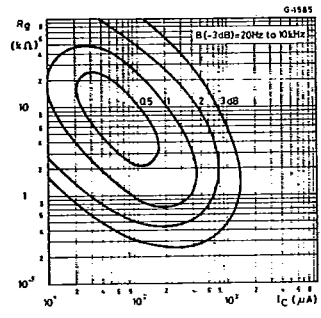


Fig. 5 - Optimum source resistance and minimum NF vs. bias current (input transistor  $Q_1$ )

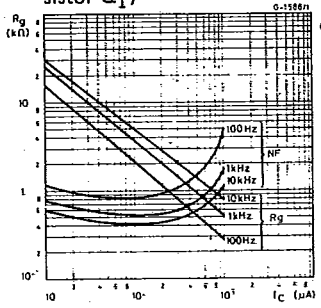


Fig. 6 - Current gain vs. collector current (input transistor  $Q_1$ )

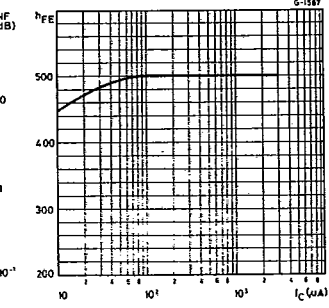


Fig. 7 - Open loop gain vs. frequency (equalization amplifier)

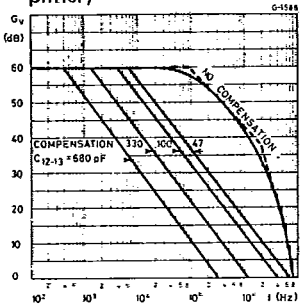
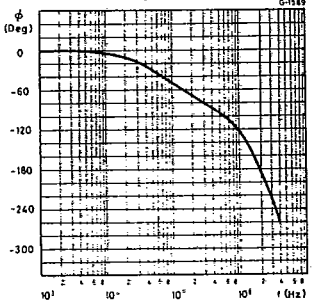
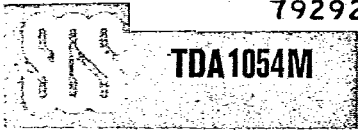


Fig. 8 - Open loop phase response vs. frequency (equalization amplifier)





APPLICATION INFORMATION

Fig. 9 - Application circuit for battery/mains cassette player and recorder

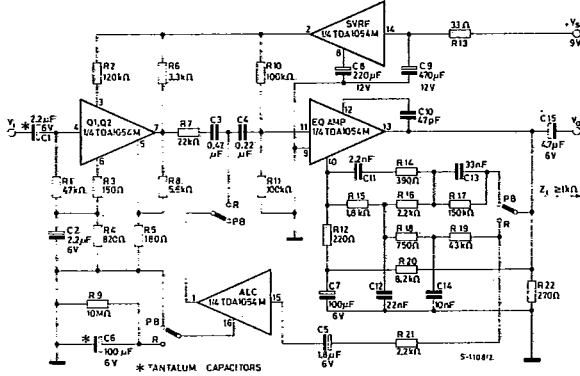
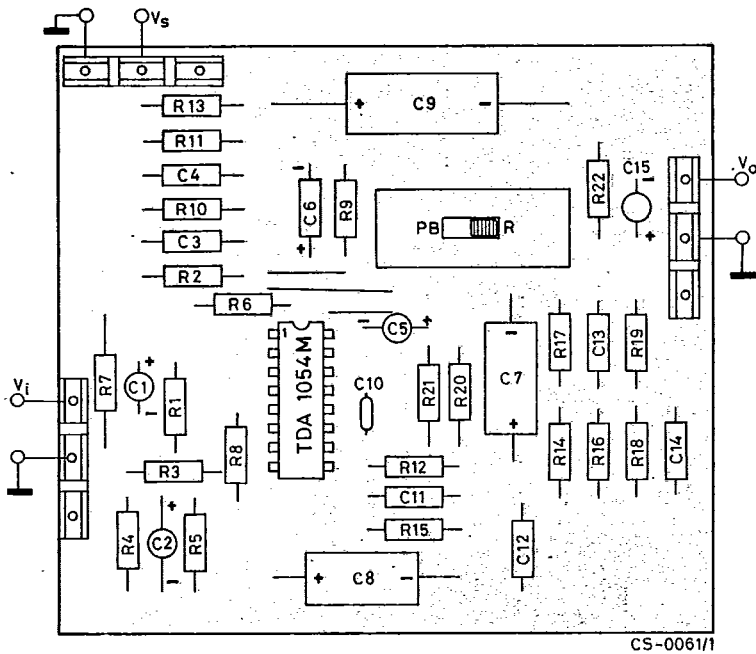


Fig. 10 - P.C. board and component layout for the circuit fig. 9 (1:1 scale)





## Typical performance of circuit in fig. 9

(T<sub>amb</sub> = 25°C, V<sub>s</sub> = 9V)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>PLAYBACK</b>					
G <sub>v</sub>	Voltage gain (open loop)	f = 20 to 20,000 Hz	110		dB
G <sub>v</sub>	Voltage gain (closed loop)	f = 1 kHz	57		dB
Z <sub>i</sub>	Input impedance	f = 100 Hz f = 1 kHz f = 10 kHz	10 41 43		kΩ kΩ kΩ
Z <sub>o</sub>	Output impedance	f = 1 kHz	12	35	Ω
B	Frequency response		see fig. 12		
d	Distortion	V <sub>o</sub> = 1V f = 1 kHz	0.1		%
	Output background noise	Z <sub>g</sub> = 300 Ω + 120 mH (DIN 45405)	1.3		mV
***	Output weighted background noise		1.3		mV
$\frac{S+N}{N}$	Signal to noise ratio	V <sub>o</sub> = 1.3V Z <sub>g</sub> = 300 Ω + 120 mH	60		dB
SVR	Supply voltage ripple rejection at the output	f <sub>ripple</sub> = 100 Hz	30		dB
t <sub>on</sub> **	Switch-on time	V <sub>o</sub> = 1V	500		ms
<b>RECORDING</b>					
G <sub>v</sub>	Voltage gain (open loop)	f = 20 to 20,000 Hz	110		dB
G <sub>v</sub>	Voltage gain (closed loop)	f = 1 kHz	70		dB
B	Frequency response		see fig. 14		
d*	Distortion without ALC	V <sub>o</sub> = 1.1V f = 1 kHz	0.3		%
d	Distortion with ALC	V <sub>o</sub> = 1.1V f = 10 kHz	0.4		%
ALC	Automatic level control range (for 3 dB of output voltage variation)	V <sub>i</sub> ≤ 40 mV f = 10 kHz	54		dB
V <sub>o</sub>	Output voltage before clipping without ALC	f = 1 kHz	2.3		V
V <sub>o</sub>	Output voltage with ALC	V <sub>i</sub> = 30 mV f = 10 kHz	1.1		V



Typical performance of circuit in fig. 9 (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_l^{**}$	Limiting time (see fig. 11)		75		ms
$t_{set}^{**}$	Level setting time (see fig. 11)		300		ms
$t_{rec}^{**}$	Recovery time (see fig. 11)		150		s
$t_{on}^{**}$	Switch-on time		500		ms
$\frac{S+N}{N}^{****}$	Signal to noise ratio with ALC	$V_o = 1.1V$	$R_g = 470 \Omega$	64	dB

\* Measured with selective voltmeter  
 \*\* This value depends on external network  
 \*\*\* When the DIN 45511 norm for frequency response is not mandatory the equalization peak at 10 kHz can be avoided — so halving the output noise  
 \*\*\*\* Weighted noise measurement (DIN 45405)

Fig. 11 - Limiting, level setting, recovery time

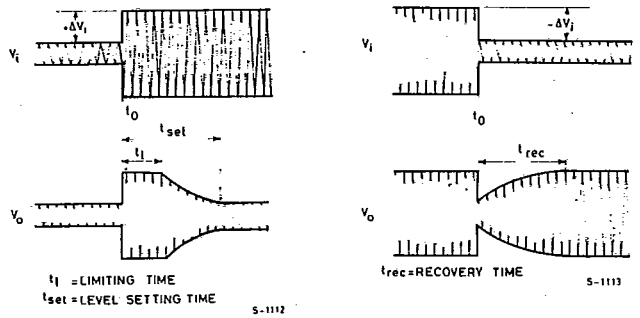


Fig. 12 - Relative frequency response for the circuit in fig. 9 (playback)

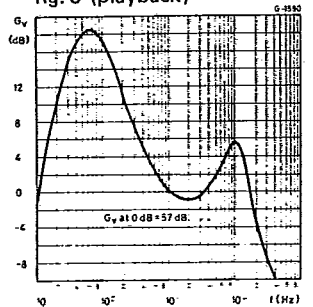


Fig. 13 - Distortion vs. frequency for the circuit in fig. 9 (playback)

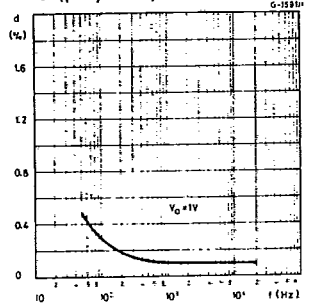


Fig. 14 - Relative frequency response for the circuit in fig. 9 (recording)

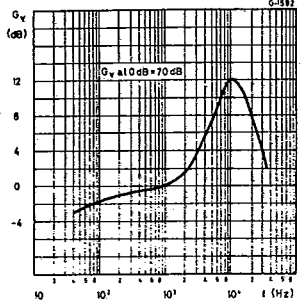




Fig. 15 - Output voltage variation and distortion with ALC vs. input voltage for the circuit in fig. 9 (recording)

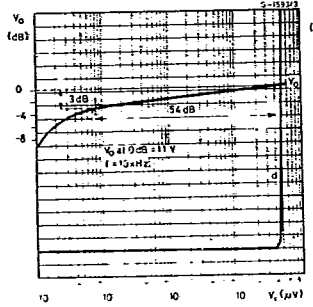


Fig. 16 - Distortion vs. frequency with ALC for the circuit in fig. 9 (recording)

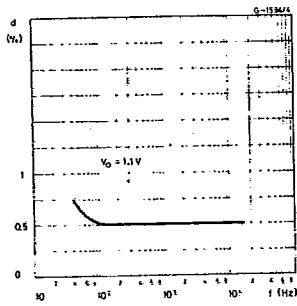


Fig. 17 - Limiting and level setting time vs. input signal variation

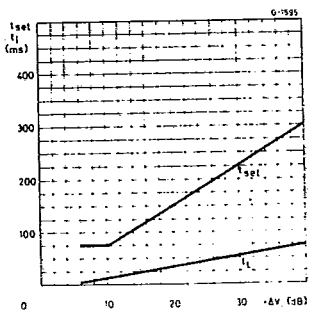
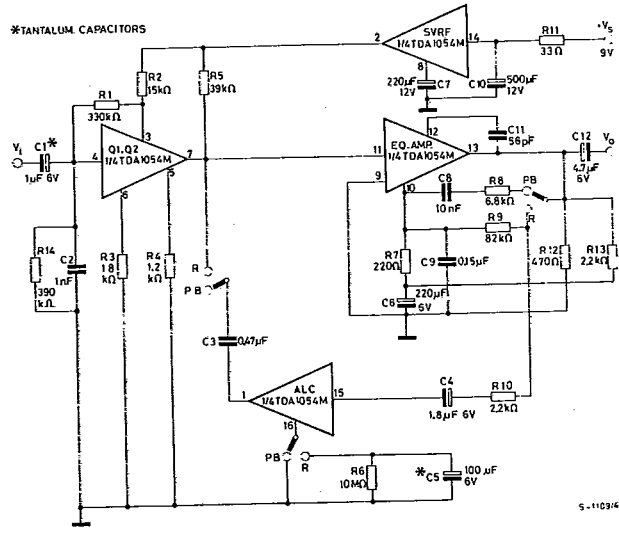


Fig. 18 - Low cost application circuit





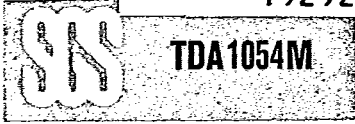
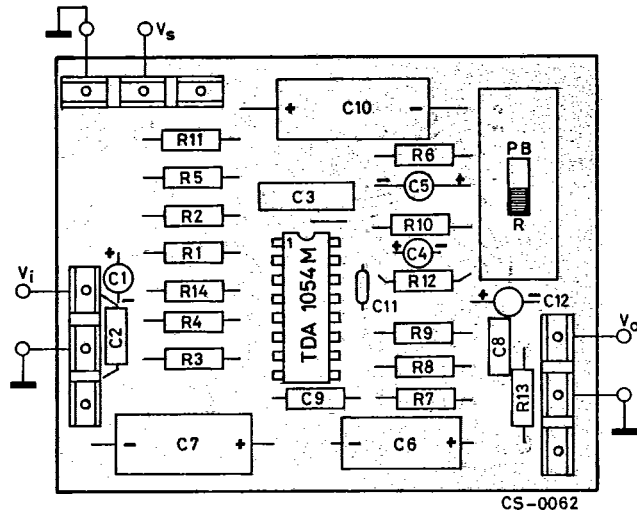


Fig. 19 - P.C. board and component layout for the circuit in fig. 18 (1:1 scale)



Typical performance of circuit in fig. 18  
 ( $T_{amb} = 25^{\circ}C$ ,  $V_s = 9V$ )

Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>PLAYBACK</b>					
$V_s$	Supply voltage	5		12	V
$I_d$	Quiescent drain current		18		mA
$G_v$	Voltage gain (closed loop)	$f = 1 \text{ kHz}$	54		dB
B	Frequency response	$f = 100 \text{ Hz}$	12		dB
		$f = 1 \text{ kHz}$	0		dB
		$f = 6 \text{ kHz}$	5		dB
		$f = 10 \text{ kHz}$	11		dB
		$f = 60 \text{ kHz}$	10		dB
d	Distortion	$V_o = 1V$ $f = 1 \text{ kHz}$	0.6		%
$e_N$	Output weighted background noise	$Z_g = 300 \Omega + 120 \text{ mH}$ (DIN 45405)	1.3		mV



Typical performance of circuit in fig. 18 (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>RECORDING</b>					
$G_v$	Voltage gain (closed loop)		70		dB
B	Frequency response	$f = 140 \text{ Hz}$	-3		dB
		$f = 1 \text{ kHz}$	0		dB
		$f = 10 \text{ kHz}$	4		dB
d	Distortion	$V_o = 1.1\text{V}$ $f = 10 \text{ kHz}$	0.7		%
ALC	Range for 3 dB of output voltage variation	$V_i \leq 40 \text{ mV}$ $f = 10 \text{ kHz}$	54		dB

Fig. 20 - Complete cassette player and recorder

