93LC46

1024-BITS SERIAL ELECTRICALLY ERASABLE PROM

■ Features

- State-of-the-art architecture
  - Non-volatile data storage
  - Operating voltage Vcc: 2.7~ 5.5V
  - Full TTL compatible inputs and outputs
  - Auto increment read for efficient data dump
- Hardware and software write protection
  - Defaults to write-disabled state at power up
  - Software instructions for write-enable/disable
  - Vcc level verification before self-timed programming cycle.
- Advanced low voltage CMOS EEPROM technology
- Versatile, easy-to-use interface
  - Self-timed programming cycle
  - Automatic erase-before-write
  - Programming status Indicator
  - Word and chip erasable
  - Stop SK anytime for power savings
- Durability and reliability
  - 40 year data retention
  - Minimum of 1M write cycles
  - Unlimited read cycles
  - ESD protection

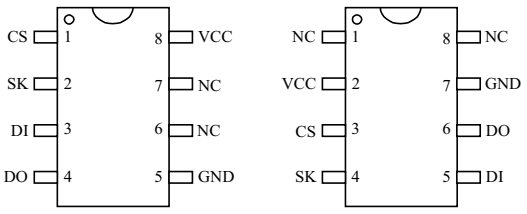
■ General Description

The 93LC46 is a 1024-bit, non-volatile, serial EEPROM. It is manufactured by using CERAMATE's advanced CMOS EEPROM technology. The 93LC46 provides efficient non-volatile read/write memory arranged as 64 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which includes read, write and write enable/disable functions. The data out pin (DO) indicates the status of the device during the self-timed non-volatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. Only when the chip is in the WRITE ENABLE state and proper Vcc operation range is the WRITE instruction accepted and thus to protect against inadvertent writes. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/BUSY status of the chip.

The 93LC46 is available in space-saving 8-lead PDIP, 8-lead SOP and rotated 8-lead SOP package.

■ Connection Diagram



PDIP-8L / SOP-8L　　Rotated SOP-8L

■ Pin Assignment

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
NC	No Connection

■ Ordering Information

93 L C 46 X XXX X

Operating Voltage	Type	Temp. grade	Package	Packing
LC : 2.7~5.5V, CMOS	46:1K	Blank: 0°C ~ +70°C	S8: SOP-8L GS8: SOP-8L, G type N8: PDIP-8L	Blank : Tube A : Taping

* All specs and applications shown above subject to change without prior notice.

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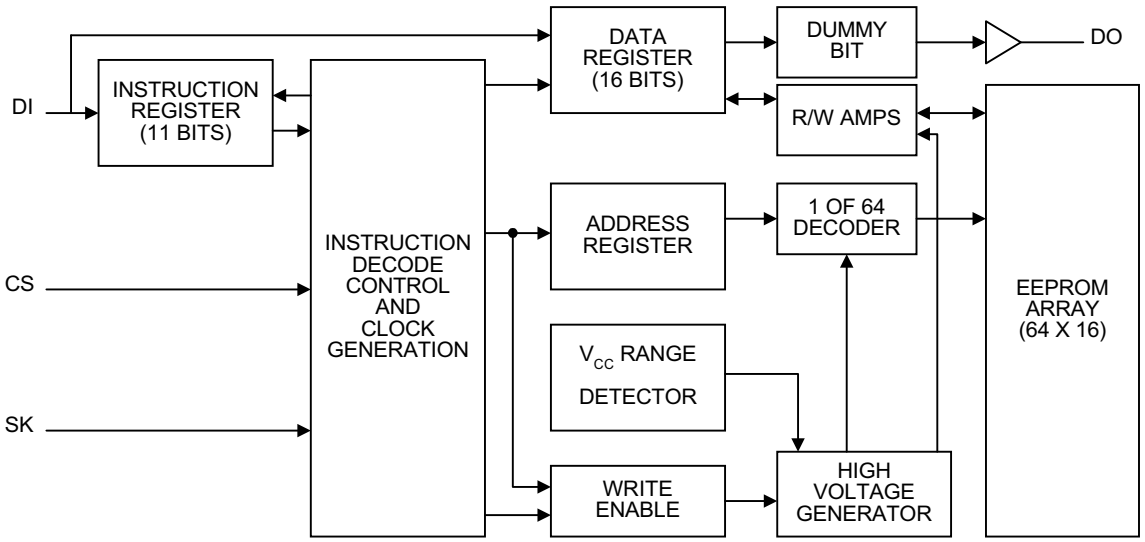
■ Block Diagram



■ Absolute Maximum Ratings

Storage Temperature.....-65°C to + 125°C
Voltage with Respect to Ground.....-0.3 to + 6.5 V
NOTE: These are STRESS rating only. Appropriate conditions for operating these devices given elsewhere may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

■ Operating Conditions

Temperature under bias: AM93LC46.....……0°C to + 70°C

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■ DC Electrical Characteristics (Vcc =2.7~5.5V, Ta = 25°C , unless otherwise noted)

Symbol	Parameter	Conditions	93LC46		Units
			Min	Max	
I_{CC1}	Operating Current (Program)	SCL = 100KHz CMOS Input Levels	—	3	mA
I_{CC2}	Operating Current (Read)	SCL = 100KHz CMOS Input Levels	—	200	µA
I_{SB1}	Standby Current	SCL=SDA=0V, Vcc=5V	—	10	µA
I_{SB2}	Standby Current	SCL=SDA=0V, Vcc=3V	—	1	
I_{IL}	Input Leakage	VIN = 0 V to VCC	-1	+1	µA
I_{OL}	Output Leakage	VOUT = 0 V to Vcc	-1	+1	µA
V_{IL}	Input Low Voltage**		-0.1	Vcc x 0.3	V
V_{IH}	Input High Voltage**		Vcc x 0.7	V_{CC}+ 0.2	V
V_{OL1}	Output Low Voltage	IOL = 2.1mA TTL	—	0.4	V
V_{OL2}	Output Low Voltage	IOL = 10uA CMOS	—	0.2	V
V_{LK}	VCC Lockout Voltage	Programming Command Can Be Executed	Default	—	V

Note. ** V_{IL} min and V_{IH} max are reference only and are not tested

■ AC Electrical Characteristics (Vcc = 2.7V ~ 5.5V, Ta = 25°C , unless otherwise noted)

Symbol	Parameter	Conditions	93LC46		Units
			Min	Max	
F_{SK}	SK Clock Frequency		0	1	MHz
T_{SKH}	SK High Time		250		ns
T_{SKL}	SK Low Time		250		ns
T_{CS}	Minimum CS Low Time		250		ns
T_{CSS}	CS Setup Time	Relative to SK	50		ns
T_{DIS}	DI Setup Time	Relative to SK	100		ns
T_{cSH}	CS Hold Time	Relative to SK	0		ns
T_{DIH}	DI Hold Time	Relative to SK	100		ns
T_{pD1}	Output Delay to "1"	AC Test		500	ns
T_{pD0}	Output Delay to "0"	AC Test		500	ns
T_{SV}	CS to Status Valid	AC Test CL = 100pF		500	ns
T_{dF}	CS to DO in 3-state	CS = VIL		100	ns
T_{wP}	Write Cycle Time			10	ms
Endurance**	5V, 25ºC, Page Mode		1M		Write cycles

Note. ** The parameter is characterized and isn't 100% tested.

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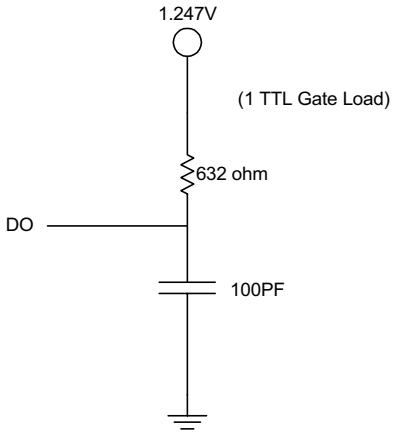

FIGURE 1. AC TEST CONDITIONS

■ Instruction Set

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A5 - A0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A5 - A0)	D15-D0*
WRALL (Write All Registers)	1	00	01XXXX	D15-D0*
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A5 - A0)	
ERAL (Erase All Registers)	1	00	10XXXX	

* If input data is not 16 bits exactly, the last 16 bits will be taken as input data (a word)

■ Pin Capacitance ** (Ta=25°C , f=1MHz)

Symbol	Parameter	Max	Units
C_{OUT}	Output capacitance	5	pF
C_{IN}	Input capacitance	5	pF

Note. ** The parameter is characterized and isn't 100% tested.

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■ Functional Descriptions

Applications
The 93LC46 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Typical applications include robotics, alarm devices, electronic locks, meters and instrumentation settings such as LAN cards, monitors and MODEM.

Endurance and Data Retention
The 93LC46 is designed for applications requiring up to 1000K programming cycles (WRITE, WRALL, EARSE and ERALL). It provides 40 years of secure data retention without power after the execution of 1000K programming cycles.

Device Operation
The 93LC46 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the 93LC46 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)
The READ instruction is the only instruction that outputs serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the rising edge transitions of SK. (Shown in Figure 3)

Auto Increment Read Operations
Sequential read is possible, since the 93LC46 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations (the address "000000" is assumed as the higher address of "111111") is output. The address will wrap around continuously with CS high until the chip select (CS) control pin is brought low. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)
Before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done, the WRITE ENABLE (WEN) instruction must be executed first. When Vcc is applied, this device powers up in the WRITE DISABLE state. The device then remains in a WRITE DISABLE state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until Vcc is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (Shown in Figure 4.)

Write Disable (WDS)
The WRITE DISABLE (WDS) instruction disables all programming capabilities. This protects the entire part against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the WRITE DISABLE state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (Shown in Figure 5.)

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■ Functional Description (Continued)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been applied to DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns (5V operation) from the falling edge of CS (tcs), DO will indicate the READY/BUSY status of the chip if CS is brought HIGH. This means that logical "0" implies the programming is still in progress while logical "1" indicates the selected register has been written, and the part is ready for another instruction. (See Figure 6.)

Note: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/BUSY flag. Therefore, it is important if you want to access the READY/BUSY flag, not to reset it through this combination of control signals.

Before a WRITE instruction can be executed, the device must be in the WRITE ENABLE (WEN) state.

Write All (WRALL)
The Write All (WRALL) instruction programs all registers with the data pattern specified in the instruction. While the WRALL instruction is being loaded, the address field becomes a sequence of DON'T-CARE bits. (Shown in Figure 7.)

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tcs), the DO pin indicates the READY/BUSY status of the chip. (Shown in Figure 7.)

Erase (ERASE)
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after minimum of t_{CS}, will cause DO to indicate the READ/BUSY status of the chip. To explain this, a logical "0" indicates the programming is still in progress while a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (Shown in Figure 8.)

Erase All (ERALL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1". (Shown in Figure 9.)

Security Consideration
To protect the entire part against accidental modification of data, each programming instruction (WRITE, WRALL, ERASE, and ERALL) must satisfy two conditions before user initiate self-timed programming cycle (the falling edge of CS). One is that the AM93LC46 is at WEN status. The other is that Vcc value must exceed a lock-out value which can be adjusted by CERAMATE TECHNICAL CO., LTD.

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■ Timing Diagram (1)

Organization Key

I/O	93LC46 (1K)		93LC56 (2K)	
	× 8	× 16	× 8	× 16
A_N	A_6	A_5	A_8 (1)	A_7 (2)
D_N	D_7	D_{15}	D_7	D_{15}

Note: (1). A_8 is a DON'T CARE value, but the extra clock is required.
(2). A_7 is a DON'T CARE value, but the extra clock is required.

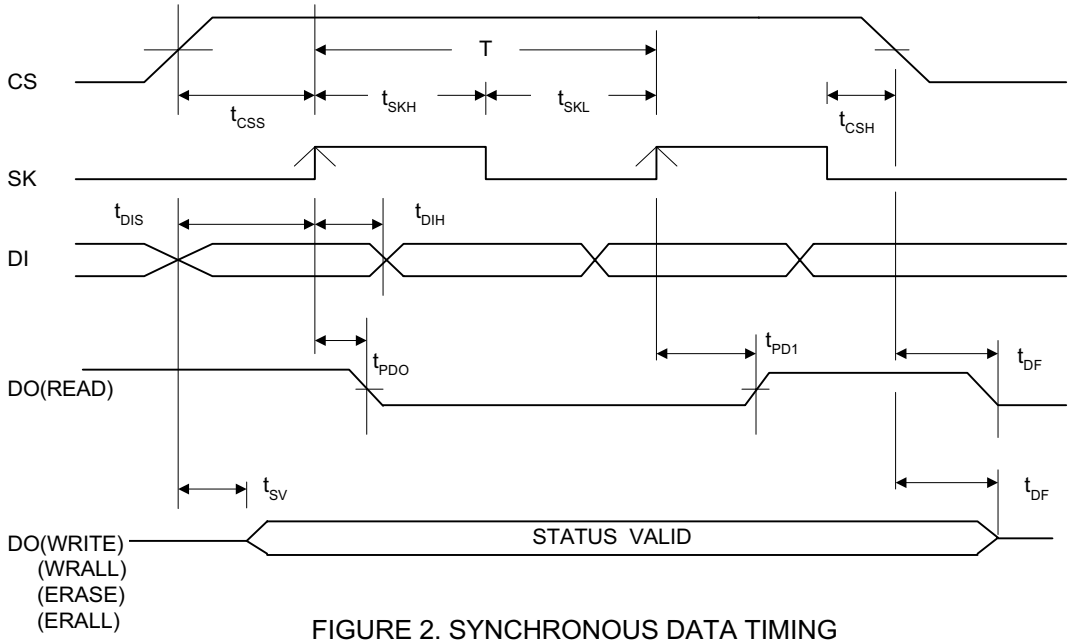
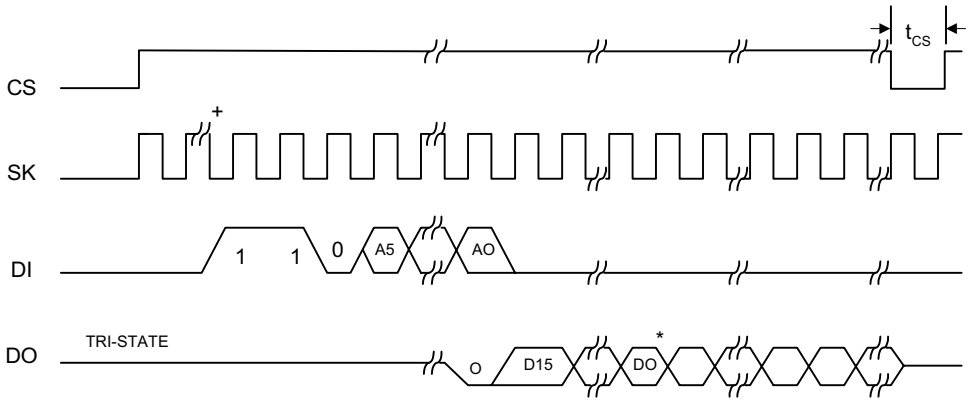


FIGURE 2. SYNCHRONOUS DATA TIMING



+For all instructions, SK cycles before start bit don't care.
*Address Pointer Cycle to the Next Register.

FIGURE 3. DATA READ CYCLE TIMING

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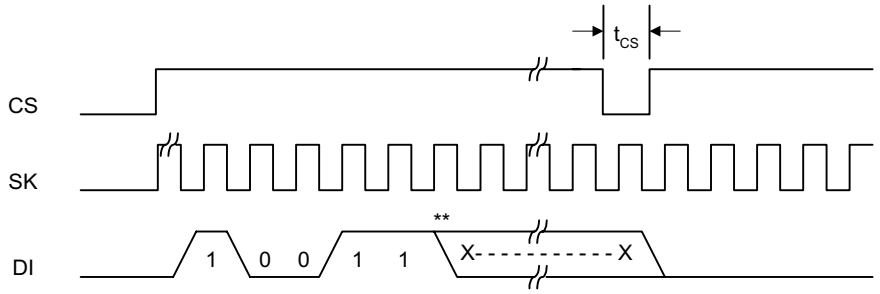
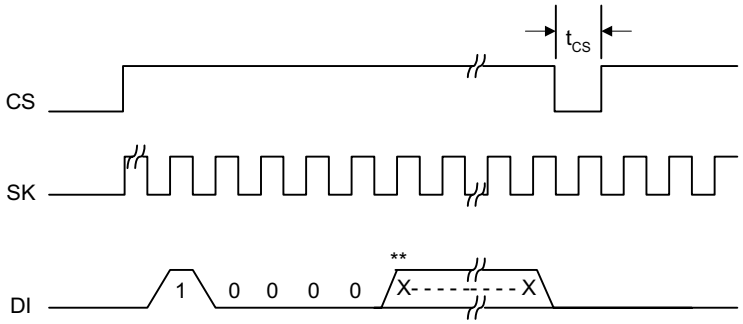
■ Timing Diagram (2)



DO = TRI-STATE
**A3~A0 don't care.

FIGURE 4. WRITE ENABLE(WEN) CYCLE TIMING



DO = TRI-STATE
**A3~A0 don't care.

FIGURE 5. WRITE DISABLE(WDS) CYCLE TIMING

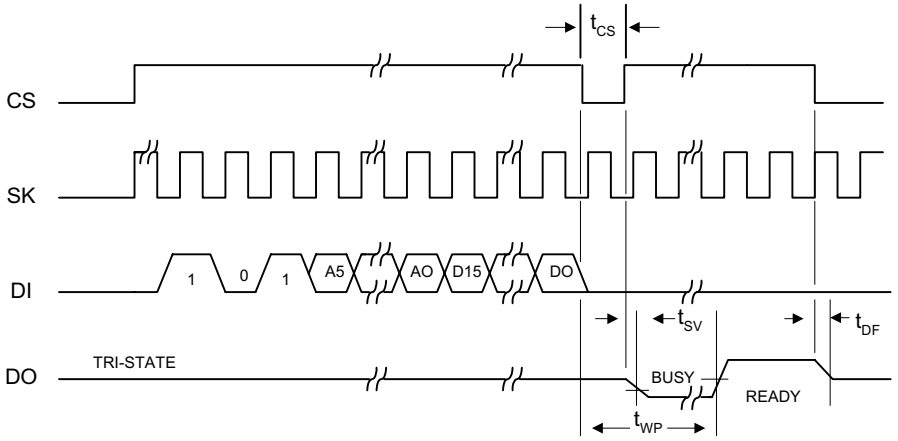


FIGURE 6. WRITE(WRITE) CYCLE TIMING

■ Timing Diagram (3)

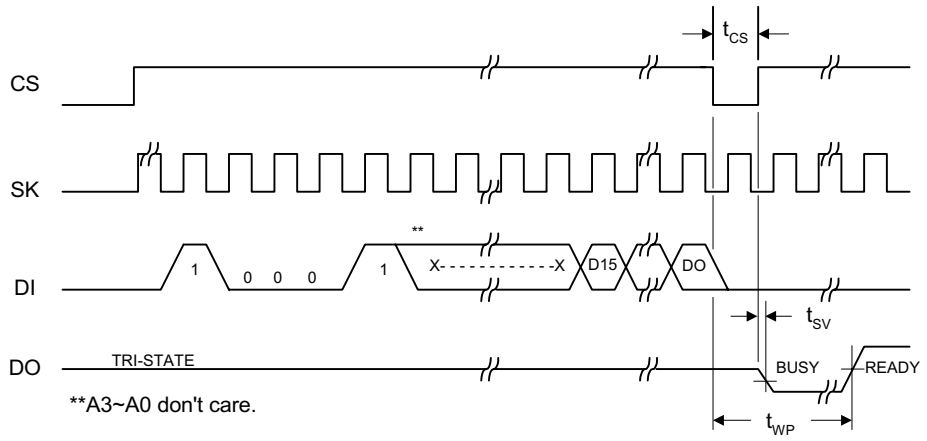


FIGURE 7. WRITE ALL(WRALL) CYCLE TIMING

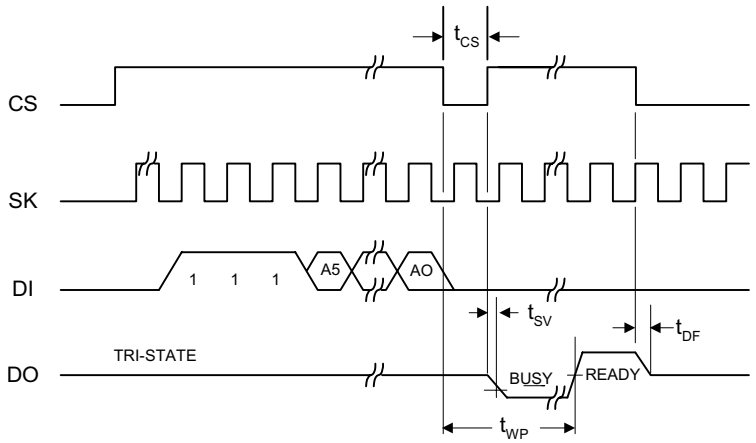


FIGURE 8. ERASE(ERASE) CYCLE TIMING

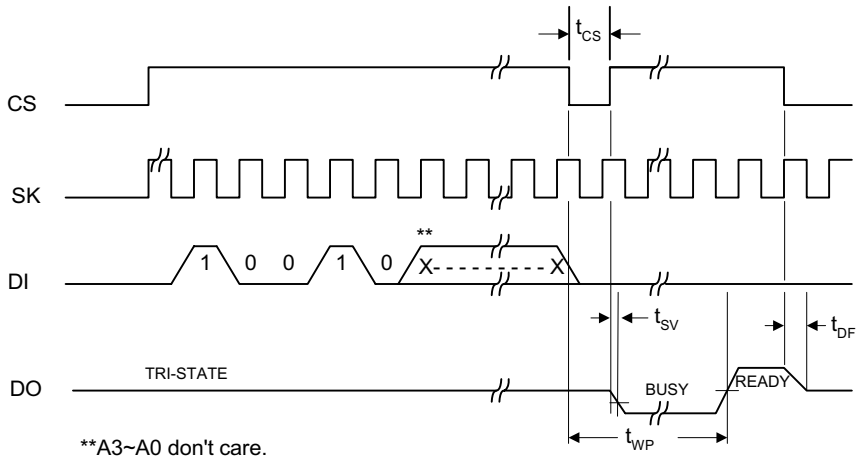
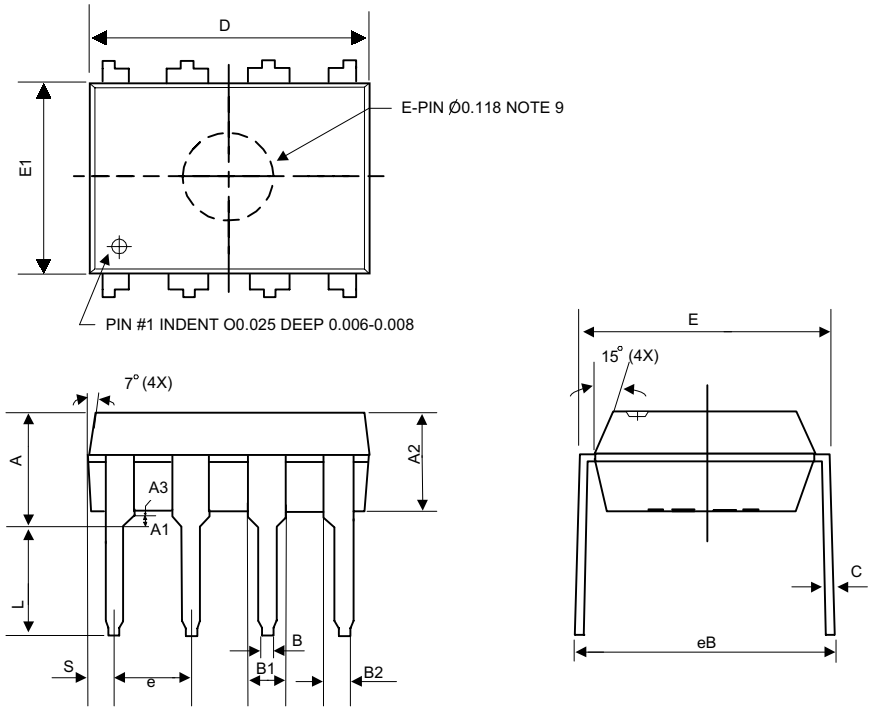


FIGURE 9. ERASE ALL(ERALL) CYCLE TIMING

PACKAGE DIAGRAMS

Plastic Dual-in-line Package(PDIP)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	5.33	-	-	0.210
A1	0.38	-	-	0.015	-	-
A2	3.25	3.30	3.45	0.128	0.130	0.136
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.14	1.27	1.52	0.045	0.050	0.060
B2	0.81	0.99	1.17	0.032	0.039	0.046
C	0.20	0.25	0.33	0.008	0.010	0.013
D	9.12	9.30	9.53	0.359	0.366	0.375
E	7.62	-	8.26	0.300	-	0.325
E1	6.20	6.35	6.60	0.244	0.250	0.260
e	-	2.54	-	-	0.100	-
L	3.18	-	-	0.125	-	-
Eb	8.38	-	9.40	0.330	-	0.370
s	0.71	0.84	0.97	0.028	0.033	0.038

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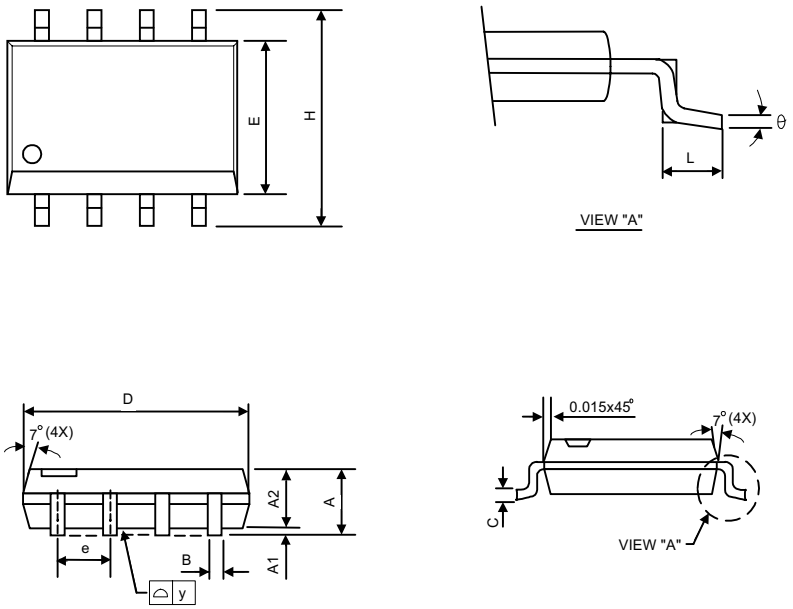
■ Package Diagram (Continued)

(2) JEDEC Small Outline Package (SOP-8L)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	5.00	0.189	0.191	0.197
E	3.80	3.91	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.10	—	—	0.004
θ	0^O	—	8^O	0^O	—	8^O

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