

# SWITCHMODE™ Series NPN Silicon Power Transistor

... designed for high speed, high current, high power applications.

- High DC current gain:  
 $h_{FE} \text{ min} = 20 \text{ at } I_C = 25 \text{ A}$   
 $= 10 \text{ at } I_C = 50 \text{ A}$
- Low  $V_{CE(sat)}$ :  
 $V_{CE(sat)} \text{ max.} = 0.6 \text{ V at } I_C = 25 \text{ A}$   
 $= 0.9 \text{ V at } I_C = 50 \text{ A}$
- Very fast switching times:  
 $T_F = 0.25 \mu\text{s at } I_C = 50 \text{ A}$

### MAXIMUM RATINGS

Rating	Symbol	BUV20	BUV60	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	125		Vdc
Collector–Base Voltage	$V_{CBO}$	160	260	Vdc
Emitter–Base Voltage	$V_{EBO}$	7		Vdc
Collector–Emitter Voltage ( $V_{BE} = -1.5 \text{ V}$ )	$V_{CEX}$	160	260	Vdc
Collector–Emitter voltage ( $R_{BE} = 100 \Omega$ )	$V_{CER}$	150	260	Vdc
Collector–Current — Continuous — Peak ( $PW \leq 10 \text{ ms}$ )	$I_C$	50		Adc
	$I_{CM}$	60		Apk
Base–Current continuous	$I_B$	10		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	250		Watts
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to 200		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	BUV20	BUV60	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.7		$^\circ\text{C/W}$

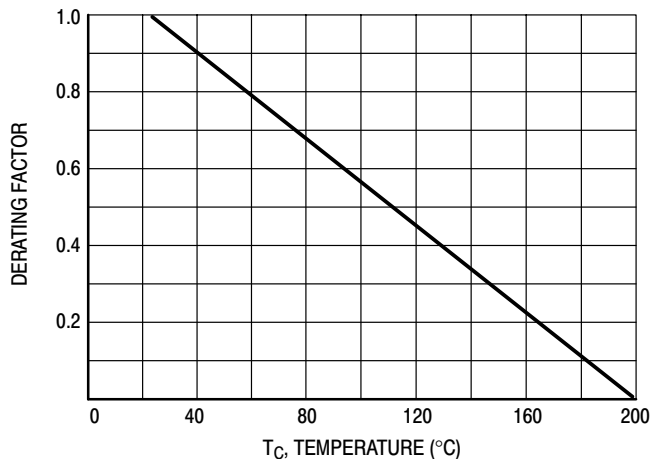
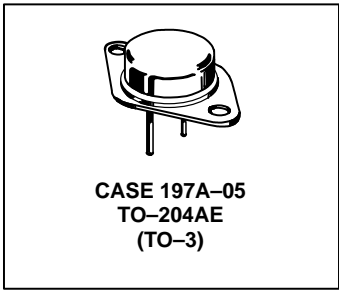


Figure 1. Power Derating

**BUV20**  
**BUV60**

**50 AMPERES**  
**NPN SILICON**  
**POWER**  
**METAL TRANSISTOR**  
**125 VOLTS**  
**250 WATTS**



# BUV20 BUV60

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS<sup>1</sup>

Collector–Emitter Sustaining Voltage ( $I_C = 200\text{ mA}$ , $I_B = 0$ , $L = 25\text{ mH}$ )	BUV20, BUV60	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias ( $V_{CE} = 140\text{ V}$ , $V_{BE} = -1.5\text{ V}$ ) ( $V_{CE} = 140\text{ V}$ , $V_{BE} = -1.5\text{ V}$ , $T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 260\text{ V}$ , $V_{BE} = -1.5\text{ V}$ )	BUV20 BUV20 BUV60	$I_{CEX}$		3.0 12	mAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 100\text{ V}$ )	BUV20	$I_{CEO}$		3.0	mAdc
Emitter–Base Reverse Voltage ( $I_E = 50\text{ mA}$ )	BUV20, BUV60	$V_{EBO}$	7		V
Emitter–Cutoff Current ( $V_{EB} = 5\text{ V}$ )	BUV20, BUV60	$I_{EBO}$		1.0	mAdc

### SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased ( $V_{CE} = 20\text{ V}$ , $t = 1\text{ s}$ ) ( $V_{CE} = 40\text{ V}$ , $t = 1\text{ s}$ )		$I_{S/b}$	12 1.5		Adc
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### ON CHARACTERISTICS<sup>1</sup>

DC Current Gain ( $I_C = 25\text{ A}$ , $V_{CE} = 2\text{ V}$ ) ( $I_C = 50\text{ A}$ , $V_{CE} = 4\text{ V}$ )	BUV20 BUV20	$h_{FE}$	20 10	60 –	
Collector–Emitter Saturation Voltage ( $I_C = 25\text{ A}$ , $I_B = 2.5\text{ A}$ ) ( $I_C = 50\text{ A}$ , $I_B = 5\text{ A}$ )	BUV20 BUV20	$V_{CE(sat)}$		0.6 1.2	Vdc
Base–Emitter Saturation Voltage ( $I_C = 50\text{ A}$ , $I_B = 5\text{ A}$ ) <sub>0</sub>	BUV20	$V_{BE(sat)}$		2.0	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 25\text{ A}$ , $I_B = 1.25\text{ A}$ ) ( $I_C = 50\text{ A}$ , $I_B = 5\text{ A}$ ) ( $I_C = 60\text{ A}$ , $I_B = 7.5\text{ A}$ )	BUV60 BUV60 BUV60	$V_{CE(sat)}$		0.9 0.9 1.2	Vdc
Base–Emitter Saturation Voltage ( $I_C = 50\text{ A}$ , $I_B = 5\text{ A}$ ) ( $I_C = 60\text{ A}$ , $I_B = 7.5\text{ A}$ )	BUV60 BUV60	$V_{BE(sat)}$		1.6 1.8	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ( $V_{CE} = 15\text{ V}$ , $I_C = 2\text{ A}$ , $f = 4\text{ MHz}$ )		$f_T$	8.0		MHz
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### SWITCHING CHARACTERISTICS (Resistive Load)

Turn-on Time	$(I_C = 50\text{ A}$ , $I_{B1} = I_{B2} = 5\text{ A}$ , $V_{CC} = 30\text{ V}$ , $R_C = 0.6\ \Omega$ )	$t_{on}$		1.5	$\mu\text{s}$
Storage Time		$t_s$		1.2	
Fall Time		$t_f$		0.25	

<sup>1</sup> Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

# BUV20 BUV60

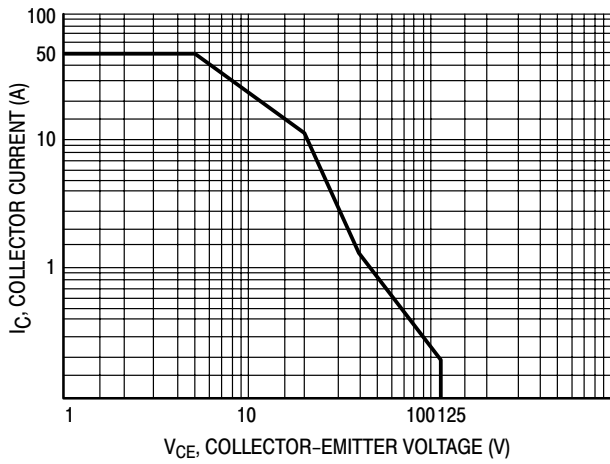


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_C = 25^\circ\text{C}$ .  $T_{J(pk)}$  is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

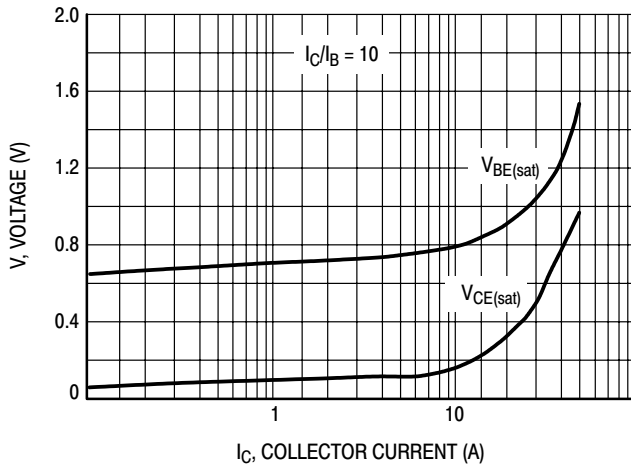


Figure 3. "On" Voltages

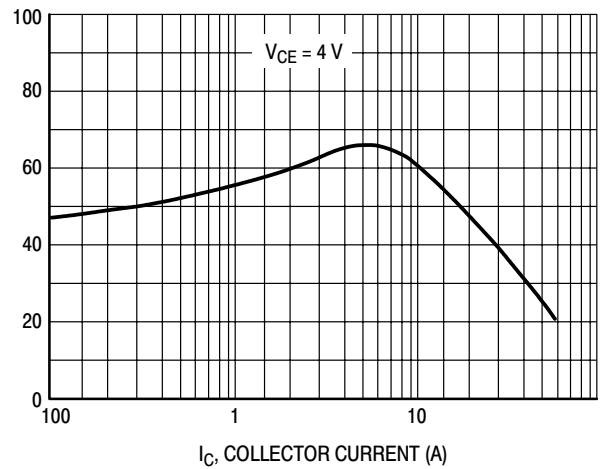


Figure 4. DC Current Gain

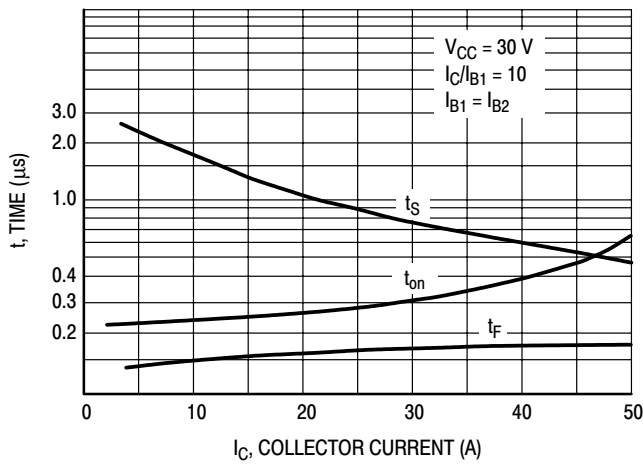


Figure 5. Resistive Switching Performance

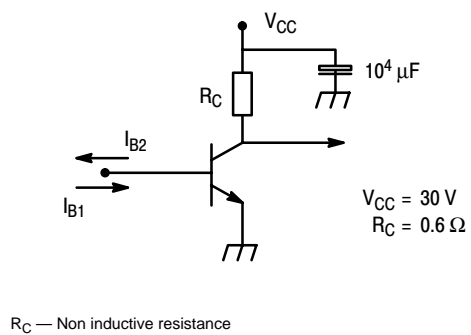
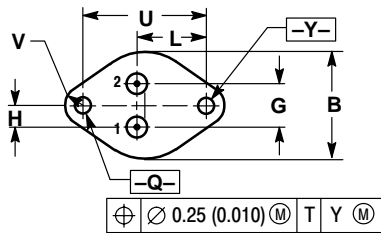
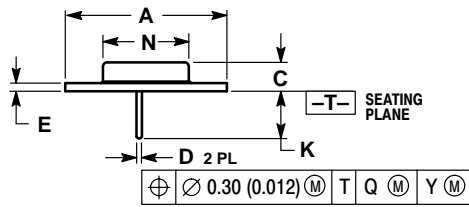


Figure 6. Switching Times Test Circuit

# BUV20 BUV60

## PACKAGE DIMENSIONS


TO-204AE (TO-3)  
CASE 197A-05  
ISSUE J



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

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