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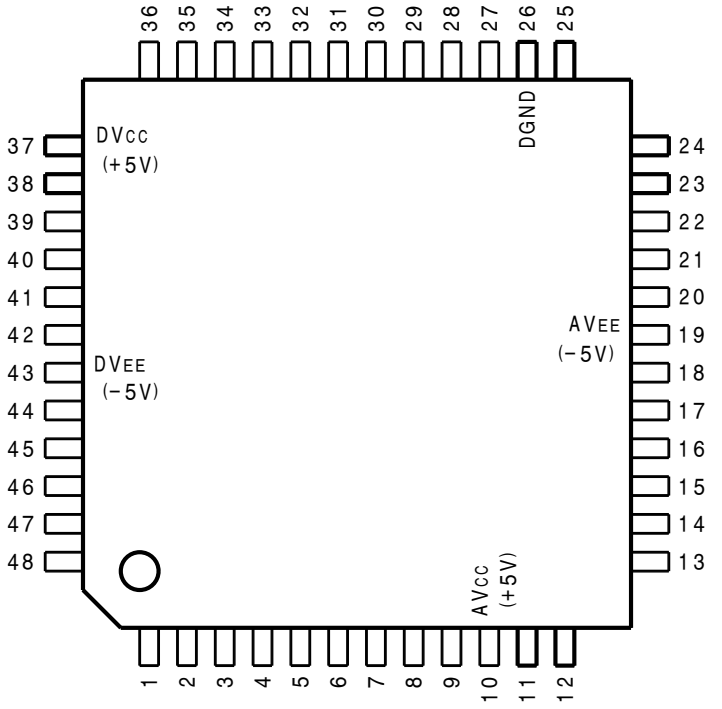
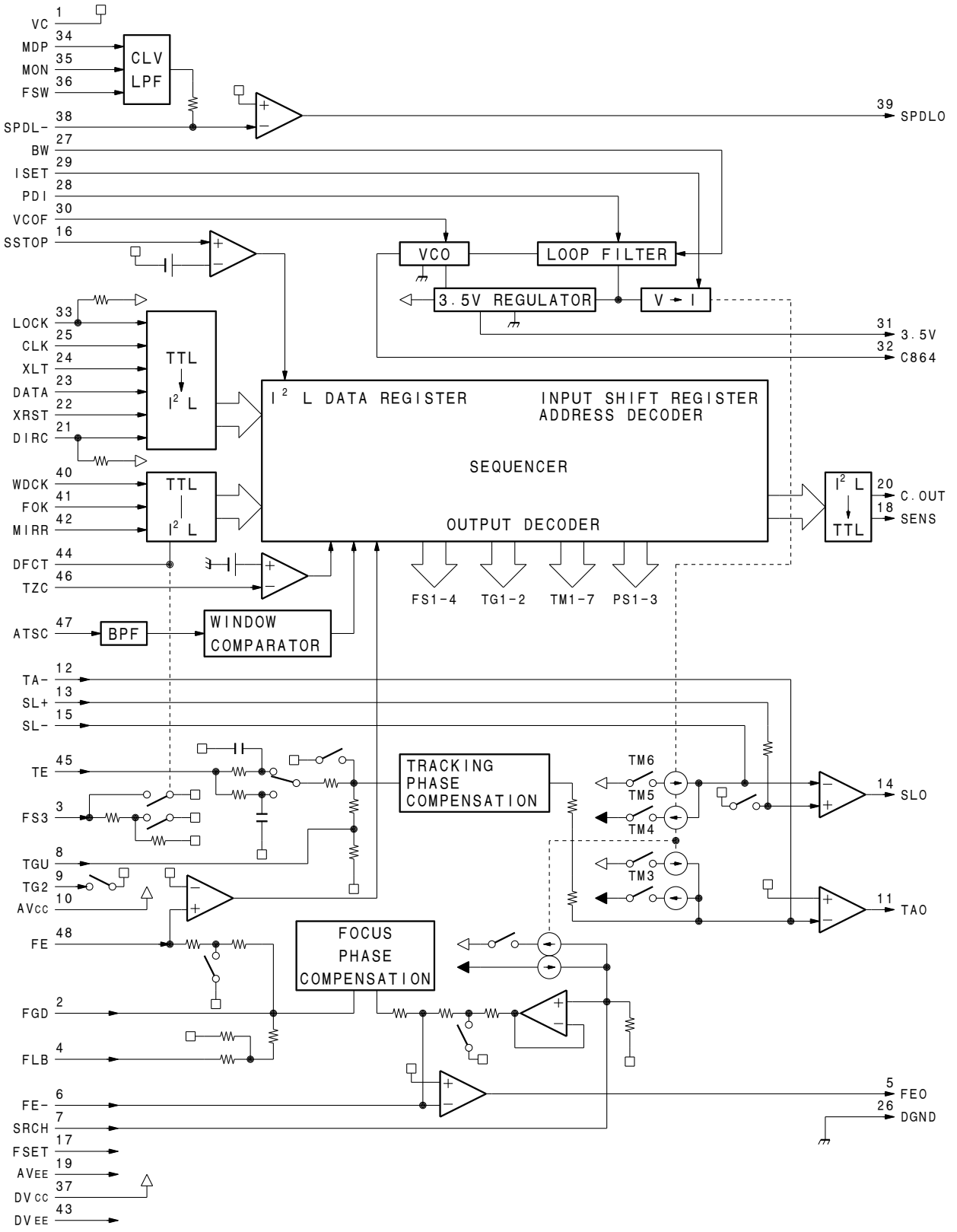
IL08

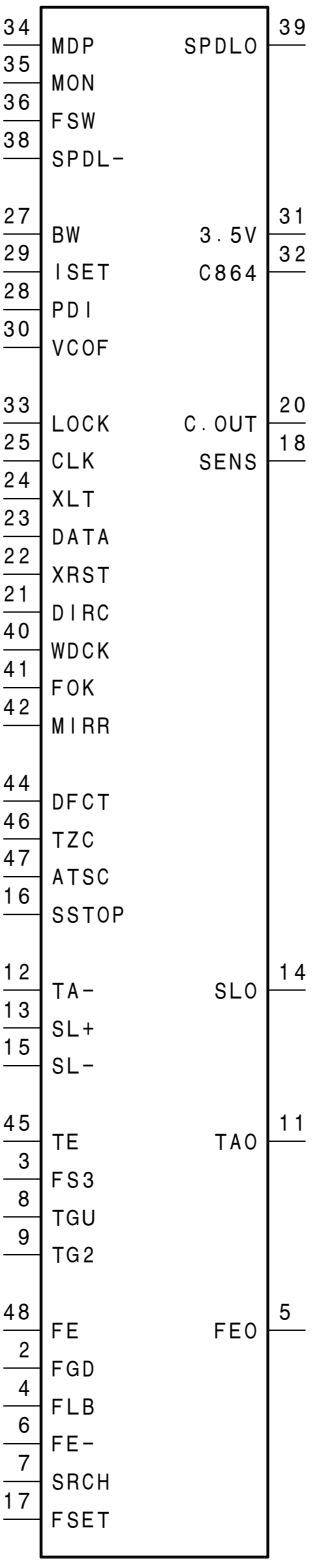
SERVO SIGNAL PROCESSOR FOR CD

-TOP VIEW-



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	VC	13	I	SL+	25	I	CLK	37	I	DVCC
2	I	FGD	14	O	SLO	26	−	DGND	38	I	SPDL−
3	I	FS3	15	I	SL−	27	I	BW	39	O	SPDLO
4	I	FLB	16	I	SSTOP	28	I	PDI	40	I	WDCK
5	O	FEO	17	I	FSET	29	I	ISET	41	I	FOK
6	I	FE−	18	O	SENS	30	I	VCOF	42	I	MIRR
7	I	SRCH	19	I	AVEE	31	O	3.5V	43	I	DVEE
8	I	TGU	20	O	C.OUT	32	O	C864	44	I	DFCT
9	I	TG2	21	I	DIRC	33	I	LOCK	45	I	TE
10	−	AVCC	22	I	XRST	34	I	MDP	46	I	TZC
11	O	TAO	23	I	DATA	35	I	MON	47	I	ATSC
12	I	TA−	24	I	XLT	36	I	FSW	48	I	FE


VC 1
MDP 34
MON 35
FSW 36
CLV LPF
SPDL- 38
39 SPDLO
BW 27
ISET 29
PDI 28
VCOF 30
SSTOP 16
VCO
LOOP FILTER
3.5V REGULATOR
V → I
31 3.5V
32 C864
LOCK 33
CLK 25
XLT 24
DATA 23
XRST 22
DIRC 21
TTL I²L
I² L DATA REGISTER
INPUT SHIFT REGISTER
ADDRESS DECODER
SEQUENCER
OUTPUT DECODER
WDCK 40
FOK 41
MIRR 42
I² L TTL
20 C.OUT
18 SENS
DFCT 44
TZC 46
FS1-4 TG1-2 TM1-7 PS1-3
ATSC 47
BPF
WINDOW COMPARATOR
TA- 12
SL+ 13
SL- 15
TE 45
FS3 3
TGU 8
TG2 9
AVCC 10
TRACKING PHASE COMPENSATION
TM6
TM5
TM4
TM3
14 SLO
11 TAO
FE 48
FOCUS PHASE COMPENSATION
FGD 2
FLB 4
FE- 6
SRCH 7
FSET 17
AVEE 19
DVCC 37
DVEE 43
5 FEO
26 DGND



INPUT

ATSC ;WINDOW COMPARATOR INPUT PIN FOR ATSC DETECTION.
BW ;TIME CONSTANT EXTERNAL PIN FOR LOOP FILTER.
CLK ;SERIAL DATA TRANSFER CLOCK INPUT FROM CPU.
DATA ;SERIAL DATA INPUT FROM CPU.
DFCT ;DEFECT SIGNAL INPUT.
DIRC ;PIN FOR ONE-TRACK JUMP.
FE ;INPUT FOR FOCUS ERROR.
FE- ;INVERSE INPUT PIN FOR FOCUS AMPLIFIER.
FGD ;CONNECT A CAPACITOR BETWEEN THIS PIN AND PIN 3 TO REDUCE HIGH-FREQUENCY GAIN.
FLB ;TIME CONSTANT EXTERNAL PIN TO RAISE THE LOW BANDWIDTH OF THE FOCUS SERVO.
FOK ;FOCUS OK SIGNAL INPUT.
FS3 ;THE HIGH-FREQUENCY GAIN OF THE FOCUS SERVO IS SWITCHED THROUGH FS3 ON AND OFF.
FSET ;PIN TO SET PEAK FREQUENCY OF FOCUS TRACKING PHASE COMPENSATION AND FC OF CLV LPF.
FSW ;TIME CONSTANT EXTERNAL PIN FOR CLV SERVO ERROR SIGNAL
ISET ;CURRENT IS INPUT TO DETERMINE FOCUS SEARCH, TRACK JUMP, AND SLED KICK HEIGHT.
LOCK ;AT"L"SLED RUNAWAY PREVENTION CIRCUIT OPERATES.
MDP ;MDP SIGNAL INPUT.
MIRR ;MIRR SIGNAL INPUT.
MON ;MON SIGNAL INPUT.
PDI ;PDO SIGNAL INPUT.
SL+ ;NON-INVERSE INPUT PIN FOR SLED AMPLIFIER.
SL- ;INVERSE INPUT PIN FOR SLED AMPLIFIER.
SPDL- ;INVERSE INPUT FOR SPINDLE DRIVE AMP.
SRCH ;TIME CONSTANT EXTERNAL PIN FOR THE FORMATION OF FOCUS SEARCH WAVEFORMS.
SSTOP ;LIMIT SW ON/OFF SIGNAL DETECTION PIN FOR DISC INNER PERIPHERY DETECTION.
TA- ;INVERSE INPUT PIN FOR TRACKING AMPLIFIER.
TE ;TRACKING ERROR SIGNAL INPUT.
TG2 ;TIME CONSTANT EXTERNAL PIN FOR THE SELECTION OF TRACKING HIGH BAND GAIN.
TGU ;TIME CONSTANT EXTERNAL PIN FOR THE SELECTION OF TRACKING HIGH BAND GAIN.
TZC ;INPUT FOR TRACKING ZERO-CROSS COMPARATOR.
VCOF ;VCO FREQUENCY CONTROL.
WDCK ;CLOCK INPUT FOR AUTO.
XLT ;LATCH INPUT FROM CPU.
XRST ;RESET INPUT PIN, RESET AT"L"

OUTPUT

C864 ;8.64MHz VCO OUTPUT
C.OUT ;TRACK NUMBER COUNT SIGNAL OUTPUT.
FEO ;FOCUS DRIVE OUTPUT.
SENS ;OUTPUTS FZC, AS, TZC, SSTOP AND BUSY THROUGH COMMAND FROM CPU.
SLO ;SLED DRIVE OUTPUT.
SPDL ;SPINDLE DRIVE OUTPUT.
TAO ;TRACKING DRIVE OUTPUT.