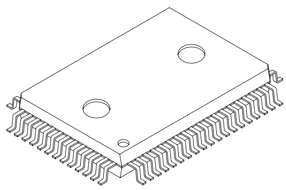
SONY

CXA2076Q

Y/C/RGB/D for PAL/NTSC Color TVs

For the availability of this product, please contact the sales office.

64 pin QFP (Plastic)



Description

The CXA2076Q is a bipolar IC which integrates the luminance signal processing, chroma signal processing, RGB signal processing, and sync and deflection signal processing functions for NTSC/PAL system color TVs onto a single chip. This IC includes deflection processing functions for wide-screen TVs, and is also equipped with a SECAM decoder interface, making it possible to construct a TV system that supports multiple color systems.

Features

- I^2C bus compatible
- Compatible with both PAL and NTSC systems (also compatible with SECAM if a SECAM decoder is connected)
- Built-in deflection compensation circuit capable of supporting various wide modes
- Countdown system eliminates need for H and V oscillator frequency adjustment
- Automatic identification of 50/60Hz vertical frequency (forced control possible)
- Non-interlace display support (even/odd selectable)
- Automatic identification of PAL, NTSC, and SECAM color systems (forced control possible)
- Automatic identification of 4.43MHz/3.58MHz crystal (forced control possible)
- Non-adjusting Y/C block filter
- One CV input, one set of Y/C inputs, two sets of analog RGB inputs (one set of which can serve as both analog and digital inputs)
- Built-in AKB circuit
- Support for forcing YS1 off

Applications

Color TVs (4:3, 16:9)

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C, SGND, DGND = 0V)

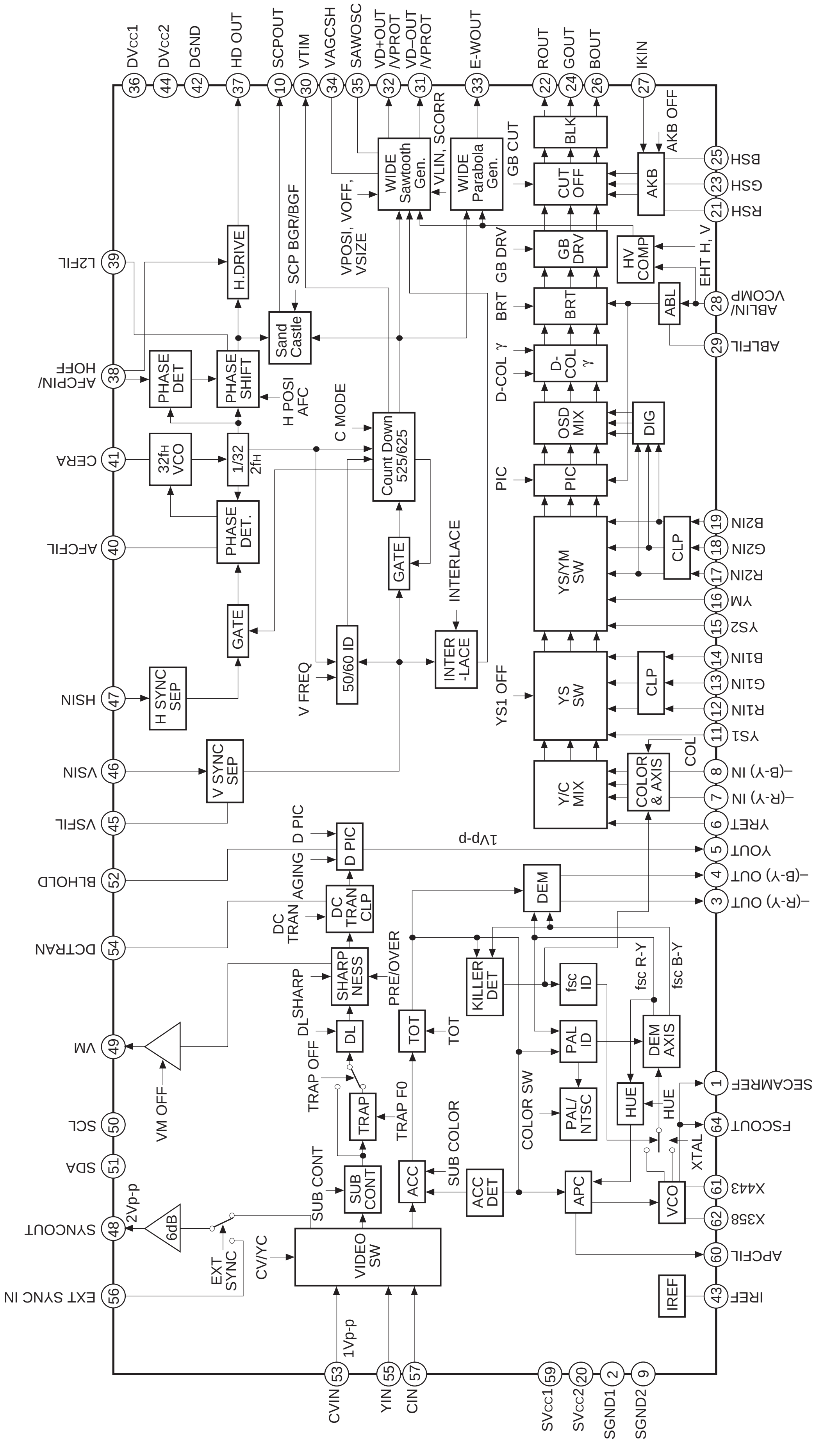
• Supply voltage	SVcc1, 2, DVcc1, 2	–0.3 to 12	V
• Operating temperature	Topr	–20 to +65	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	PD	1.7 (when mounted on 50mm × 50mm board)	W
• Voltages at each pin		–0.3 to SVcc1, SVcc2, DVcc1, DVcc2 + 0.3	V

Operating Conditions

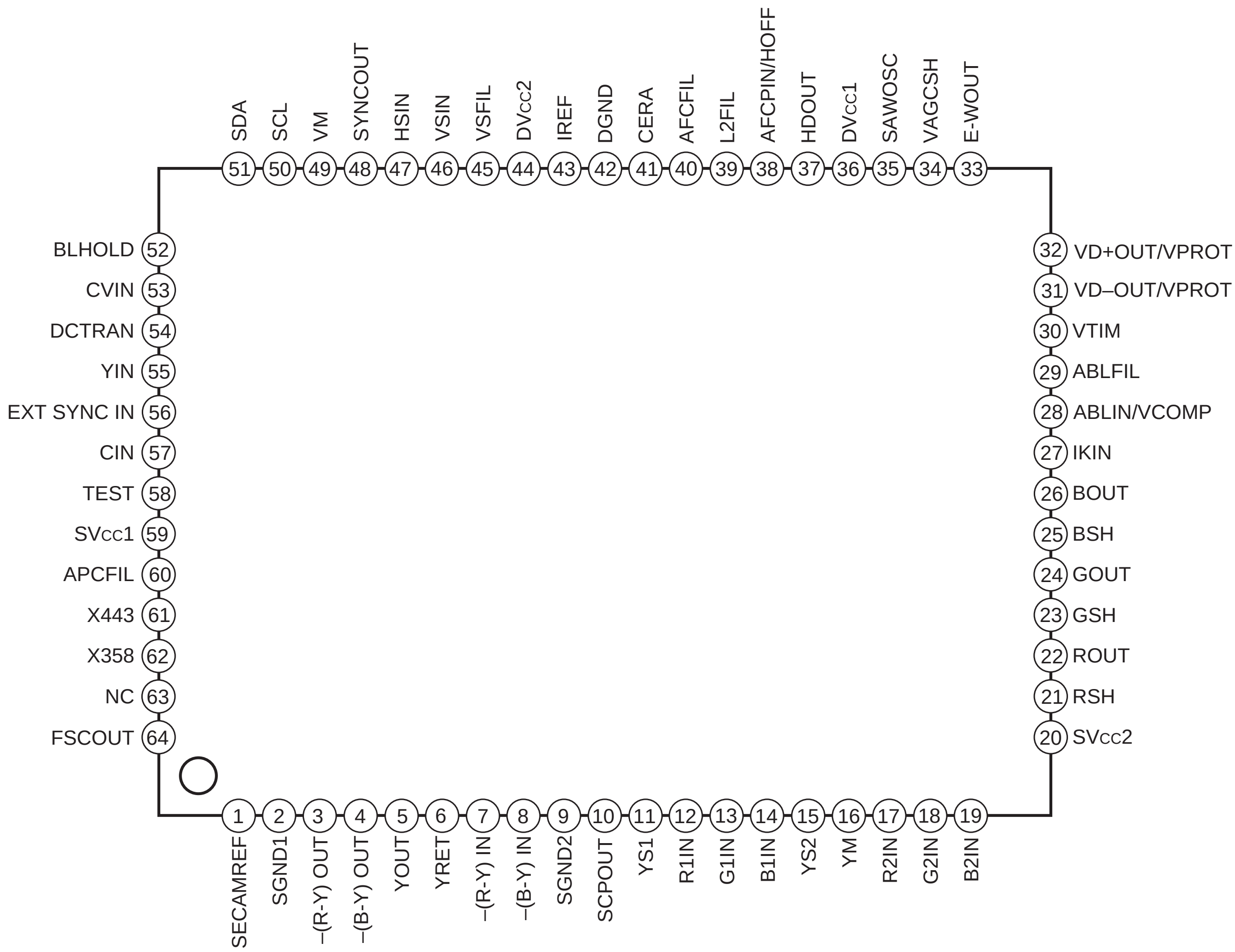
Supply voltage	SVcc1, 2	9.0 ± 0.5	V
	DVcc1, 2	9.0 ± 0.5	V

E96Z27-PS

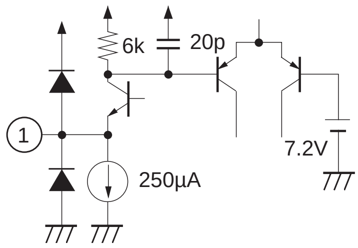
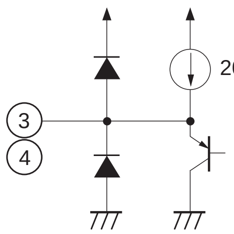
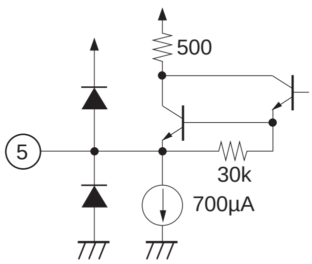
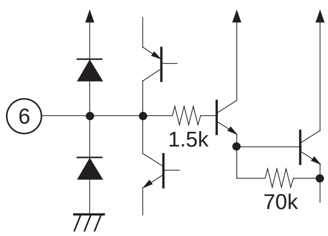
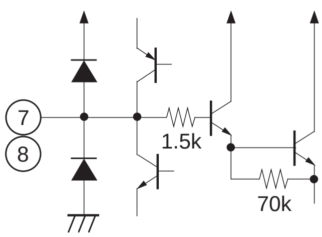
Block Diagram

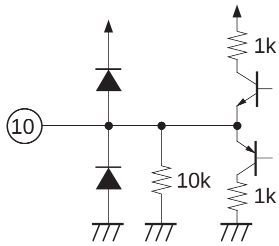
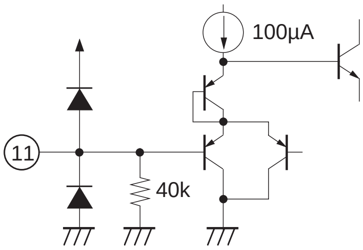
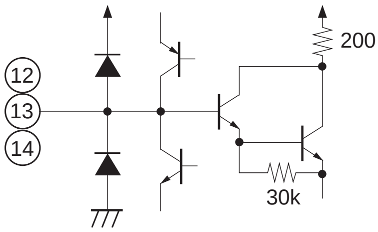
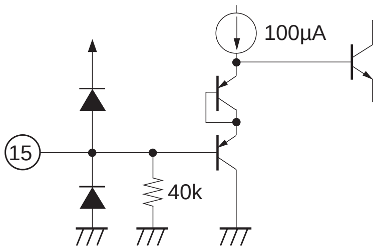
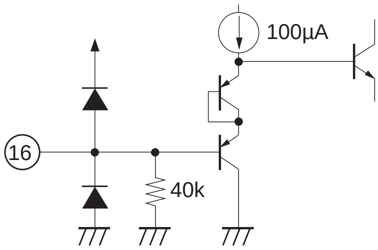


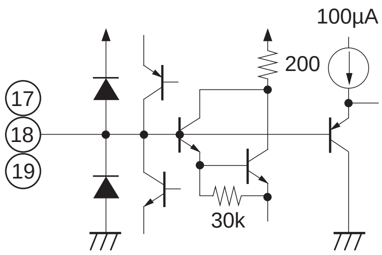
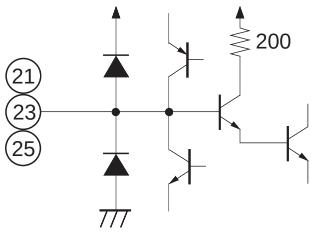
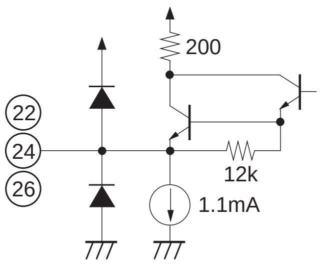
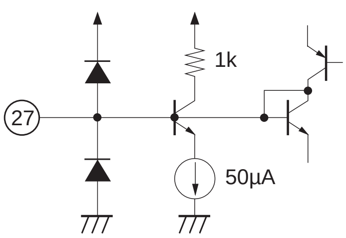
Pin Configuration

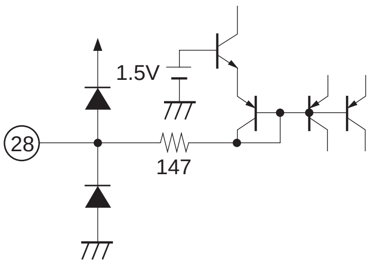
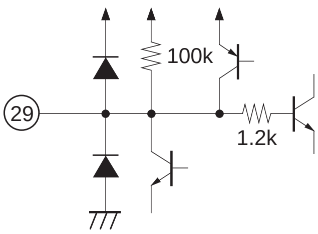
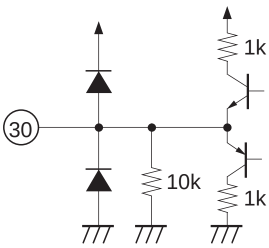
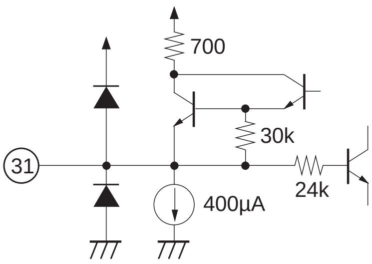
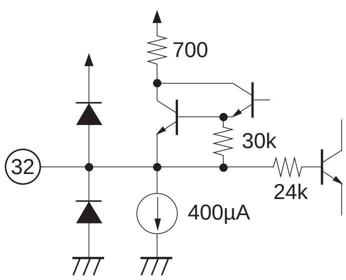


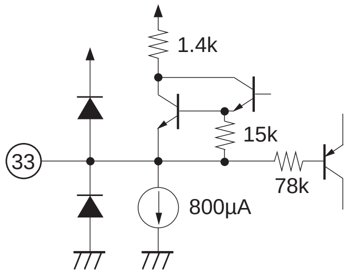
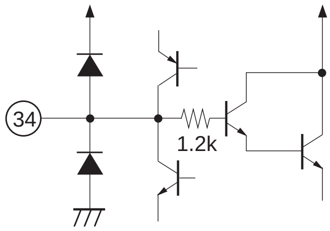
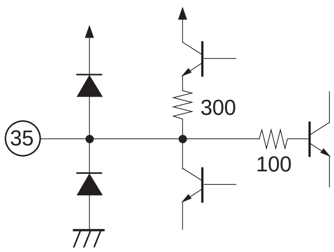
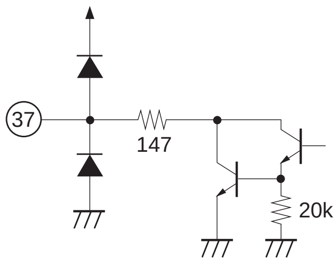
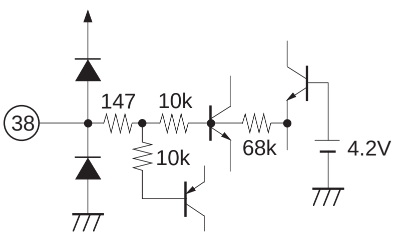
Pin Description

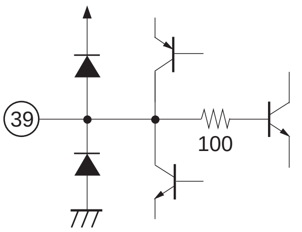
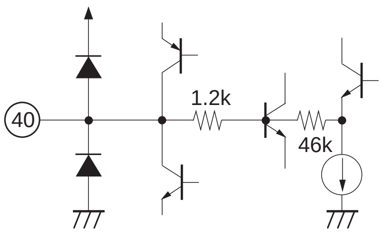
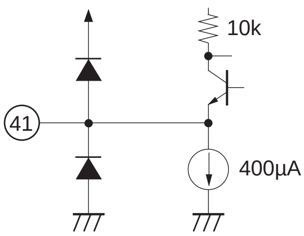
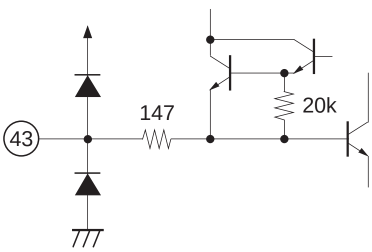
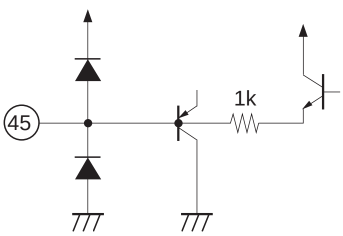
Pin No.	Symbol	Equivalent circuit	Description
1	SECAMREF		SECAM decoder interface. This pin serves as both a 4.43MHz output and as a SECAM identification input/output pin.
2	SGND1	—	GND for Y/C block.
3 4	–(R-Y) OUT –(B-Y) OUT		Color difference signal outputs. Go to high impedance when the SECAM system is detected. Standard output levels for 75% CB: B-Y: 0.665Vp-p R-Y: 0.525Vp-p
5	YOUT		Luminance signal output. Black level is 3.5VDC. Standard output level for 100 IRE input: 1Vp-p
6	YRET		Luminance signal input. Clamped to 4.8V at the burst timing. Standard input level for 100 IRE input: 1Vp-p
7 8	–(R-Y) IN –(B-Y) IN		Color difference signal inputs. Clamped to 5.5V at the burst timing. Standard input levels for 75% CB: B-Y: 1.33Vp-p R-Y: 1.05Vp-p
9	SGND2		GND for the RGB block.

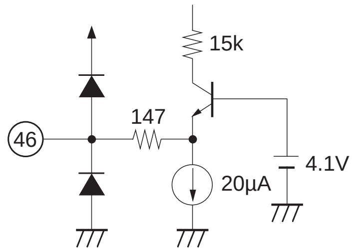
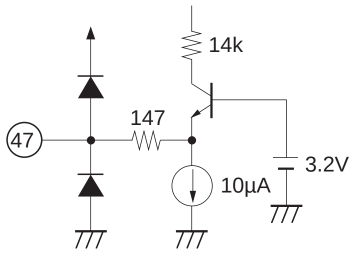
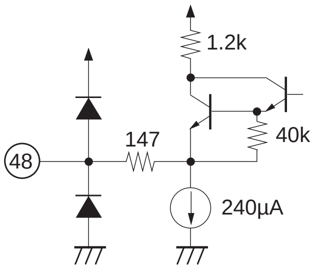
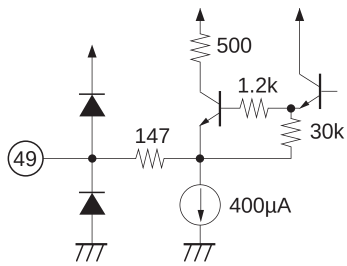
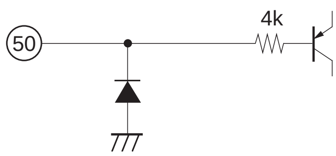
Pin No.	Symbol	Equivalent circuit	Description
10	SCPOUT		Sand castle pulse output. The 0 to 5V BGP pulse, the phase of which is controlled through the bus, is superimposed with the 0 to 2V H and VBLK pulse for output.
11	YS1		YSSW control input. When YS is high, the RGB1 block signal is selected; when YS is low, the Y/C block is selected. This function can be disabled by the YS1OFF setting for the I^2C bus. VILMAX = 0.4V VIHMIN = 1.0V
12 13 14	R1IN G1IN B1IN		Analog R, G and B signal inputs. Input a 0.7Vp-p (no sync, 100 IRE) signal via a capacitor. The signal is clamped to 5.7V at the burst timing of the signal input to the HSIN input pin (Pin 47).
15	YS2		YS/YMSW YS control input. When YS is high, the RGB2 block signal is selected; when YS is low, the YSSW output signal is selected. VILMAX = 0.4V VIHMIN = 1.0V
16	YM		YS/YMSW YM control input. When YM is high, the YSSW output signal is attenuated by 9.6dB. VILMAX = 0.4V VIHMIN = 1.0V

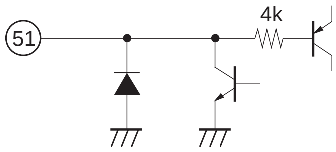
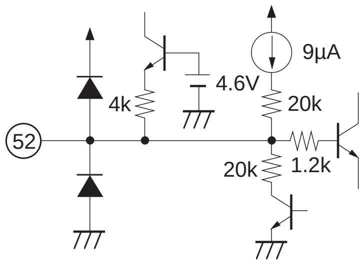
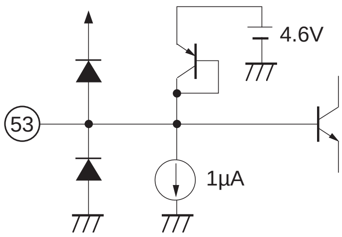
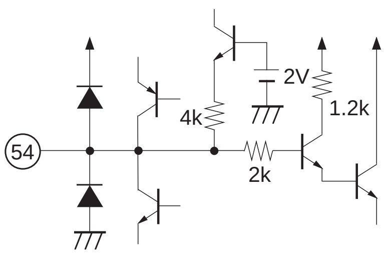
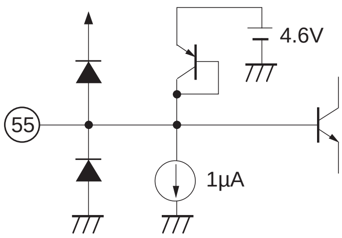
Pin No.	Symbol	Equivalent circuit	Description
17 18 19	R2IN G2IN B2IN		Analog/digital (dual-purpose) RGB signal inputs. The input signals are input via capacitors. When using analog input, input a 0.7Vp-p signal (no sync, 100 IRE); when using digital input, input a signal of at least 1.5Vp-p (Vth = 1.2V). The display level is 67 IRE. When using digital input, digital input is selected regardless of the YS setting. In addition, the VM output is turned off. These pins are clamped to 5.7V at the burst timing of the signal input to the sync input pin (Pin 47).
20	SVcc2		Power supply for RGB block.
21 23 25	RSH GSH BSH		Sample-and-hold for R, G and B AKB. Connect to GND via a capacitor. When not using AKB (manual CUTOFF mode), R, G and B cut-off voltage can be controlled by applying a control voltage to each pin. The control voltage is 4.5 ± 1V.
22 24 26	ROUT GOUT BOUT		R, G and B signal outputs. 2.5Vp-p is output during 100% white input.
27	IKIN		Input the signal converted from the CRT beam current (cathode current Ik) to a voltage via a capacitor. The V blanking part is clamped to 2.7V at the V retrace timing. The input for this pin is the reference pulse return, and the loop operates so that the Rch is 1Vp-p and the G and Bch are 0.81Vp-p. The G and Bch can be varied by ±0.5V by the bus CUTOFF control. When not using AKB, this pin should be open.

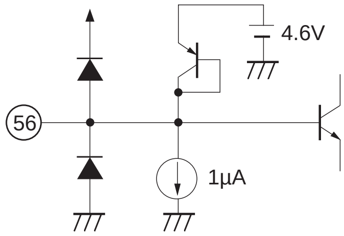
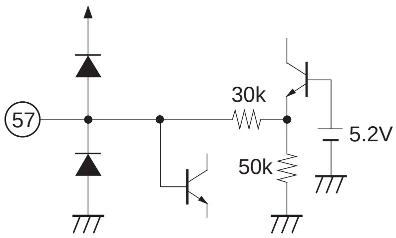
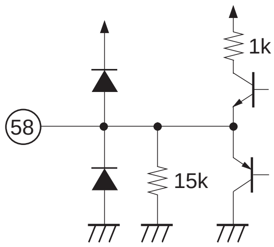
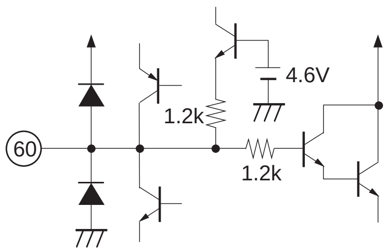
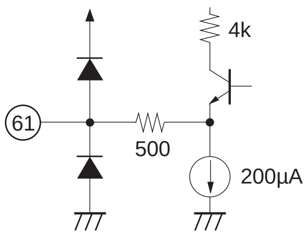
Pin No.	Symbol	Equivalent circuit	Description
28	ABLIN/VCOMP		ABL control signal input and VSAW high voltage fluctuation compensation signal input. High voltage compensation has linear control characteristics for the pin voltage range of about 8V to 1V. The control characteristics can be varied through EHT-V control of the bus. ABL begins to have effect below a threshold voltage of about 1.2V. ABL functions as PIC/BRT-ABL (average value type).
29	ABLFIL		Connect a capacitor to form the LPF of the ABL control signal.
30	VTIM		V timing pulse output. Outputs the timing pulse from V sync identification to the end of V blanking. Pulses are positive polarity from 1 to 6V. During zoom mode, the V blanking pulse which has been expanded before and after the V sync is superimposed and output as the 1 to 3V pulse.
31	VD–OUT/VPROT		V sawtooth wave output and V protect signal input. When a large current (3mA) is drawn from this pin, the RGB outputs are all blanked and "1" is output to the status register VNG.
32	VD+OUT/VPROT		Serves as both a V sawtooth wave output with the reverse polarity of VD–OUT, and a Vprotect signal input. The Vprotect function can even be applied to this pin.

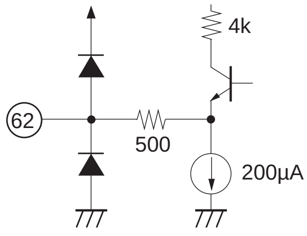
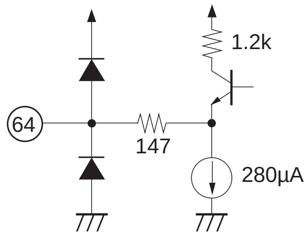
Pin No.	Symbol	Equivalent circuit	Description
33	E-WOUT		V parabola wave output.
34	VAGCSH		Sample-and-hold for AGC which maintains the V sawtooth wave at a constant amplitude. Connect to GND via a capacitor.
35	SAWOSC		Connect a capacitor to generate the V sawtooth wave. For the capacitor, use an MPS (metalized polyester capacitor), etc., with a small tan δ.
36	DV$_{CC}$1		Power supply for the V deflection block.
37	HD OUT		H drive signal output. This signal is output with the open collector.
38	AFCPIN/HOFF		H deflection pulse input for H AFC. Input an about 5Vp-p pulse via a capacitor. Set the pulse width to 10 to 12µs. This pin is also used as the hold-down signal input for the HD output, and if this pin is 1V or less for a 7V cycle or longer, the hold-down function operates and the HD output is held to 9VDC. In addition, the RGB outputs are all blanked. Outputs "1" to the status register XRAY.

Pin No.	Symbol	Equivalent circuit	Description
39	L2FIL		Filter for H AFC. Connect to GND via a capacitor. The H phase can also be controlled from this pin by leading current in and out of this capacitor. As the pin voltage rises, the picture shifts to the left; as the pin voltage drops, the picture shifts to the right.
40	AFCFIL		CR connection for the AFC lag-lead filter.
41	CERA		Connect the 32 × FH VCO ceramic oscillator.
42	DGND		GND for the deflection block.
43	IREF		Internal reference current setting. Connect to GND via a resistor with an error of less than 1% (such as a metal film resistor).
44	$DV_{CC}2$		Power supply for the H deflection block.
45	VSFIL		Filter for V sync separation. Connect to GND via a capacitor.

Pin No.	Symbol	Equivalent circuit	Description
46	VSIN		Sync signal input for V sync separation. Input a 2Vp-p Y signal (or a 0.6Vp-p sync signal).
47	HSIN		Sync signal input for H sync separation. Input a 2Vp-p Y signal (or a 0.6Vp-p sync signal).
48	SYNCOUT		Sync signal output for VSIN and HSIN. The output can be selected from the internal sync signals (Pin 53 or Pin 55) or the external sync signal (Pin 56) by the I^2C bus. Output signal level: 2Vp-p (0.6Vp-p sync only) Input/output gain: 6dB
49	VM		Outputs the differential waveform of the VM (Velocity Modulation) Y signal. (6.6VDC, 1.1Vp-p) The signal advanced for 200ns from YOUT is output. The delay time versus YIN is determined by the DL setting of the I^2C bus. This output can be turned off through the I^2C bus. This output can also be turned off by YS1, YM, and YS2.
50	SCL		I^2C bus protocol SCL (Serial Clock) input. VILMAX = 1.5V VIHMIN = 3.5V

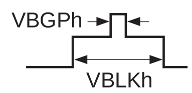
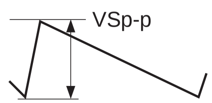
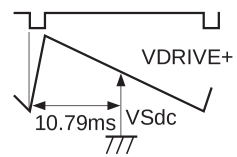
Pin No.	Symbol	Equivalent circuit	Description
51	SDA		I^2C bus protocol SDA (Serial Data) I/O. VILMAX = 1.5V VIHMIN = 3.5V VOLMAX = 0.4V
52	BLHOLD		Capacitor connection for black peak hold of the dynamic picture (black expansion).
53	CVIN		Composite video signal input. Input the 1Vp-p (100% white including sync) CV signal via a capacitor. The sync level of the input signal is clamped to 3.8V.
54	DCTRAN		Connect a capacitor that determines the DC transmission ratio to GND.
55	YIN		Y signal input. Input a 1Vp-p (100% white including sync) Y signal via a capacitor. The sync level of the input signal is clamped to 3.8V.

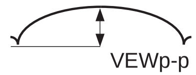
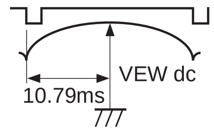
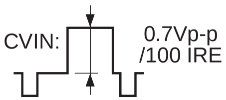
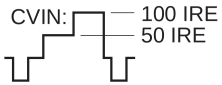
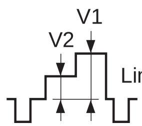
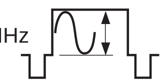
Pin No.	Symbol	Equivalent circuit	Description
56	EXT SYNC IN		External sync signal input. Input a 0.3Vp-p sync signal (or a 1Vp-p CV signal or Y signal) via a capacitor. The sync level of the input signal is clamped to 3.8V.
57	CIN		Chroma signal input. Input a C signal with a burst level of 300mVp-p via a capacitor. Input signal is biased to 4.5V internally.
58	TEST		Test pin. Outputs a 0 to 3V V-SYNC SEP with positive polarity. If not used, leave this pin open.
59	SVcc1		Power supply for Y/C block.
60	APCFIL		CR connection for the chroma APC lag-lead filter.
61	X443		Connect a 4.433619MHz crystal oscillator.

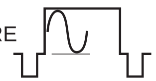
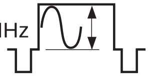
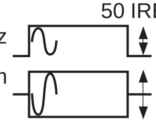
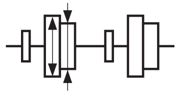
Pin No.	Symbol	Equivalent circuit	Description
62	X358		Connect a 3.579545MHz crystal oscillator.
63	NC		Not connected. Normally connected to GND to prevent interference with other pins.
64	FSCOUT		Subcarrier output. Output level: 5.2VDC, 0.4Vp-p

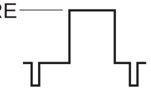
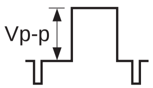
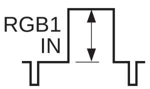
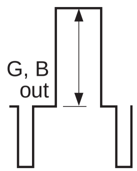
Electrical Characteristics

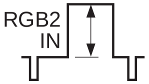
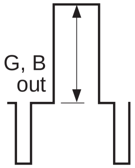
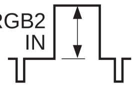
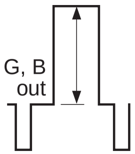
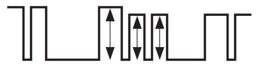
Setting conditions
- Ta = 25°C, $SV_{CC}1, 2 = DV_{CC}1, 2$ = 9V, SGND1, 2 = DGND = 0V
- Measures the following after setting the I²C bus register as shown in "I²C Bus Register Initial Settings".

No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
1	Signal block current consumption	SICC	V_{CC} = 9.0V, Bus data = center	20, 59	Measure the pin inflow current.	42	65	90	mA
2	Sync block current consumption	DICC	V_{CC} = 9.0V, Bus data = center	36, 44	Measure the pin inflow current.	30	48	67	mA
Sync deflection block items									
3	Horizontal free-running frequency	fHFR	AFC MODE = 0h	37	HDRIVE output frequency	15.55	15.734	15.90	kHz
4	Horizontal sync pull-in range	ΔfHR	SYNCIN: composite sync	—	Confirm that I²C status register HLOCK is 1 (the pull-in range when f_H is shifted from 15.734kHz).	–400	—	400	Hz
5	HD output pulse width	HDw	SYNCIN: composite sync	37	Measure the pulse width for the section where the HDRIVE output is high.	24.5	25.5	26.5	µs
6	SCP BLK output pulse width	VBLKh	SCP Measure the pulse width for the section where the BLK output is high.	10		11.6	12.1	12.6	µs
7	SCP BGP output pulse width	VBGPh	SCP Measure the pulse width for the section where the BGP output is high.	10		2.5	2.9	3.3	µs
8	VDRIVE output amplitude	VSp-p	SYNCIN: composite sync	31, 32	Measure the VDRIVE output Vp-p. 	0.9	1.0	1.1	V
9	VDRIVE output center potential	VSdc		31, 32		2.9	3.0	3.1	V

No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
10	EWDRIVE output amplitude	VEWp-p	SYNCIN: composite sync	33	Measure the EWDRIVE output Vp-p. 	0.42	0.52	0.62	V
11	EWDRIVE output center potential	VEWdc		33		3.8	3.95	4.1	V
Signal block items									
12	R, G and B output amplitude	VRout1		22, 24, 26	Output amplitude when a video signal with an amplitude of 0.7Vp-p/100 IRE is input.	2.25	2.5	2.85	V
13	R, G and B output linearity	Lin		22, 24, 26	 $Lin = \frac{V1}{V2 \times 2} \times 100$	96	100	104	%
14	C-TRAP attenuation (3.58MHz)	C-Trap3.58	 TRAPOFF = 0/1 TRAP-F0 = 7h	22	Input fsc to CVIN. Ratio of the fsc component of the Yout amplitude when CTRAP = 1 against the Yout amplitude when CTRAP = 0. 	—	–30	—	dB

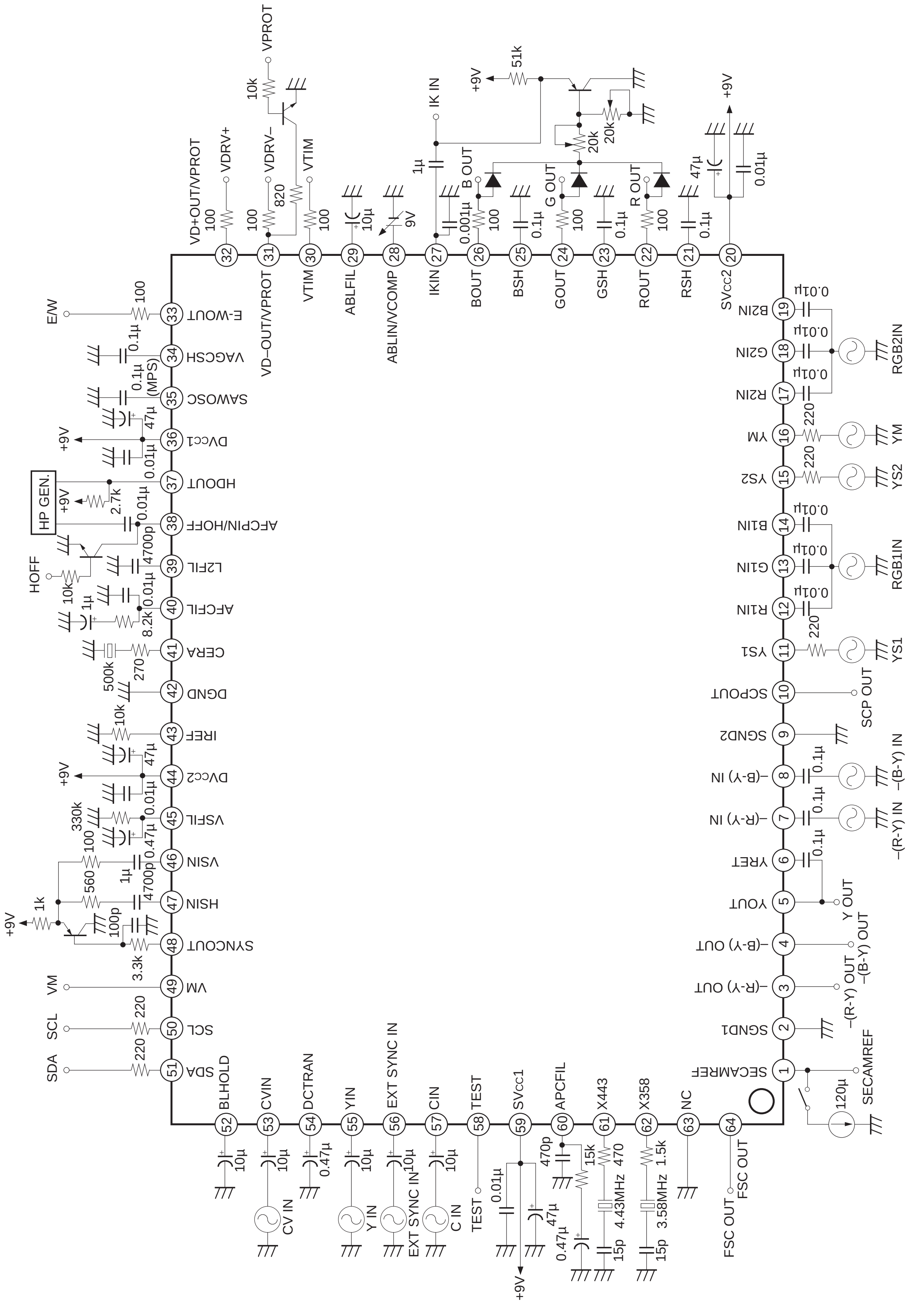
No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
15	C-TRAP attenuation (4.43MHz)	C-Trap4.43	CVIN: fsc, 50 IRE  TRAPOFF = 0/1 TRAP-F0 = 7h	22	Input fsc to CVIN. Ratio of the fsc component of the Yout amplitude when CTRAP = 1 against the Yout amplitude when CTRAP = 0. f = 4.43MHz 	—	–30	—	dB
16	VM output	Vvm	CVIN: 3MHz, 50 IRE VMOFF = 0	49	50 IRE f = 3MHz Vvm 	0.75	0.95	1.15	V
17	Color difference –(R-Y) output	Vr-y	4.43MHz PAL input burst fsc 300mVp-p 640mVp-p fsc + 90° CIN  450mVp-p fsc + 0°, fsc + 180° SUB-COLOR = 7h	3	–(R-Y) OUT  Vr-y	440	510	570	mV
18	Color difference –(B-Y) output	Vb-y		4	–(B-Y) OUT  Vb-y	570	640	710	mV
19	Color gain –(R-Y)	Vcolr-y	–(R-Y) IN: 525mVp-p  PAL input: COLOR = 1Fh	22	ROUT  Vcolr-y	1.4	1.6	1.8	V
20	Color gain –(B-Y)	Vcolb-y	–(B-Y) IN: 665mVp-p  PAL input: COLOR = 1Fh	24	BOUT  Vcolb-y	1.1	1.3	1.5	V

No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
21	Hue center offset	ϕoffset	HUE = 1Fh, SUB – HUE = 7h	—		–8	0	8	deg
22	Killer point	KP	CVIN: Burst only	—		—	–35	—	dB
23	APC pull-in range	ΔfAPC		—	Confirm that the burst frequency is pulled in at 3.58MHz ±400Hz.	–400	—	400	Hz
24	Dynamic color operation R output	ΔGdcolR		22	ROUT, BOUT 	94	96	98	%
25	Dynamic color operation B output	ΔGdcolB	D-COL = 0/1	24	$\Delta GdcolR = \frac{Vp\text{-}p\ (DCOL = 1)}{Vp\text{-}p\ (DCOL = 0)} \times 100$ $\Delta GdcolB = \frac{Vp\text{-}p\ (DCOL = 1)}{Vp\text{-}p\ (DCOL = 0)} \times 100$	102	104	106	%
26	YM gain	ΔGYM		22, 24, 26	Output amplitude ratio when the R, G and BOUT YM = 1 and 0	–10.6	–9.6	–8.6	dB
27	R output amplitude during linear R1 input	VLR1out	YS1: 1V RGB1IN: 0.7Vp-p	22	 VLR1out = Vout	1.85	2.05	2.25	V
28	G output amplitude during linear G1 input	VLG1out	YS1: 1V RGB1IN: 0.7Vp-p	24	 VLG1out = Vout	1.85	2.05	2.25	V
29	B output amplitude during linear B1 input	VLB1out	YS1: 1V RGB1IN: 0.7Vp-p	26	VLB1out = Vout	1.85	2.05	2.25	V

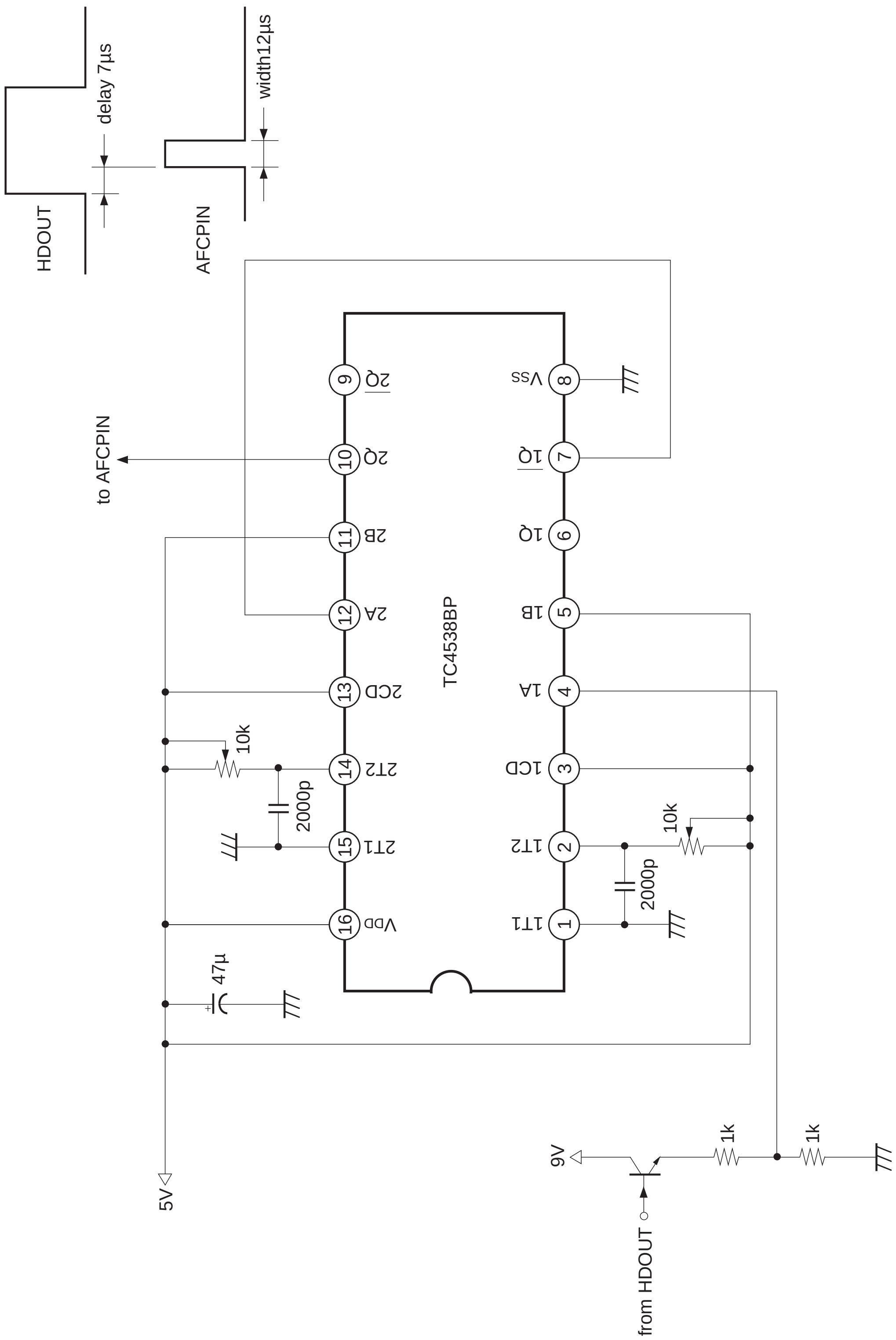
No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents		Min.	Typ.	Max.	Unit
30	R output amplitude during linear R2 input	VLR2out	YS2: 1V RGB2IN: 0.7Vp-p	22	 RGB2 IN	VLR2out = Vout	1.85	2.05	2.25	V
31	G output amplitude during linear G2 input	VLG2out	YS2: 1V RGB2IN: 0.7Vp-p	24	 R, G, B out	VLG2out = Vout	1.85	2.05	2.25	V
32	B output amplitude during linear B2 input	VLB2out	YS2: 1V RGB2IN: 0.7Vp-p	26		VLB2out = Vout	1.85	2.05	2.25	V
33	R output amplitude during digital R2 input	VDRout	RGB2IN: 1.5Vp-p	22	 RGB2 IN	VDRout = Vout	58	67	75	IRE
34	G output amplitude during digital G2 input	VDGout	RGB2IN: 1.5Vp-p	24	 R, G, B out	VDGout = Vout	58	67	75	IRE
35	B output amplitude during digital B2 input	VDBout	RGB2IN: 1.5Vp-p	26		VDBout = Vout	58	67	75	IRE
36	IK level R	VIKR	SYNCIN: composite sync GCUTOFF = 0h BCUTOFF = 0h	27	 VIKG VIKR VIKB		0.85	1.00	1.15	V
37	IK level G	VIKG		27			0.22	0.35	0.5	V
38	IK level B	VIKB		27			0.22	0.35	0.5	V

Electrical Characteristics Measurement Circuit

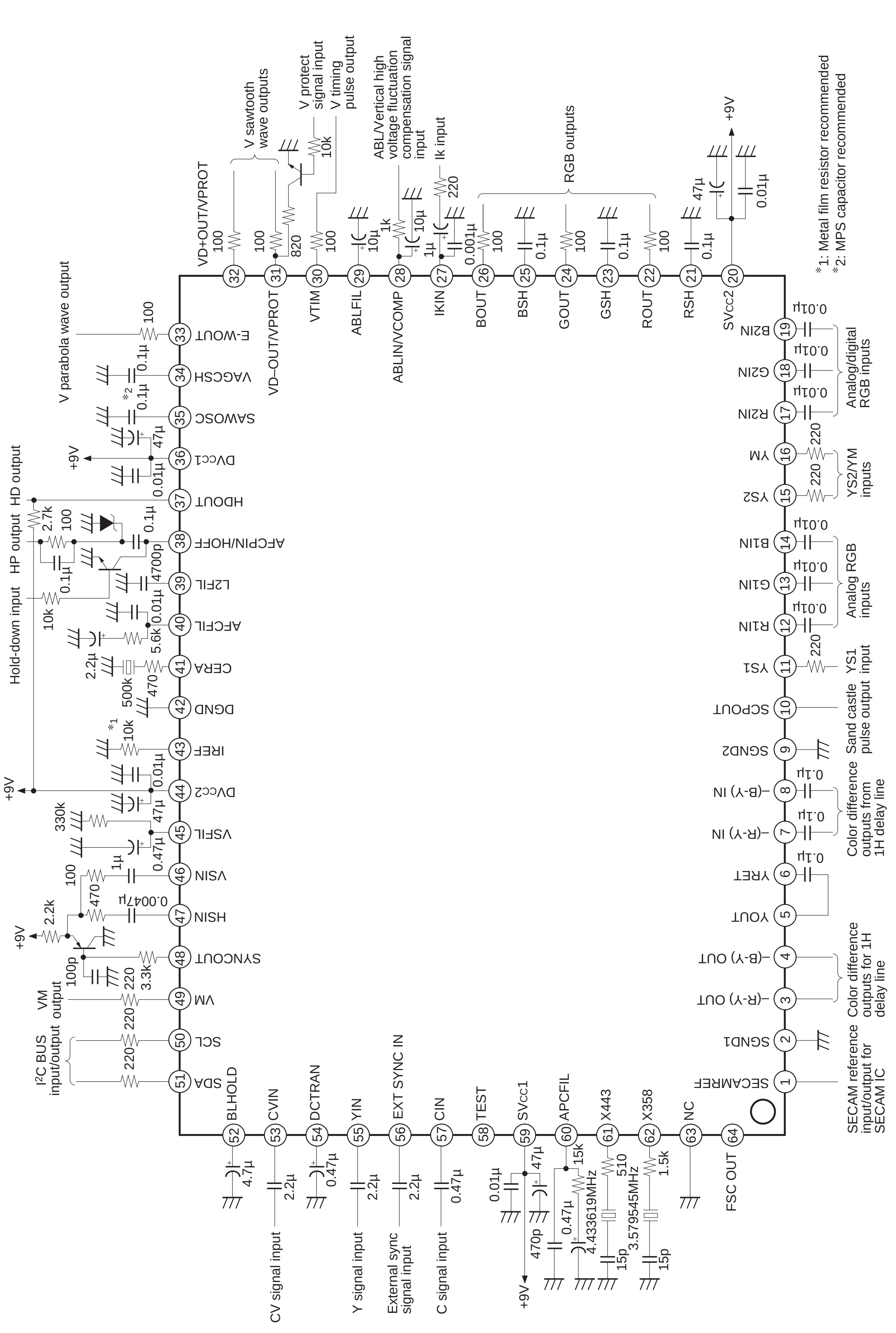
Signal sources ~ are all GND unless otherwise specified in the Measurement conditions column of Electrical Characteristics.



HP GEN.


HDOUT
AFCPIN
delay 7µs
width12µs
TC4538BP
to AFCPIN
from HDOUT
5V
9V
47µ
10k
10k
2000p
2000p
1k
1k
VDD
2T1
2T2
2CD
2A
2B
2Q
2Q
VSS
1Q
1Q
1B
1A
1CD
1T2
1T1

Application Circuit



*1: Metal film resistor recommended
*2: MPS capacitor recommended

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Electrical Characteristics Measurement Conditions "I²C Bus Register Initial Settings"

Register name	No. of bits	Initial setting	Description
PICTURE	6	3Fh	Maximum value
TRAPOFF	1	1h	TRAP off
VMOFF	1	1h	VM off
HUE	6	1Fh	Center value
DCTRAN	1	0h	DCTRAN off
D-PIC	1	0h	DPIC off
COLOR	6	1Fh	Center value
TOT	1	0h	TOT off
BRIGHT	6	1Fh	Center value
D-COL	1	0h	DCOL off
SHARPNESS	4	7h	Center value
PRE-OVER	2	3h	Maximum value
COLOR SW	2	0h	Automatic switching
SUB-CONT	4	7h	Center value
TRAP F0	4	7h	Center value
SUB-COLOR	4	7h	Center value
UP-CORNER-PIN	4	7h	Center value
SUB-BRIGHT	6	1Fh	Center value
GAMMA	2	0h	Minimum value
G-DRIVE	6	2Ah	Center value
AGING	1	0h	AGING off
B-DRIVE	6	2Ah	Center value
INTERLACE	2	0h	Interlace
G-CUTOFF	4	0h	Minimum value
B-CUTOFF	4	0h	Minimum value
RON	1	1h	R output on
GON	1	1h	G output on
BON	1	1h	B output on
PICON	1	1h	Picture mute off
VOFF	1	0h	VD output on
FHHI	1	0h	FH normal
CD-MODE	1	0h	Automatic switching
AKBOFF	1	0h	AKB on
V-SIZE	6	1Fh	Center value
V FREQ	2	0h	Automatic switching

Register name	No. of bits	Initial setting	Description
V-POSITION	6	1Fh	Center value
AFC-MODE	2	1h	Low gain
S-CORR	4	0h	Minimum value
V-LIN	4	7h	Center value
H-SIZE	6	1Fh	Center value
REF-POSI	2	3h	Maximum value
PIN-COMP	6	1Fh	Center value
VBLKW	2	0h	Minimum value
H-POSITOPN	4	7h	Center value
PIN-PHASE	4	7h	Center value
AFC-BOW	4	7h	Center value
AFC-ANGLE	4	7h	Center value
SCP BGR	2	1h	Center value
SCP BGF	2	1h	Center value
XTAL	2	0h	Automatic switching
EXT SYNC	1	0h	Internal sync
CV/YC	1	0h	CV input
V-ASPECT	6	0h	Minimum value
ZOOM SW	1	0h	ZOOM SW off
HBLKSW	1	0h	HBLKSW off
V-SCROLL	6	1Fh	Center value
JMPSW	1	0h	JMPSW off
HSIZESW	1	0h	HSIZESW off
UP-VLIN	4	0h	Minimum value
LO-VLIN	4	0h	Minimum value
LEFT-BLK	4	7h	Center value
RIGHT-BLK	4	7h	Center value
EHT H	2	0h	EHT H off
EHT V	2	0h	EHT V off
LO-CORNER-PIN	4	7h	Center value
YS1OFF	1	0h	YS1 normal
DL	3	3h	Center value
KIL-OFF	1	0h	Normal
CRT-TYP	1	0h	16:9 CRT

Definition of I²C Bus Registers

Slave Addresses

88h: Slave Receiver
89h: Slave Transmitter

Register Table

"*": Undefined

Control Register

Sub Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
××× 0 0 0 0 0 00 h	PICTURE						TRAPOFF	VMOFF
××× 0 0 0 0 1 01 h	HUE						DC-TRAN	D-PIC
××× 0 0 0 1 0 02 h	COLOR						TOT	*
××× 0 0 0 1 1 03 h	BRIGHT						D-COL	*
××× 0 0 1 0 0 04 h	SHARPNESS				PRE-OVER		COLOR SW	
××× 0 0 1 0 1 05 h	SUB-CONT				TRAP F0			
××× 0 0 1 1 0 06 h	SUB-COLOR				UP-CORNER-PIN			
××× 0 0 1 1 1 07 h	SUB-BRIGHT						GAMMA	
××× 0 1 0 0 0 08 h	G-DRIVE						AGING	0
××× 0 1 0 0 1 09 h	B-DRIVE						INTERLACE	
××× 0 1 0 1 0 0A h	G-CUTOFF				B-CUTOFF			
××× 0 1 0 1 1 0B h	RON	GON	BON	PICON	VOFF	FHHI	CD-MODE	AKBOFF
××× 0 1 1 0 0 0C h	V-SIZE						V-FREQ	
××× 0 1 1 0 1 0D h	V-POSITION						AFC-MODE	
××× 0 1 1 1 0 0E h	S-CORR				V-LIN			
××× 0 1 1 1 1 0F h	H-SIZE						REF-POSI	
××× 1 0 0 0 0 10 h	PIN-COMP						VBLKW	
××× 1 0 0 0 1 11 h	H-POSITION				PIN-PHASE			
××× 1 0 0 1 0 12 h	AFC-BOW				AFC-ANGLE			
××× 1 0 0 1 1 13 h	SCP BGR		SCP BGF		XTAL		EXT SYNC	CV/YC
××× 1 0 1 0 0 14 h	V-ASPECT						ZOOM SW	HBLKSW
××× 1 0 1 0 1 15 h	V-SCROLL						JMP SW	HSIZESW
××× 1 0 1 1 0 16 h	UP-VLIN				LO-VLIN			
××× 1 0 1 1 1 17 h	LEFT-BLK				RIGHT-BLK			
××× 1 1 0 0 0 18 h	EHT H		EHT V		LO-CORNER-PIN			
××× 1 1 0 0 1 19 h	*	*	KIL-OFF	CRT-TYP	YS1 OFF	DL		

Status Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
H LOCK	IKR	VNG	XRAY	COLOR SYS			FV

Description of Registers

Register name (No. of bits)

1. Video switch register

CV/YC	(1)	: CV input/YC input selector 0 = CV input selected 1 = YC input selected
EXT SYNC	(1)	: EXT SYNC selector switch 0 = Internal sync (CV or Y) selected 1 = EXT SYNC selected

2. Y signal block register

SUB-CONT	(4)	: Contrast gain control (Y gain control) 0h = –3.5dB 7h = 0dB Fh = +2.5dB
TRAP-F0	(4)	: Chroma trap f0 fine adjustment (Y block chroma trap current control) 0h = High 7h = Center Fh = Low
SHARPNESS	(4)	: Sharpness gain control (Sharpness F0 3MHz) 0h = –6dB 7h = +2.5dB Fh = +6.5dB
PRE-OVER	(2)	: Sharpness preshoot/overshoot ratio control 0h = 1:1 (PRE: OVER) 3h = 2:1
VM OFF	(1)	: Y signal output ON/OFF for VM 0 = ON 1 = OFF
TRAP OFF	(1)	: Y block chroma trap ON/OFF 0 = Trap ON 1 = Trap OFF
DL	(3)	: Y signal delay time control (80ns/step) 0h = Max. 7h = Min.

DC-TRAN (1) : Y DC transmission ratio selector switch
0 = 100%
1 = 81%

D-PIC (1) : Y black expansion ON/OFF switch
0 = OFF
1 = ON Point of inflection: 30 IRE

3. C signal block register

TOT (1) : Chroma TOT filter band selector switch
0 = TOT — TRAP OFF
1 = TOT — TRAP ON (TRAP fo 2MHz)

COLOR (6) : Color gain control (Chroma gain control)
0h = Color OFF (–40dB or less)
1Fh = 0dB B output: 1.02Vp-p (I/O gain: +11dB, 0.285Vp-p input)
3Fh = +6dB

SUB-COLOR (4) : Color gain control (ACC reference level control)
0h = –5dB
7h = 0dB
Fh = +3dB

HUE (6) : Hue control (Phase control for chroma demodulation axis)
Control not possible for a PAL system.
0h = +35° Flesh color appears red.
1Fh = 0°
3Fh = –35° Flesh color appears green.

XTAL (2) : XTAL selection setting switch
0h = Automatic identification
1h = Force to XTAL1 (3.58MHz)
2h = Force to XTAL2 (4.43MHz)

COLOR SW (2) : Color system setting
0h = Automatic identification
1h = Force to PAL
2h = Force to NTSC
3h = Force to SECAM

KIL-OFF (1) : Forced color killer OFF switch
0 = Normal operation
1 = Forced color killer OFF

4. RGB signal block register

PICTURE (6) : Picture gain control (RGB gain control)
0h = –14dB
3Fh = 0dB RGB output: 2.5Vp-p (I/O gain: +8dB, 1Vp-p input)

BRIGHT (6) : Bright control (RGB DC bias control)
0h = –440mV
1Fh = 0mV (–300mV for REF-P level)
3Fh = +450mV

SUB-BRIGHT (6) : Bright control (RGB DC bias control)
0h = –440mV
1Fh = 0mV (–300mV for REF-P level)
3Fh = +450mV

G-DRIVE (6) : Gch drive gain adjustment (Gch gain control)
0h = G/R –4.5dB
2Ah = G/R 0dB (G/R 0dB)
3Fh = G/R +1.5dB

B-DRIVE (6) : Bch drive gain adjustment (Bch gain control)
0h = B/R –4.5dB
2Ah = B/R 0dB (B/R 0dB)
3Fh = B/R +1.5dB

G-CUTOFF (4) : Gch cut-off adjustment (Gch reference pulse value control of IKIN pin input)
0h = +34%
7h = +81% (G/R)
Fh = +135%

B-CUTOFF (4): Bch cut-off adjustment (Bch reference pulse value control of IKIN pin input)
0h = +34%
7h = +81% (B/R)
Fh = +135%

D-COL (1) : Dynamic color ON/OFF switch
0 = Dynamic color OFF
1 = Dynamic color ON (R, Bch level control)

GAMMA (2) : Gamma control (RGB gamma correction amount control)
0h = Gamma OFF
3h = Gamma peak 17 IRE (at input 40 IRE), +400mV (at 2.5Vp-p OUT)

REF-POSITION (2) : Reference pulse timing setting
0h = From rising edge of V TIM: Rch 22H, Gch 23H, Bch 24H
1h = From rising edge of V TIM: Rch 20H, Gch 21H, Bch 22H
2h = From rising edge of V TIM: Rch 18H, Gch 19H, Bch 20H
3h = From rising edge of V TIM: Rch 16H, Gch 17H, Bch 18H

PIC-ON (1) : ON/OFF switch for RGB output with a reference pulse
(Set to OFF mode at power-on.)
0 = RGB output OFF (All blanked status)
1 = RGB output ON

R ON (1) : ON/OFF switch for Rch video output without a reference pulse
(Operates when PIC ON = 1, set to OFF mode at power-on.)
0 = Rch video output OFF (Blanked status, reference pulse only output)
1 = Rch video output ON

G ON (1) : ON/OFF switch for Gch video output without a reference pulse
(Operates when PIC ON = 1, set to OFF mode at power-on.)
0 = Gch video output OFF (Blanked status, reference pulse only output)
1 = Gch video output ON

B ON (1) : ON/OFF switch for Bch video output without a reference pulse
(Operates when PIC ON = 1, set to OFF mode at power-on.)
0 = Bch video output OFF (Blanked status, reference pulse only output)
1 = Bch video output ON

AKB OFF (1) : AKB ON/OFF switch (Set to ON mode at power-on.)
0 = AKB ON
1 = AKB OFF (IK CLAMP, IK S/H and reference pulse fixed to OFF)
R, G and B cut-off adjustment at AKB OFF performed by voltage applied to RSH, GSH and BSH pins, respectively.

YS1 OFF (1) : YS1 forced OFF mode/YS1 normal mode
0 = YS1 normal mode
1 = YS1 forced OFF mode

5. Deflection block register

AFC-MODE	(2)	: AFC loop gain control (PLL between H SYNC and H VCO) 0h = H free run mode 1h = Small gain 2h = Medium gain 3h = Large gain
FH-HI	(1)	: H oscillator frequency fixation ON/OFF switch (Set to ON mode at power-on.) 0 = H oscillator frequency fixation OFF AFC normal mode 1 = H oscillator frequency fixation ON Oscillator frequency fixed to maximum value (approx. 16.2kHz).
V FREQ	(1)	: V frequency mode setting 0, 1h = Automatic identification 2h = Forced mode (50Hz) 3h = Forced mode (60Hz)
V OFF	(1)	: V sawtooth wave oscillation stop ON/OFF switch (Set to OFF mode at power-on.) 0 = Oscillation stop OFF (V DRIVE– and V DRIVE+: normal output) 1 = Oscillation stop ON (V DRIVE– and V DRIVE+: DC output and DC value vary according to V POSITION.)
CD-MODE	(1)	: V countdown system mode selector (Set to automatic selection mode during power-on.) 0 = Non-standard signal mode, standard signal mode and no signal mode automatically selected 1 = Fixed to non-standard signal mode (V oscillator frequency is 55Hz during no signal mode "free run".)
VBLKW	(2)	: VBLK width control (Blanked pulses after reference pulse. Operates when JMPSW = 1; blanked pulses after reference pulse fixed to 1H when JMPSW = 0.) 0h = 12H from Bch reference pulse 1h = 11H from Bch reference pulse 2h = 10H from Bch reference pulse 3h = 9H from Bch reference pulse
H-POSITION	(4)	: Horizontal position adjustment (HAFC phase control) 0h = 1µs delay Picture position shifts to right. (Picture delayed with respect to HD.) 7h = 0µs Fh = 1µs advance Picture position shifts to left. (Picture advanced with respect to HD.)
V-POSITION	(6)	: Vertical position adjustment (V SAW output DC bias control) 0h = –0.09V Picture position drops, V DRIVE+ output DC Down. 1Fh = 0V Center potential: DC 3V 3Fh = +0.09V Picture position rises, V DRIVE+ output DC Up.

V-SIZE (6) : Vertical amplitude adjustment (V SAW output gain control)
0h = –14% Vertical picture size decreases.
1Fh = 0% Amplitude: 1.23Vp-p, center potential: DC 3V when V-ASPECT is 2FH.
3Fh = +14% Vertical picture size increases.

V-LIN (4) : Vertical linearity adjustment (Gain control for V SAW secondary component)
0h = 115% (Bottom/top of picture) Top of picture compressed; bottom of picture expanded.
7h = 100% (Bottom/top of picture)
Fh = 85% (Bottom/top of picture) Top of picture expanded; bottom of picture compressed.

S-CORR (4) : Vertical S correction amount adjustment (V SAW secondary component gain control)
0h = Secondary component amplitude by adding sawtooth and other signals = 0
Fh = Secondary component amplitude by adding sawtooth and other signals = Maximum

AFC-BOW (4) : Vertical line bow compensation amount adjustment (Phase control according to HAFC parabola wave)
0h = Top and bottom of picture delayed 500ns with respect to picture center.
7h = 0 ns
Fh = Top and bottom of picture advanced 500ns with respect to picture center.

AFC-ANGLE (4) : Vertical line slope compensation amount adjustment (Phase control according to HAFC V SAW)
0h = Top of picture delayed 1000ns, bottom of picture advanced 1000ns with respect to picture center.
7h = 0 ns
Fh = Top of picture advanced 1000ns, bottom of picture delayed 1000ns with respect to picture center.

PIN-COMP (6) : Horizontal pin distortion compensation amount adjustment (V parabola wave gain control)
0h = 0.10Vp-p Horizontal size for top/bottom of picture increases. (Compensation amount minimum)
1Fh = 0.58Vp-p Amplitude, center potential: DC 4V when V-ASPECT is 2Fh
3Fh = 1.06Vp-p Horizontal size for top/bottom of picture decreases. (Compensation amount maximum)

H-SIZE (6) : Horizontal amplitude adjustment (V parabola wave DC bias control)
0h = –0.5V Horizontal picture size decreases, EW-DRIVE output DC Down.
1Fh = 0V Amplitude: 0.58Vp-p, center potential: DC 4 V when V-ASPECT is 2Fh
3Fh = +0.5V Horizontal picture size increases, EW-DRIVE output DC Up.

EHT-H (2) : Horizontal high-voltage fluctuation compensation amount setting (DC adjustment for parabolic output)
0h = 0V (Compensation amount when 1V is applied to ABL IN versus 8V applied to ABL IN)
3h = –0.1V (Compensation amount when 1V is applied to ABL IN versus 8V applied to ABL IN)

EHT-V (2) : Vertical high-voltage fluctuation compensation amount setting (V SAW output gain control)
0h = 0% (Compensation amount when 1V is applied to ABL IN versus 8V applied to ABL IN)
3h = –7% (Compensation amount when 1V is applied to ABL IN versus 8V applied to ABL IN)

INTERLACE (1) : Interlace mode and non-interlace display selector switch
0,1h = Interlace mode
2h = Interlace mode; 1/2H shift applied to EVEN lines
3h = Interlace mode; 1/2H shift applied to ODD lines

PIN-PHASE (4) : Horizontal trapezoidal distortion compensation amount adjustment (V parabola wave center timing control)

0h = 1.5ms advance	Horizontal size for top of picture increases; horizontal size for bottom of picture decreases.
7h = 0ms	8.9ms from 4VDC VTIM
Fh = 1.5ms delay	Horizontal size for top of picture decreases; horizontal size for bottom of picture increases.

UP-CORNER-PIN (4) : Horizontal pin distortion compensation amount adjustment for top of picture (V parabola wave top gain control)

0h = –0.2V	Horizontal size for top of picture decreases. (compensation amount maximum)
7h = 0V	(0.7Vp-p 4:3 mode)
Fh = +0.2V	Horizontal size for top of picture increases. (compensation amount minimum)

LO-CORNER-PIN (4) : Horizontal pin distortion compensation amount adjustment for bottom of picture (V parabola wave bottom gain control)

0h = –0.2V	Horizontal size for bottom of picture decreases. (compensation amount maximum)
7h = 0V	(0.7Vp-p 4:3 mode)
Fh = +0.2V	Horizontal size for bottom of picture increases. (compensation amount minimum)

V-ASPECT (6) : Aspect ratio control. (Gain control for sawtooth wave)

0h = 75%	16:9 CRT full
2Fh = 100%	4:3 CRT full, amplitude: 1.23Vp-p
3Fh = 112%	

ZOOM SW (1) : Zoom mode ON/OFF switch for 16:9 CRT (25% of video cut)

0 = Zoom OFF	Sawtooth wave amplitude: 1.23Vp-p
1 = Zoom ON	Sawtooth wave amplitude: 70%

HBLKSW (1) : HBLK width control ON/OFF switch during 4:3 software full display mode on a 16:9 CRT

0 = Control OFF	HBLK pulse generated from HPIN.
1 = Control ON	HBLK pulse generated as pulse generated from HPIN or as pulse generated from HVCO and width adjusted. Width adjustment is performed by the LEFT-BLK and RIGHT-BLK registers.

V-SCROLL (6) : Vertical picture scroll control during zoom mode on a 16:9 CRT (DC component added to sawtooth wave AGC output to control ZOOMSW cut timing.)

0h = –0.2V	Scrolled toward top of screen by 32H and top of picture zoomed.
1Fh = 0V	
3Fh = +0.2V	Scrolled toward bottom of screen by 32H and bottom of picture zoomed.

JUMPSW	(1)	: Reference pulse jump mode ON/OFF switch (In addition to V-ASPECT control, sawtooth wave gain control performed for 100% of VBLK interval and 67% of picture interval) 0 = Jump mode OFF 1 = Jump mode ON On a 4:3 CRT, jump mode expands the sawtooth wave amplitude to 112% with V-ASPECT; on a 16:9 CRT, jump mode compresses the sawtooth wave amplitude to 75% with V-ASPECT. The V blanking width is expanded at both the top and bottom of the picture. Blanking for the bottom of the picture starts 251H after VTIM, and blanking for the top of the picture can be varied as the blanking width after the reference pulse from the VBLKW register.
HSIZESW	(1)	: Lowers the E-W OUT DC level (during H-SIZE compression) 0 = Normal 1 = –1.35V
UP-VLIN	(4)	: Vertical linearity adjustment for top of picture (Secondary component gain control for sawtooth wave added to sawtooth wave AGC output) 0h = 100% (Bottom/top of picture) Fh = 115% (Bottom/top of picture) Top of picture compressed.
LO-VLIN	(4)	: Vertical linearity adjustment for bottom of picture (Tertiary component gain control for sawtooth wave added to sawtooth wave AGC output) 0h = 100% (Bottom/top of picture) Fh = 85% (Bottom/top of picture) Bottom of picture compressed.
LEFT-BLK	(4)	: HBLK width control for the left side of picture when HBLKSW = 1 (Phase control for timing pulse generated from HVCO) 0h = +1.3µs HBLK width maximum 7h = 0µs Center HBLK: 13µs Fh = –1.3µs HBLK width minimum
RIGHT-BLK	(4)	: HBLK width control for the right side of picture when HBLKSW = 1 (Phase control for timing pulse generated from HVCO) 0h = +1.3µs HBLK width maximum 7h = 0µs Center HBLK: 13µs Fh = –1.3µs HBLK width minimum
SCP BGR	(2)	: Controls the phase of the rising edge of the burst pulse in sand castle pulse output (0.4µs/step) 0h = +0.4µs 1h = Center 3h = –0.8µs
SCP BGF	(2)	: Controls the phase of the falling edge of the burst pulse in sand castle pulse output (0.4µs/step) 0h = +0.4µs 1h = Center 3h = –0.8µs
CRT-TYP	(1)	: Corner Pin range for 16:9 or 4:3 CRT 0 = 16:9 Mode 1 = 4:3 Mode

6. Other

AGING (1) : White output aging mode ON/OFF switch
(Takes priority over RGB ON and PIC ON control. Set to OFF mode at power-on.)
0 = Aging mode OFF
1 = Aging mode ON (When there is no input signal, a 60 IRE flat signal is output from the Y block)

7. Status register

HLOCK (1) : Lock status between H SYNC and H VCO
0 = HVCO free run status
1 = Locked to H SYNC

IKR (1) : AKB operation status
0 = REF-P at Ik small and AKB loop unstable.
1 = REF-P at Ik sufficient and AKB loop stable.

VNG (1) : Signal input status to V PROT pin
0 = No V PROT input
1 = V PROT input (In this case, the RGB output is blanked.)

XRAY (1) : Signal input status to XRAY control pin (HOFF pin)
0 = No XRAY control input
1 = XRAY control input (In this case, the RGB output is blanked.)

COLOR SYS (3) : Color system status
0h = —
1h = —
2h = NO STANDARD
3h = SECAM
4h = 3.58MHz NTSC
5h = 4.43MHz NTSC
6h = 3.58MHz PAL
7h = 4.43MHz PAL

FV (1) : Vertical frequency status register
0 = 50Hz
1 = 60Hz

Description of Operation

1. Power-on sequence

The CXA2076Q does not have an internal power-on sequence. Therefore, power-on sequence is all controlled by the set microcomputer (I^2C bus controller).

1) Power-on

The IC is reset and the RGB outputs are all blanked. Hdrive starts to oscillate, but oscillation is at the maximum frequency (16kHz or more) and is not synchronized to the input signal. Output of vertical signal VTIM starts, but Vdrive is DC output. Bus registers which are set by power-on reset are as follows.

AGING	= 0: All white output aging mode OFF
RON	= 0: Rch video blanking ON
GON	= 0: Gch video blanking ON
BON	= 0: Bch video blanking ON
PICON	= 0: RGB all blanking ON
VOFF	= 1: VDRIVE output stopped mode
VFREQ	= 0: Automatic identification mode (identification starts at 50Hz)
FHHI	= 1: H oscillator maximum frequency mode
HSIZESW	= 0: Normal
CD-MODE	= 0: Automatic selection mode of the countdown mode
AKBOFF	= 0: AKB mode

2) Bus register data transfer

The register setting sequence differs according to the set sequence. Register settings for the following sequence are shown as an example.

Set sequence	CXA2076Q register settings
Power-on	Reset status in 1) above.
↓	↓
Degauss	Reset status in 1) above. The CRT is degaussed in the completely darkened condition.
↓	↓
VDRIVE oscillation	The IC is set to the power-on initial settings. (See the following page.) A sawtooth wave is output to VDRIVE and the IC waits for the vertical deflection to stabilize. The HDRIVE oscillator frequency goes to the standard frequency.
↓	↓
AKB operation start	PICON is set to 1 and a reference pulse is output from Rout, Gout and Bout. Then, the IC waits for the cathode to warm up and the beam current to start flowing.
↓	↓
AKB loop stable	Status register IKR is monitored. IKR = 0: No cathode current IKR = 1: Cathode current Note that the time until IKR returns to 1 differs according to the initial status of the cathode.
↓	↓
Video output	RON, GON and BON are set to 1 and the video signal is output from Rout, Gout and Bout.

I²C bus power-on initial settings

The initial settings listed here for power-on when VDRIVE starts to oscillate are reference values; the actual settings may be determined as needed according to the conditions under which the set is to be used.

Register Table

"*" Undefined

Control Register

Sub Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
××× 0 0 0 0 0 00 h	1	1	1	1	1	1	0	0
××× 0 0 0 0 1 01 h	0	1	1	1	1	1	0	1
××× 0 0 0 1 0 02 h	0	1	1	1	1	1	0	*
××× 0 0 0 1 1 03 h	0	1	1	1	1	1	1	*
××× 0 0 1 0 0 04 h	0	1	1	1	0	0	0	0
××× 0 0 1 0 1 05 h	0	1	1	1	0	1	1	1
××× 0 0 1 1 0 06 h	0	1	1	1	0	1	1	1
××× 0 0 1 1 1 07 h	0	1	1	1	1	1	0	0
××× 0 1 0 0 0 08 h	0	1	1	1	1	1	0	0
××× 0 1 0 0 1 09 h	0	1	1	1	1	1	0	0
××× 0 1 0 1 0 0A h	0	1	1	1	0	1	1	1
××× 0 1 0 1 1 0B h	0	0	0	0	0	0	0	0
××× 0 1 1 0 0 0C h	0	1	1	1	1	1	0	0
××× 0 1 1 0 1 0D h	0	1	1	1	1	1	1	0
××× 0 1 1 1 0 0E h	0	1	1	1	0	1	1	1
××× 0 1 1 1 1 0F h	0	1	1	1	1	1	0	0
××× 1 0 0 0 0 10 h	0	1	1	1	1	1	0	0
××× 1 0 0 0 1 11 h	0	1	1	1	0	1	1	1
××× 1 0 0 1 0 12 h	0	1	1	1	0	1	1	1
××× 1 0 0 1 1 13 h	0	1	0	1	0	0	0	0
××× 1 0 1 0 0 14 h	0	0	0	0	0	0	1	1
××× 1 0 1 0 1 15 h	0	1	1	1	1	1	0	0
××× 1 0 1 1 0 16 h	0	1	1	1	0	1	1	1
××× 1 0 1 1 1 17 h	0	1	1	1	1	1	1	1
××× 1 1 0 0 0 18 h	0	0	1	1	0	1	1	1
××× 1 1 0 0 1 19 h	*	*	0	0	0	0	1	1

3) Power-on initial settings

The initial settings listed here for power-on when VDRIVE starts to oscillate are reference values; the actual settings may be determined as needed according to the conditions under which the set is to be used.

PICTURE	= 3Fh	Max (User Control)
TRAP OFF	= 0	Chroma Trap ON
VM OFF	= 0	VM out ON
HUE	= 1Fh	Center (User Control)
DC-TRAN	= 0	Y DC transmission ratio 100%
D-PIC	= 1	Y black expansion ON
COLOR	= 1Fh	Center (User Control)
TOT	= 0	Chroma low frequency increased
BRIGHT	= 1Fh	Center (User Control)
D-COL	= 1	Dynamic Color ON
SHARPNESS	= 7h	Center (User Control)
PRE-OVER	= 0	Sharpness pre/over ratio 1:1
COLOR SW	= 0	AUTO
SUB-CONT	= 7h	Center (Adjust)
TRAP F0	= 7h	Center (Adjust)
SUB-COLOR	= 7h	Center (Adjust)
UP-CORNER-PIN	= 7h	Center (Adjust)
SUB-BRIGHT	= 1Fh	Center (Adjust)
GAMMA	= 0	Gamma OFF
G-DRIVE	= 1Fh	Center (Adjust)
AGING	= 0	Aging Mode OFF
B-DRIVE	= 1Fh	Center (Adjust)
INTERLACE	= 0	INTERLACE mode
G-CUTOFF	= 7h	Center (Adjust)
B-CUTOFF	= 7h	Center (Adjust)
RON	= 0	Rch video output OFF
GON	= 0	Gch video output OFF
BON	= 0	Bch video output OFF
PICON	= 0	RGB all blanked
VOFF	= 0	Vdrive oscillation
FHHI	= 0	Horizontal oscillator frequency standard
CD-MODE	= 0	V countdown auto mode
AKBOFF	= 0	AKB ON
V-SIZE	= 1Fh	Center (Adjust)
V-FREQ	= 0	AUTO
V-POSITION	= 1Fh	Center (Adjust)
AFC-MODE	= 2	Center
S-CORR	= 7h	Center (Adjust)
V-LIN	= 7h	Center (Adjust)
H-SIZE	= 1Fh	Center (Adjust)
REF-POSI	= 0	
PIN-COMP	= 1Fh	Center (Adjust)
VBLKW	= 0	

(Power-on initial settings cont.)

H-POSITION	= 7h	Center (Adjust)
PIN-PHASE	= 7h	Center (Adjust)
AFC-BOW	= 7h	Center (Adjust)
AFC-ANGLE	= 7h	Center (Adjust)
SCP BGR	= 1	Center
SCP BGF	= 1	Center
XTAL	= 0	AUTO
EXT SYNC	= 0	Internal SYNC
CV/YC	= 0	CV input
V-ASPECT	= 0h	16:9 CRT Full Mode
ZOOMSW	= 1	16:9 CRT
HBLKSW	= 1	Hblk width adjust ON
V-SCROLL	= 1Fh	Center (User Control)
JMPSW	= 0	16:9 CRT Full Mode
HSIZE SW	= 0	Normal
UP-VLIN	= 7h	16:9 CRT Full Mode
LO-VLIN	= 7h	16:9 CRT Full Mode
LEFT-BLK	= Fh	Hblk width Min.
RIGHT-BLK	= Fh	Hblk width Min.
EHT-H	= 0	Hdrive high-voltage compensation OFF
EHT-V	= 3	Vdrive high-voltage compensation amount maximum
LO-CORNER-PIN	= 7h	Center (Adjust)
KIL-OFF	= 0	Normal
CRT-TYP	= 0	16:9 Mode
YS1 OFF	= 0	Normal
DL	= 3	Normal (Adjust)

2. Various mode settings

The CXA2076Q contains bus registers for deflection compensation which can be set for various wide modes. Wide mode setting registers can be used separately from registers for normal picture distortion adjustment, and once deflection adjustment has been performed in full mode, wide mode settings can be made simply by changing the corresponding register data.

- VDRIVE signal picture distortion adjustment registers
  V-SIZE, V-POSITION, S-CORR, V-LIN
- E/WDRIVE signal picture distortion adjustment registers
  H-SIZE, PIN-COMP, PIN-PHASE, UP-CORNER-PIN, LO-CORNER-PIN
- Wide mode setting registers
  V-ASPECT, ZOOMSW, HBLKSW, V-SCROLL, JMPSW, HSIZESW, UP-VLIN, LO-VLIN, LEFT-BLK, RIGHT-BLK

Examples of various modes are listed below. These modes are described using 570 (NTSC: 480) lines as the essential number of display scanning lines. Wide mode setting register data is also listed, but settings may differ slightly due to IC variation. The standard setting data differs for 16:9 CRTs and 4:3 CRTs.

Register	16:9 CRT	4:3 CRT
V-ASPECT	0h	2Fh
V-SCROLL	1Fh	1Fh
ZOOMSW	1	0
UP-VLIN	0h	0h
LO-VLIN	0h	0h
JMPSW	0	0
HSIZESW	0	0
HBLKSW	0	0
LEFT-BLK	7h	7
RIGHT-BLK	7h	7h

1) 16:9 CRT full mode

This mode reproduces the full 570 (NTSC:480) lines on a 16:9 CRT. 4:3 images are reproduced by stretching the picture to the left and right.

Normal images are compressed vertically, but 16:9 images can be reproduced in their original 16:9 aspect ratio with a video source which compresses (squeezes) 16:9 images to 4:3 images. The register settings are the 16:9 CRT standard values.

2) 16:9 CRT normal mode

In this mode, 4:3 images are reproduced without modification. A black border appears at the left and right of the picture. In this mode, the H deflection size must be compressed by 25% compared to full mode. The CXA2076Q permits compression with a register (HSIZESW) that compresses the H size by 25%. Because excessive current flows to the horizontal deflection coil in this case, adequate consideration must be given to the allowable power dissipation, etc., of the horizontal deflection coil in the design of the set. In addition, this concern can also be addressed through measures taken external to the IC, such as by switching the horizontal deflection coil. Full mode should be used when using memory processing to add a black border to the video signal.

H blanking of the image normally uses the flyback pulse input to AFCPIN (Pin 38). However, the blanking width can be varied according to the control register setting when blanking is insufficient for the right and left black borders.

The following three settings are added to the 16:9 CRT standard values for the register settings.

HBLKSW = 1
LEFT-BLK = Adjustment value
RIGHT-BLK = Adjustment value

The H angle of deflection also decreases, causing it to differ from the PIN compensation amount during H size full status. Therefore, in addition to the wide mode registers, PIN-COMP must also be readjusted only for this mode.

3) 16:9 CRT zoom mode

In this mode, 4:3 images are reproduced by enlarging the picture without other modification. The top and bottom of normal 4:3 images are lost, but almost the entire picture can be reproduced for vista size video software, etc. which already has black borders at the top and bottom. The enlargement ratio can be controlled by the V-ASPECT register, and enlarging the picture by 33% compared to full mode allows zooming to be performed for 4:3 images without distortion. In this case, the number of scanning lines is reduced to 430 lines compared to 570 lines for full mode. The zooming position can be shifted vertically by the V-SCROLL register.

V blanking of the image normally begins from V sync and continues for 2H after the AKB reference pulse, and the top and bottom parts are also blanked during this mode.

Adjust the following two registers with respect to the 16:9 CRT standard values for the register settings.

V-ASPECT = 2Fh
V-SCROLL = 1Fh or user control

4) 16:9 CRT subtitle-in mode

When CinemaScope size images which have black borders at the top and bottom of the picture are merely enlarged with the zoom mode in 3) above, subtitles present in the black borders may be lost. Therefore, this mode is used to super-compress only the subtitle part and reproduce it on the display.

Add the LO-VLIN adjustment to the zoom mode settings for the register settings.

V-ASPECT = 2Fh
V-SCROLL = 1Fh or user control
LO-VLIN = Adjustment value

The LO-VLIN register causes only the linearity at the bottom of the picture to deteriorate. Therefore, UP-VLIN should also be adjusted if the top and bottom of the picture are to be made symmetrical. Since the picture is compressed vertically, the number of scanning lines exceeds 430 lines.

5) 16:9 CRT V compression mode

This mode is used to reproduce two 4:3 video displays such as for PandP. The V size must be compressed to 67% in order to reproduce two displays on a 16:9 CRT without distortion using 480 scanning lines, and this can be set by JMPSW. Compression is performed after the AKB reference pulse, so the reference pulse remains in the overscan position. The V blanking width after the reference pulse becomes larger than normal and can be varied by the VBLKW register. During this mode, the bottom V blanking width is also expanded to 3H wider than normal so that the bottom of the picture is not overscanned.

16:9 CRT standard values are used with only the JMPSW setting changed for the register settings.

JMPSW = 1

6) 16:9 CRT wide zoom mode

This mode reproduces 4:3 video software naturally on wide displays by enlarging 4:3 images without other modification and compressing the parts of the image which protrude from the picture into the top and bottom parts of the picture. The display enlargement ratio is controlled by V-ASPECT, and the compression ratios at the top and bottom of the picture are controlled by UP-VLIN and LO-VLIN.

Adjust the following three registers with respect to the 16:9 CRT standard values for the register settings.

V-ASPECT = Adjustment value
UP-VLIN = Adjustment value
LO-VLIN = Adjustment value

7) 4:3 CRT normal mode

This is the standard mode for 4:3 CRTs.

The register settings are the 4:3 CRT standard values.

8) 4:3 CRT V compression mode

This mode is used to reproduce M-N converter output consisting of 16:9 images expanded to a 4:3 aspect ratio and other squeezed signals without distortion on a 4:3 CRT. The V size must be compressed to 75% in order to reproduce a 4:3 squeezed signal at a 16:9 aspect ratio without any distortion. Compressing the V size with the JMPSW register used in mode 5) above, compresses the V size to 67%. Therefore, V-ASPECT is set to enlarge the V size by 8%. AKB reference pulse handling and V blanking are the same as for mode 5) above.

4:3 CRT standard values are used with the V-ASPECT and JMPSW settings changed for the register settings.

V-ASPECT = 3Fh
JMPSW = 1

Mode Settings

Setting	CRT SIZE	SOFT SIZE	MODE NAME	I²C BUS REGISTER
1)-1	16:9	16:9	16:9 CRT full	V-ASPECT = 0h: V size 75%
1)-2	16:9	4:3	Wide full	V-ASPECT = 0h: V size 75%
2)	16:9	4:3	16:9 CRT normal	V-ASPECT = 0h: V size 75% HBLKSW = 1h: HBLK width adjustment ON LEFT-BLK = Adjustable RIGHT-BLK = Adjustable PIN-COMP = Adjustable (External support: H-DY H amplitude 75%)
3)	16:9	4:3	16:9 CRT zoom	V-ASPECT = 2Fh: V size 100% ZOOMSW = 1h: Zoom ON V size limited at 75% V-SCROLL = 0h: Zoom bottom of video image 1Fh: Zoom center of video image 3Fh: Zoom top of video image Adjustable: Open to user
4)	16:9	4:3 (16:9 + subtitle area)	16:9 CRT with subtitle area on	V-ASPECT = 2Fh: V size 100% UP-VLIN = Adjustable: Slightly compresses top of video image LO-VLIN = Adjustable: Significantly compresses bottom of video image ZOOMSW 1h: V size limited at 75% (V-SCROLL = Adjustable)
5)	16:9	4:3	16:9 CRT V compression	V-ASPECT = 0h: V size 75% JMPSW = 1h: Reference pulse skipping ON V size compressed 67% after the reference pulse (compressed to 50% total) VBLKW = Adjustable: VBLK width expanded at top and bottom of video image
6)	16:9	4:3	16:9 CRT wide zoom	V-ASPECT = Adjustable: V size 90% UP-VLIN = Adjustable: LO-VLIN = Adjustable: (S-CORR = Adjustable): Compression of top and bottom of video image
7)	4:3	4:3	4:3 CRT normal	V-ASPECT = 2Fh: V size 100%
8)	4:3	16:9	4:3 CRT V compression	V-ASPECT = 3Fh: V size 112% JMPSW = 1h: Reference pulse skipping ON (compressed to 75% total) VBLKW = Adjustable: VBLK width expanded at top and bottom of video image

* The amount of picture distortion compensation in a vertical direction position of the CRT does not change in response to the above modes; as a result, the initial values of each picture distortion register can be used as is.

3. Signal processing

The CXA2076Q is comprised of sync signal processing, H deflection signal processing, V deflection signal processing, and Y/C/RGB signal processing blocks, all of which are controlled by the I^2C bus.

1) Sync signal processing

Pin 48 (SYNC OUT) outputs at 2Vp-p either the internal signal (CVIN/YIN) selected by the internal video switch, or the external sync signal input from Pin 56 (EXT SYNC IN).
This selection is controlled by the I^2C bus. The signal output from Pin 48 is buffered by a PNP Tr. and is then input to HSIN (Pin 47) or VSIN (Pin 46) through a suitable filter.
The Y signals input to Pins 46 and 47 are sync separated by the horizontal and vertical sync separation circuits. The resulting horizontal sync signal and the signal (FH = 15625Hz or 15734Hz) obtained by frequency dividing the 32FH-VCO output using the ceramic oscillator (frequency 500kHz or 503.5kHz) by 32 are phase-compared, the AFC loop is constructed, and an H pulse synchronized with the H sync is generated inside the IC. Adjustment of the H oscillator frequency is unnecessary. When the AFC is locked to the H sync, 1 is output to the status register (HLOCK) and that can be used to detect the presence of the video signal.
The vertical sync signal is sent to the V countdown block where the most appropriate window processing is performed to obtain V sync timing information which resets the counter. AKB and other V cycle timing are then generated from this reset timing.

2) H deflection signal processing

The H pulse obtained through sync processing is phase-compared with the H deflection pulse input from Pin 38 to control the phase of the HDRIVE output and the horizontal position of the image projected on the CRT. In addition, the compensation signal generated from the V sawtooth wave is superimposed, and the vertical picture distortion is compensated.
The H deflection pulse is used for H blanking of the video signal. When the pulse input from Pin 38 has a narrow width, the pulse generated by the IC can be added to the H deflection pulse and used as the H blanking pulse (HBLKSW).
Pin 38 is normally pulse input, but if the pin voltage drops to the GND level, HDRIVE output stops and 1 is output to the status register (XRAY). To release this status, turn the power off and then on again.

3) V deflection signal processing

The V sawtooth wave is generated at the cycle of the reset pulse output from the countdown system. After performing wide deflection processing for this sawtooth wave, picture distortion adjustment is performed by the VDRIVE and E/WDRIVE function circuits and the signal is output as the VDRIVE and E/WDRIVE signals.

4) Y signal processing

Either CVIN, input from Pin 53, or YIN, output from Pin 55, is selected by the video switch and then is passed to the Y signal processing circuit as the Y signal. The input level is 1Vp-p.
The Y signal passes through the subcontrast control, the trap for eliminating the chroma signal, the delay line, the sharpness control, the clamp and the black expansion circuits, and is then output to Pin 5 as YOUT. The differentiated waveform of the Y signal, advanced for about 200ns from YOUT is output from Pin 49 as the VM signal. The delay time is set by the bus register (DL).
When CVIN is selected, the trap is on; when YIN is selected, the trap is off.
The f0 of the internal filter is automatically adjusted within the IC. Because the f0 of the filter is not specified when the color killer function is operating, turn the trap off if there are any difficulties. In addition, the f0 of the trap will be affected slightly by variations among IC, so fine adjustment through the I^2C bus (TRAP-F0) may be required.

5) C signal processing

The CVBS signal or chroma signal (specified input level: burst level of 300mVp-p) selected by the video switch passes through the ACC, TOT, chroma amplifier and demodulation circuits, becomes the R-Y and B-Y color difference signals, and is inverted for output on Pins 3 and 4. The color difference signals are averaged together by the external 1H delay line, and are input to Pins 7 and 8. Both color difference signals are clamped together with the Y signal input to Pin 5. They are then combined with the G-Y signal in the color control and axis control circuits. After Y/C mixing, the signals become the RGB signals.

If the burst level goes to –35dB or less with respect to the specified input level, the color killer operates.

In addition, the color system (PAL/NTSC) and the subcarrier frequency (4.43MHz/3.58MHz) are automatically identified according to the input chroma signal, and the internal VCO, demodulation circuit, axis control circuit, etc., are adjusted automatically.

Furthermore, SECAM signals can also be identified if an external SECAM decoder is connected to Pin 1. In this case, Pins 3 and 4 and the SECAM decoder color difference output are linked together directly, and automatically one side goes to high impedance, the other goes to low impedance according to the input chroma signal, and then they are input to the external 1H delay line.

System identification can be set to automatic or forced mode by the I^2C bus (XTAL and COLOR SW). The color system is output to the status register (COLOR SYS).

6) RGB Signal processing

The RGB signals obtained from the Y/C block pass through the half-tone switch circuit (YM SW), the two switch circuits for the external RGB signals (YS1, YS2 SW), the picture control, dynamic color, gamma compensation, clamp, brightness control, drive adjustment, cut-off adjustment and auto cut-off circuits, and are output to Pins 22, 24 and 26.

The RGB signals input to Pins 12, 13, 14, 17, 18, and 19 are 100 IRE, 100% white 0.7Vp-p signals, in accordance with the standard for normal video signals. If signals of 1.5Vp-p or more are input to Pins 17, 18, and 19, 67 IRE output is obtained (digital input).

The voltage applied to Pin 28 (ABLIN) is compared with the internal reference voltage, integrated by the capacitor which is connected to Pin 29, and performs picture control and brightness control.

In order to adjust the white balance (black balance), this IC has a drive control function which adjusts the gain between the RGB outputs and a cut-off control function which adjusts the DC level between the RGB outputs. Both drive control and cut-off control are adjusted by the I^2C bus, with the Rch fixed and the G and Bch variable. An auto cut-off function (AKB) which forms a loop between the IC and CRT and performs adjustment automatically has also been added. This function can compensate for changes in the CRT with time. Auto cut-off operation is as follows.

- R, G and B reference pulses for auto cut-off, shifted 1H each in the order mentioned, appear at the top of the picture (actually, in the overscan portion). The reference pulse uses 1H in the V blanking interval, and is output from each R, G and B output pin.
- The cathode current (Ik) of each R, G and B output is converted to a voltage and input to Pin 27.
- The voltage input to Pin 27 is compared with the reference voltage in the IC, and the current generated by the resulting error voltage charges the capacitors connected to Pins 21, 23 and 25 for the reference pulse interval and is held during all other interval.
- The loop functions to change the DC level of the R, G and B outputs in accordance with the capacitor pin voltage so that the Pin 27 voltage matches the reference voltage in the IC.

The Rch for the reference voltage in the IC is fixed and the G and Bch are cut-off controlled by the I^2C bus. During G/B-CUTOFF center status, the loop functions so that the Rch for the reference pulse input to Pin 27 is 1Vp-p and the G and Bch are 0.81Vp-p.

The reference pulse timing can be varied by the I^2C bus.

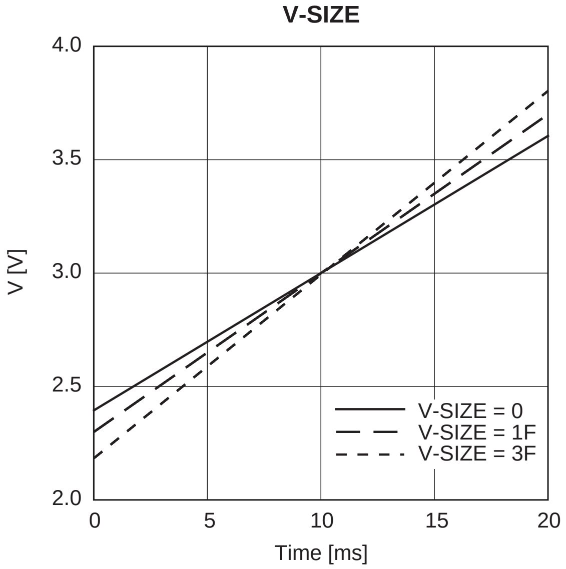
When AKB is not used, the IC can be set to manual cut-off mode with I^2C bus settings. In this case, the DC level of the R, G and B outputs can be varied by applying voltages independently to Pins 21, 23 and 25.

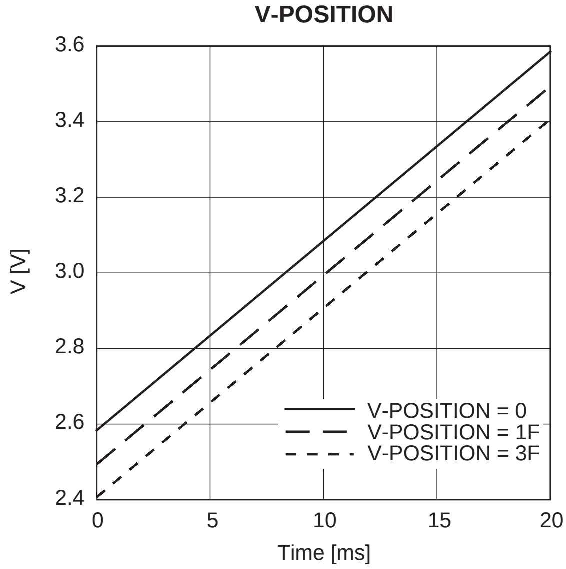
4. Notes on operation

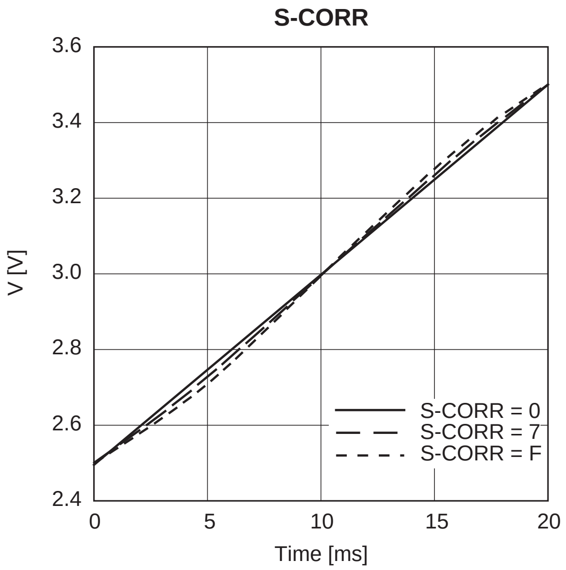
Because the RGB signals and deflection signals output from the CXA2076Q are DC direct connected, the board pattern must be designed consideration given to minimizing interference from around the power supply and GND.
Do not separate the GND patterns for each pin; a solid earth is ideal. Locate the power supply side of the by-pass capacitor which is inserted between the power supply and GND as near to the pin as possible. Also, locate the XTAL oscillator, ceramic oscillator and IREF resistor as near to the pin as possible, and do not wire signal lines near this pin. Drive the Y, external Y/color difference and external RGB signals at a sufficiently low impedance, as these signals are clamped when they are input using the capacitor connected to the input pin.
DC bias is applied to the chroma signal within the IC. Input the chroma signal with low impedance via an external capacitor.
Use a resistor (such as a metal film resistor) with an error of less than 1% for the IREF pin.
Use a capacitor, such as an MPS (metalized polyester capacitor) with a small tan δ for SAWOSC.
When using a line frequency FH of 15625Hz for the main clock (PAL-B, G, etc.), Murata's Ceralock CSB500F63 is recommended. This will yield a free-run frequency in the neighborhood of 15625Hz.

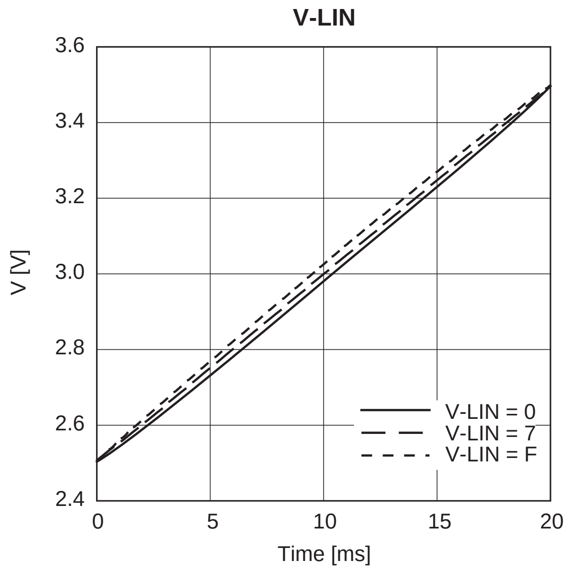
Curve Data

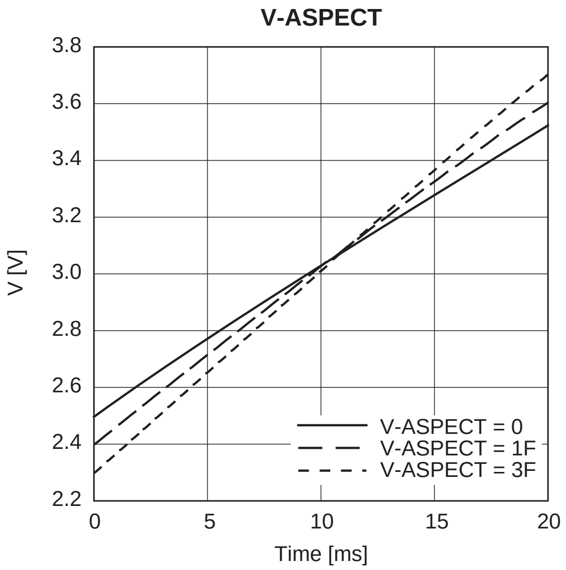
I^2C bus data conforms to the "I^2C Bus Register Initial Settings" of the Electrical Characteristics Measurement Conditions (P. 22).

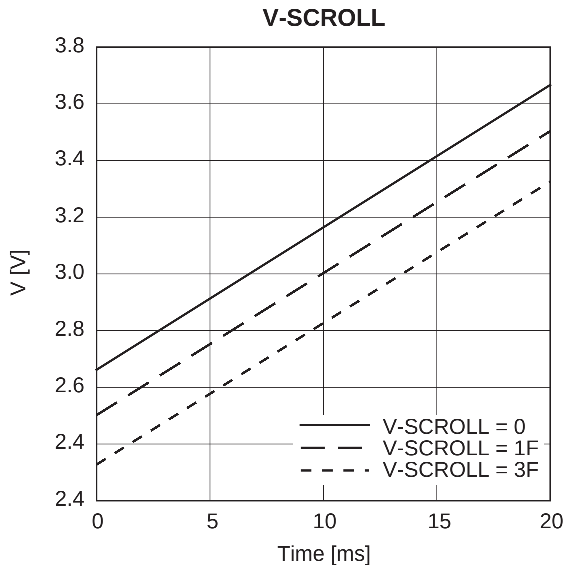




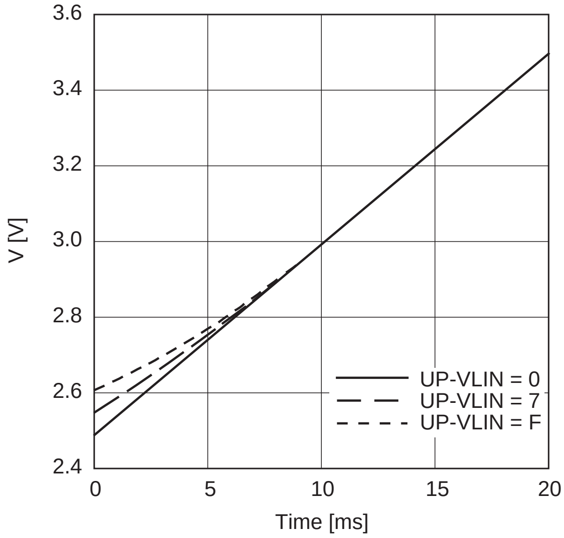




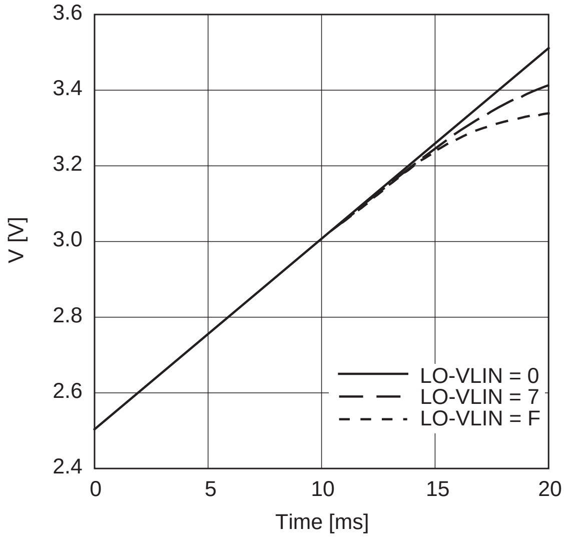




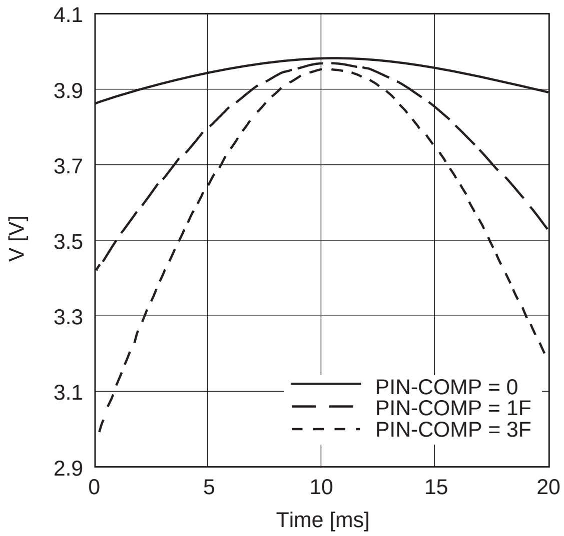
UP-VLIN



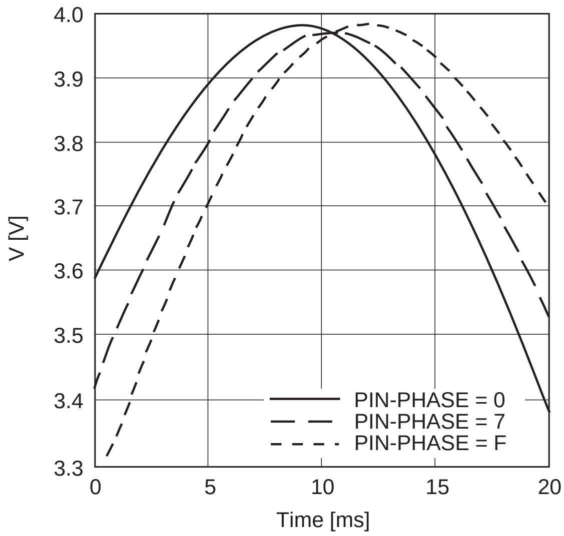
LO-VLIN



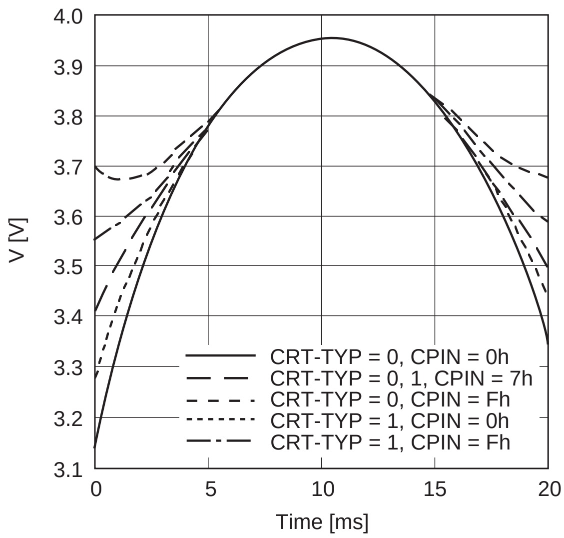
PIN-COMP



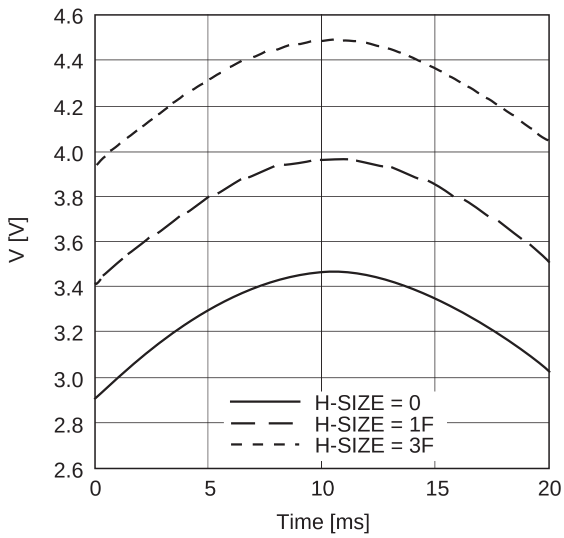
PIN-PHASE

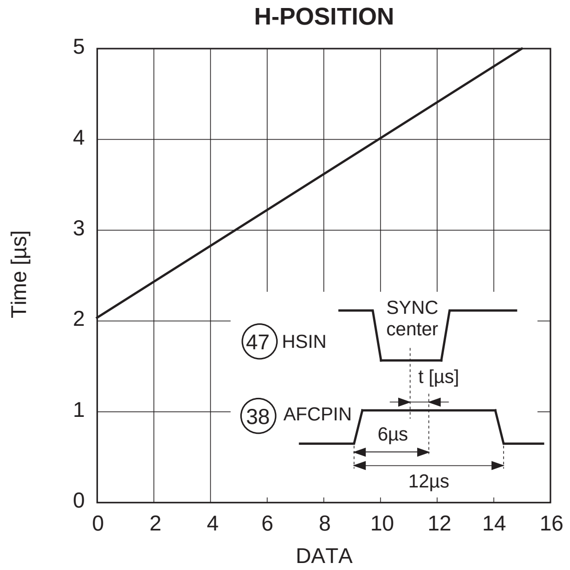


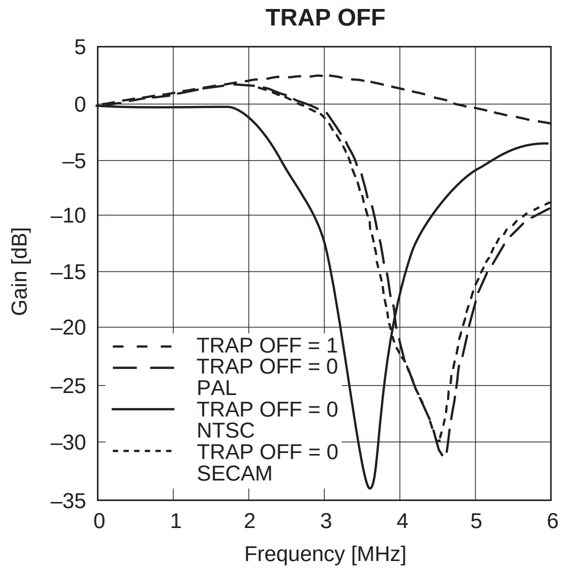
CORNER-PIN

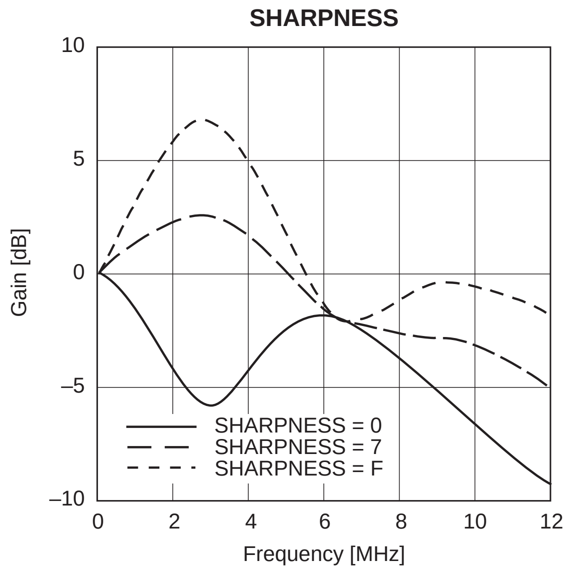


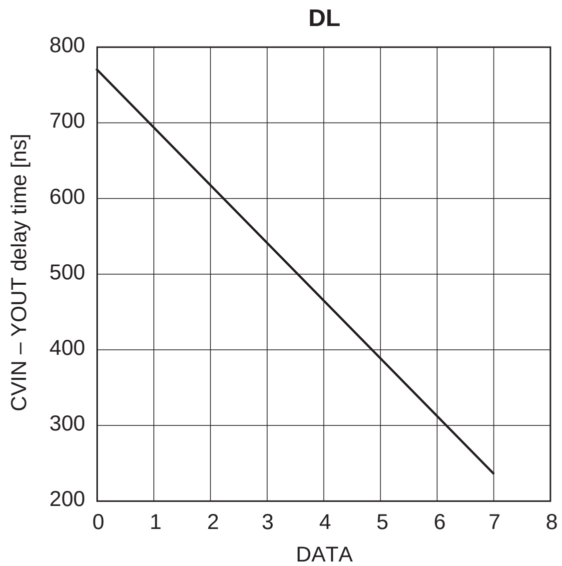
H-SIZE

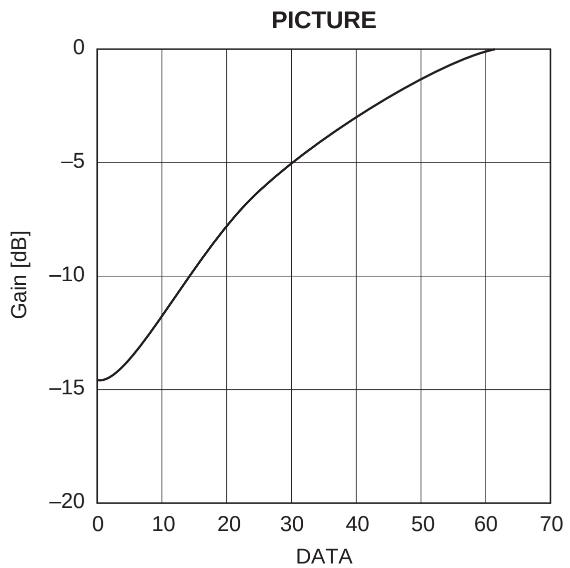


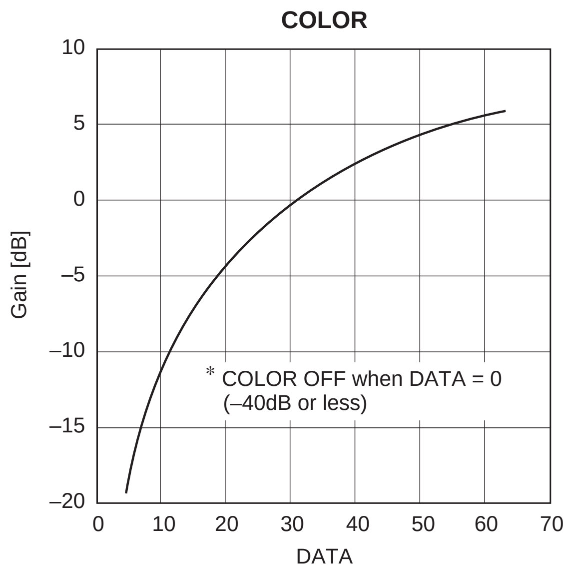

H-POSITION
Time [µs]
DATA
47 HSIN
SYNC center
t [µs]
38 AFCPIN
6µs
12µs

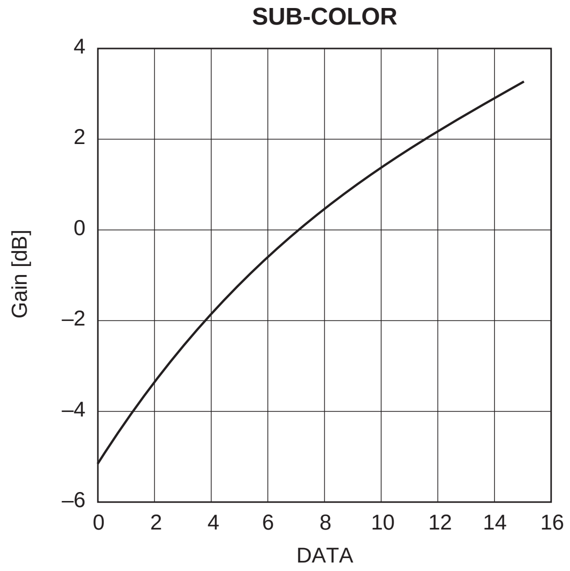

TRAP OFF
Gain [dB]
Frequency [MHz]
TRAP OFF = 1
TRAP OFF = 0 PAL
TRAP OFF = 0 NTSC
TRAP OFF = 0 SECAM

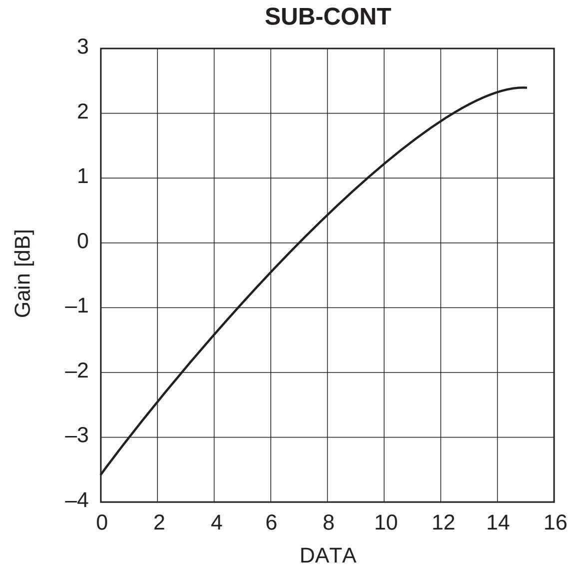

SHARPNESS
Gain [dB]
Frequency [MHz]
SHARPNESS = 0
SHARPNESS = 7
SHARPNESS = F

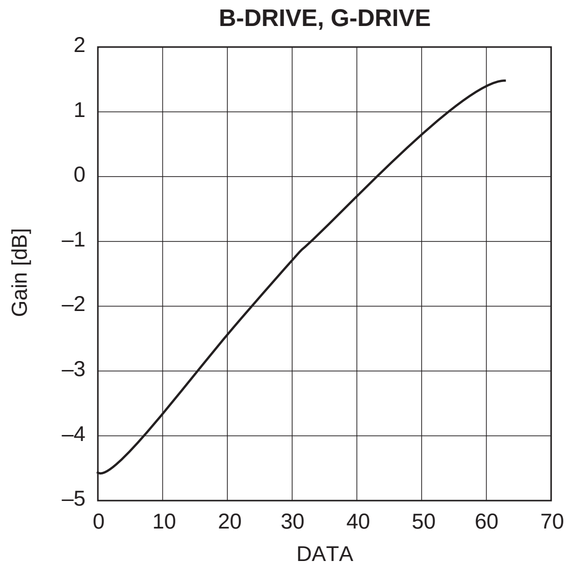

DL
CVIN – YOUT delay time [ns]
DATA

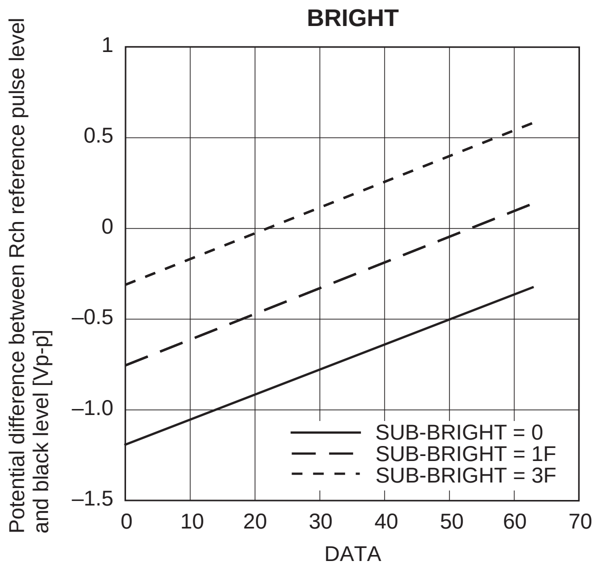

PICTURE
Gain [dB]
DATA

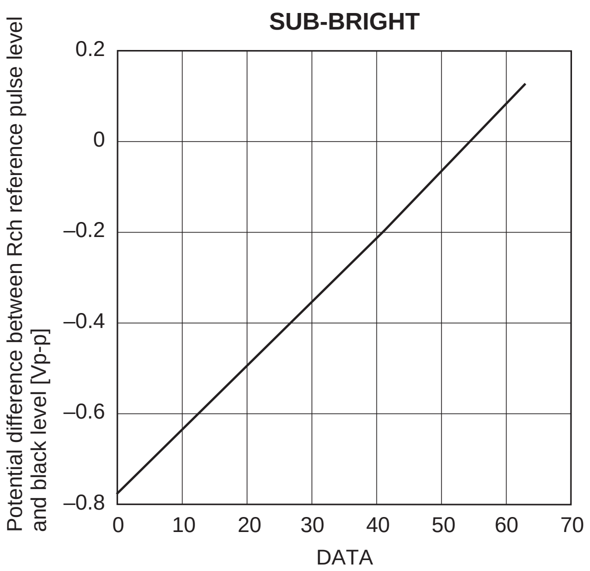

COLOR
Gain [dB]
DATA
* COLOR OFF when DATA = 0
(–40dB or less)

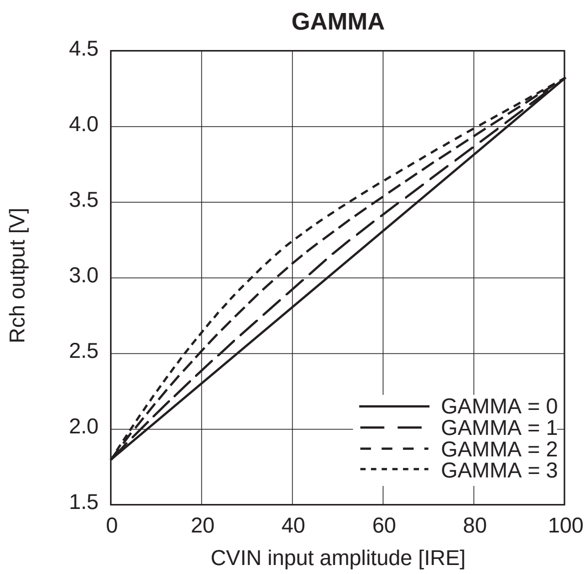

SUB-COLOR
Gain [dB]
4
2
0
–2
–4
–6
0 2 4 6 8 10 12 14 16
DATA


SUB-CONT
Gain [dB]
3
2
1
0
–1
–2
–3
–4
0 2 4 6 8 10 12 14 16
DATA

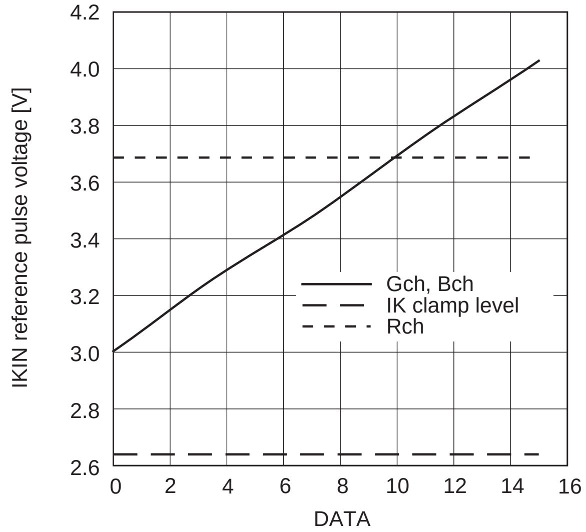

B-DRIVE, G-DRIVE
Gain [dB]
2
1
0
–1
–2
–3
–4
–5
0 10 20 30 40 50 60 70
DATA


BRIGHT
Potential difference between Rch reference pulse level and black level [Vp-p]
1
0.5
0
–0.5
–1.0
–1.5
0 10 20 30 40 50 60 70
DATA
SUB-BRIGHT = 0
SUB-BRIGHT = 1F
SUB-BRIGHT = 3F

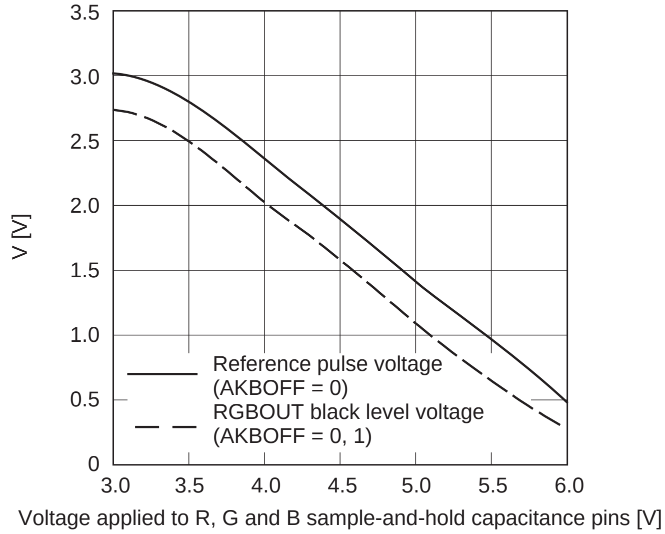

SUB-BRIGHT
Potential difference between Rch reference pulse level and black level [Vp-p]
0.2
0
–0.2
–0.4
–0.6
–0.8
0 10 20 30 40 50 60 70
DATA


GAMMA
Rch output [V]
4.5
4.0
3.5
3.0
2.5
2.0
1.5
0 20 40 60 80 100
CVIN input amplitude [IRE]
GAMMA = 0
GAMMA = 1
GAMMA = 2
GAMMA = 3

G-CUTOFF, B-CUTOFF

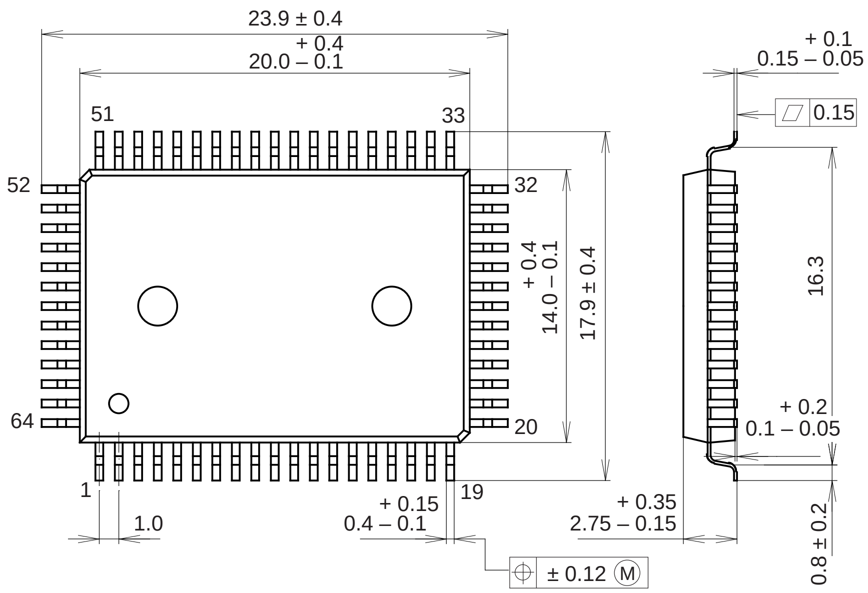


AKB open loop characteristics



Package Outline Unit: mm

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	∗QFP064-P-1420-A
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.5g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).