SONY

CXA2040AQ

I²C Bus-Compatible Video Switch

Description

The CXA2040AQ is an I²C bus-compatible 5-input, 3-output video switch for TVs.

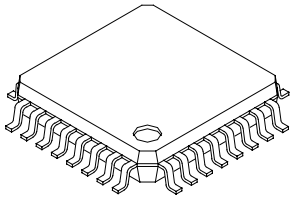
Features

- Serial data control via I²C bus
- 5 composite video input systems
- 2 Y/C (S terminal) input systems
- 3 composite video output systems
- 1 Y/C (S terminal) output system
- Input can be selected independently for each output system.
- SYNC_ID function for CV1 system input
- Built-in 6dB amplifier for CVOUT2 system output
- Built-in Y/C MIX circuit
- Slave address can be changed (90H/92H).
- High impedance maintained by I²C bus line (SDA, SCL) even when power is OFF.

Applications

TVs

32 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.0	W

(when mounted on a 50mm × 50mm board)

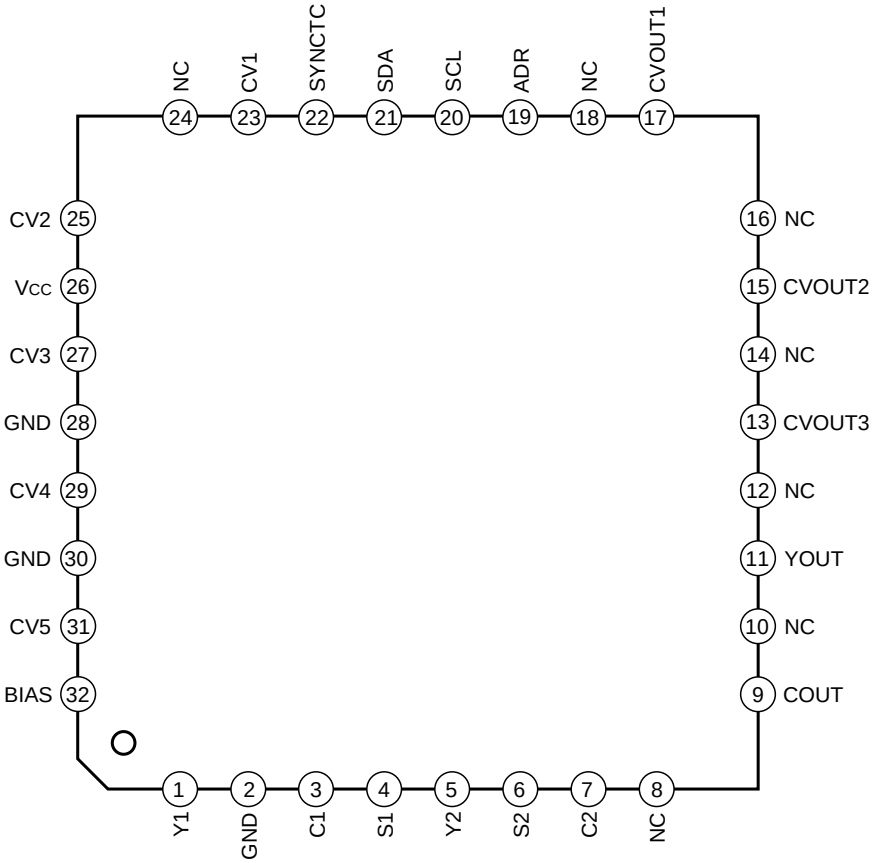
Operating Conditions

Supply voltage	V_{CC}	9.0 ± 0.5	V

Structure

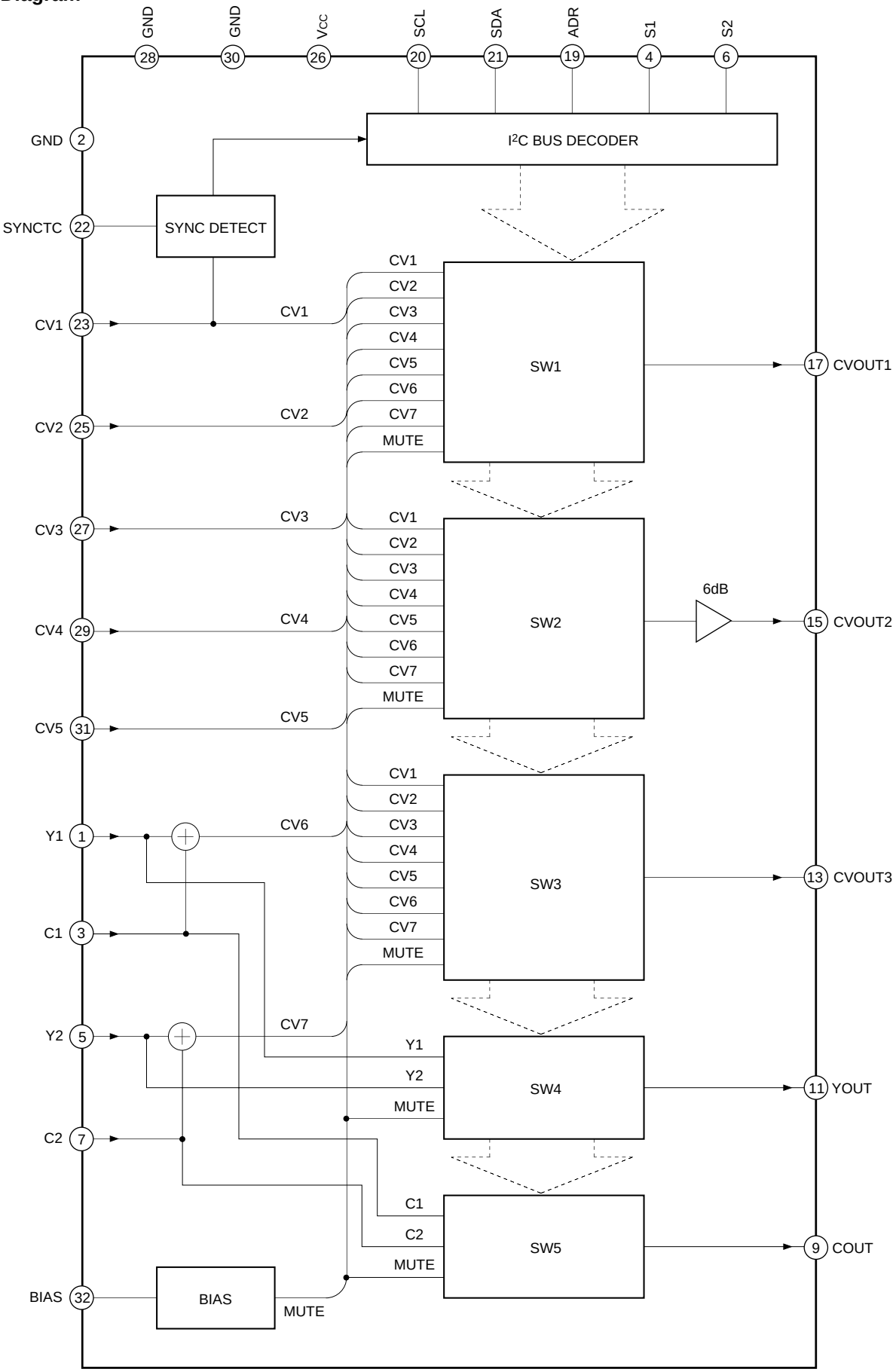
Bipolar silicon monolithic IC

Pin Configuration (Top View)



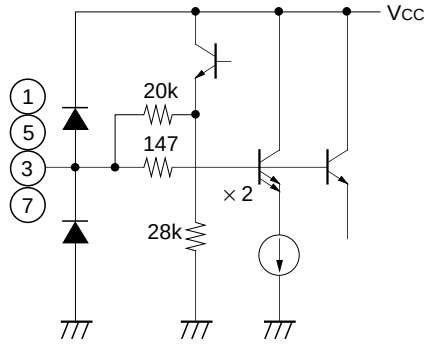
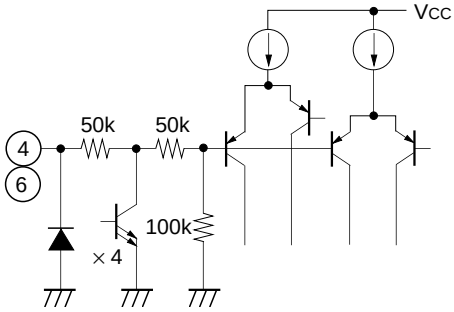
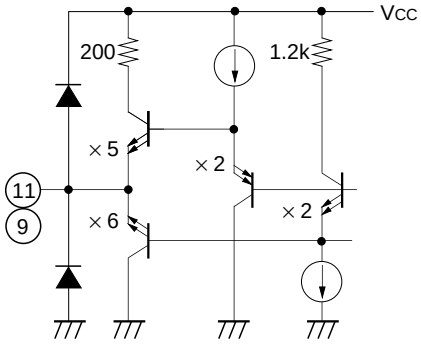
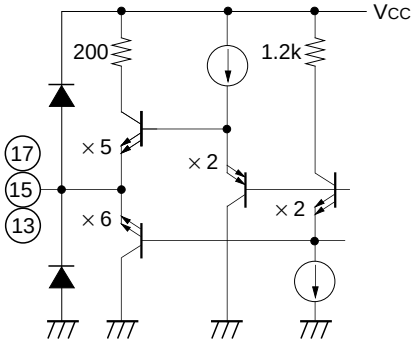
E96Z28A26

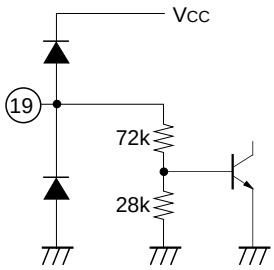
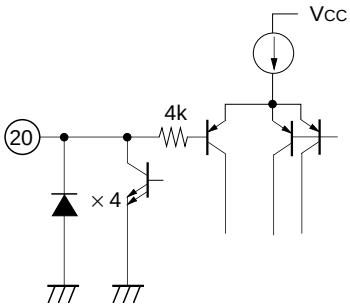
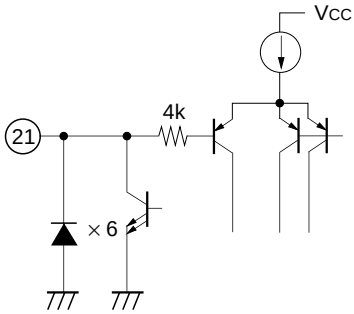
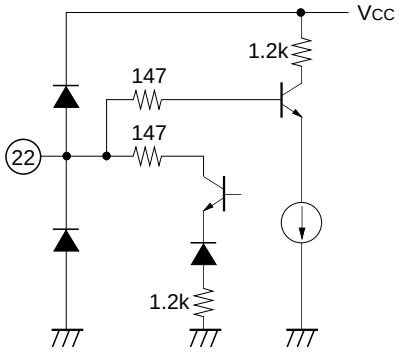
Block Diagram

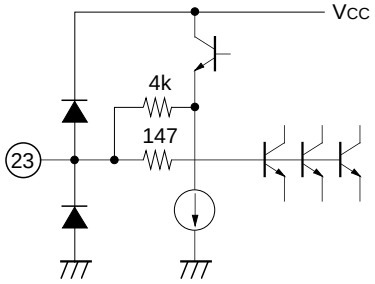
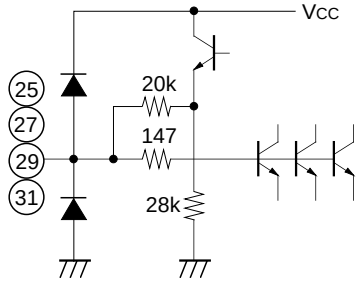
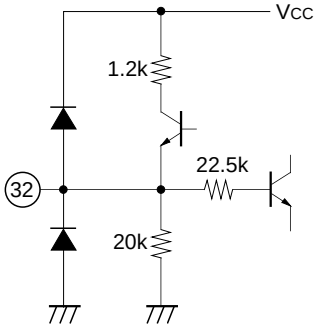


* Numbers inside circles indicate the IC pin numbers.

Pin Description

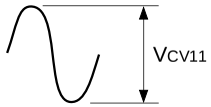
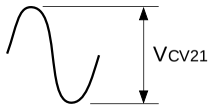
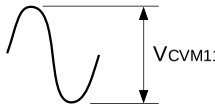
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 5 3 7	Y1 Y2 C1 C2	4.5V		Y/C separation signal inputs. Biased to approximately 4.5V. Input the input signals through capacitors. Connect protective resistor of 220Ω between these pins and the capacitors. Y1 and Y2 pins: Luminance signals input. C1 and C2 pins: Chrominance signals input.
4 6	S1 S2			Applying a DC voltage to S1 and S2 pins allows these voltages to be applied to the microcomputer as the I²C bus status register data. S1, S2 = 0 to 2V OPEN = 0, SEL = 1 S1, S2 = 4.75 to 7.25V OPEN = 0, SEL = 0 S1, S2 = 9.5 to 12V OPEN = 1, SEL = 0
11 9	YOUT COUT	4.5V		Y/C signal outputs. YOUT pin: Luminance signal output. COUT pin: Chrominance signal output.
17 15 13	CVOUT1 CVOUT2 CVOUT3	4.5V		Composite video signal outputs. CVOUT1, CVOUT2: 0dB output with respect to the input signal. CVOUT2: +6dB output with respect to the input signal.

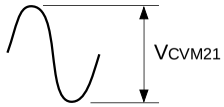
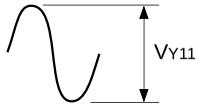
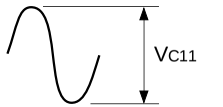
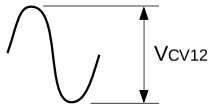
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
19	ADR			Selects the slave address for the I²C bus. 90H at 1.0V or less 92H at 3.5V or more 90H when open
20	SCL	—		I²C bus signal input. Connect protective resistor of 220Ω between this pin and the SCL line.
21	SDA	—		I²C bus signal input. Connect protective resistor of 220Ω between this pin and the SDA line.
22	SYNCTC			Sync tip clamp time constant for Sync Separation. Connect 68kΩ resistor between this pin and Vcc. Connect 0.1µF capacitor between this pin and GND.

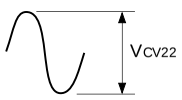
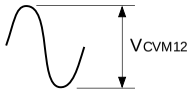
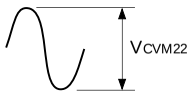
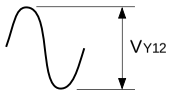
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
23	CV1	3.1V		Composite video signal input. Clamped to approximately 3.1V. Input the input signal through capacitor. Connect protective resistor of 220Ω between this pin and the capacitor. The composite video signal input to CV1 is also taken into the "SYNC DETECT circuit" of which SYNC is existed or not.
25 27 29 31	CV2 CV3 CV4 CV5	4.5V		Composite video signal input. Biased to approximately 4.5V. Input the input signals through capacitors. Connect protective resistor of 220Ω between these pins and the capacitors.
26	Vcc	9.0V*1		Power supply. Apply 9.0V.
2 28 30	GND	0.0V*1		GND.
32	BIAS	4.5V		4.5V bias. Attach a decoupling capacitor between this pin and GND. This pin cannot be used as an external power supply.
8 10 12 14 16 18 24	NC			NC (not connected). Connect to GND. If these NC pins are not connected to GND, the cross talk and other desired values indicated in the Electrical Characteristics cannot be obtained.

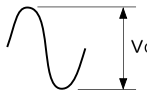
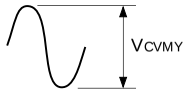
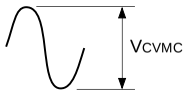
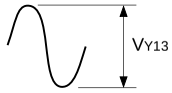
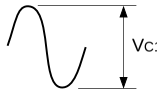
*1 Applied externally.

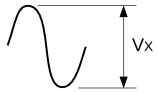
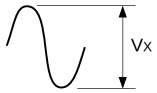
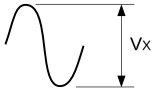
Electrical Characteristics See Electrical Characteristics Measurement Circuit 2 for Cross talk and MUTE. (Ta = 25°C, V_{CC} = 9V)
See Electrical Characteristics Measurement Circuit 1 for all other items.

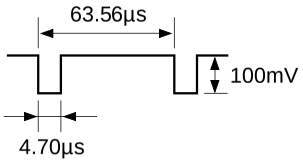
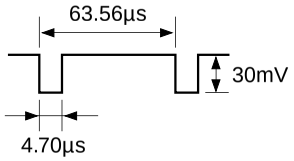
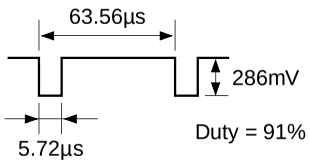
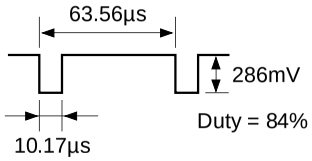
No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption	I_{CC}	V_{CC} = 9V, no signal	26	Measure the pin inflow current.	18.0	28	39.0	mA
2	Pin voltage	V_{BIAS}	V_{CC} = 9V, no signal	32	Measure the pin voltage.	4.25	4.50	4.75	V
3	CV system gain 1	G_{CV11}	CV1 In, CV2 In, CV3 In, CV4 In or CV5 In 100kHz, 0.3Vp-p CW Select each input with I²C bus control and obtain the I/O gain.	13, 17	 $20\text{Log}\frac{V_{CV11}}{0.3Vp\text{-}p}$	–0.40	0.00	0.40	dB
4	CV system gain 2	G_{CV21}	CV1 In, CV2 In, CV3 In, CV4 In or CV5 In 100kHz, 0.3Vp-p CW Select each input with I²C bus control and obtain the I/O gain.	15	 $20\text{Log}\frac{V_{CV21}}{0.3Vp\text{-}p}$	5.75	6.25	6.75	dB
5	CV system (Y/C MIX) gain 1	G_{CVM11}	Y1 and C1 (CV6) In or Y2 and C2 (CV7) In 100kHz, 0.15Vp-p CW Select each input with I²C bus control and obtain the I/O gain.	13, 17	 $20\text{Log}\frac{V_{CVM11}}{0.3Vp\text{-}p}$ * Since the sum of 0.15Vp-p and 0.15Vp-p is input to each switch, calculations are performed with 0.3Vp-p.	–0.40	0.10	0.60	dB

No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
6	CV system (Y/C MIX) gain 2	G_{CVM21}	Y1 and C1 (CV6) In or Y2 and C2 (CV7) In 100kHz, 0.15Vp-p CW Select each input with I^2C bus control and obtain the I/O gain.	15	 $20\text{Log}\frac{V_{CVM21}}{0.3\text{Vp-p}}$ * Since the sum of 0.15Vp-p and 0.15Vp-p is input to each switch, calculations are performed with 0.3Vp-p.	5.75	6.40	7.05	dB
7	Y system gain	G_{Y11}	Y1 In or Y2 In 100kHz, 0.3Vp-p CW Select each input with I^2C bus control and obtain the I/O gain.	11	 $20\text{Log}\frac{V_{Y11}}{0.3\text{Vp-p}}$	–0.40	0.00	0.40	dB
8	C system gain	G_{C11}	C1 In or C2 In 100kHz, 0.3Vp-p CW Select each input with I^2C bus control and obtain the I/O gain.	9	 $20\text{Log}\frac{V_{C11}}{0.3\text{Vp-p}}$	–0.40	0.00	0.40	dB
9	CV system frequency response 1	ΔG_{CV12}	CV1 In, CV2 In, CV3 In, CV4 In or CV5 In 10MHz, 0.3Vp-p CW Select each input with I^2C bus control and obtain the I/O gain. Then obtain the difference from the I/O gain measured by Test 3.	13, 17	 $20\text{Log}\frac{V_{CV12}}{V_{CV11}}$ * V_{CV11} and V_{CV12} should be the same I/O.	–0.85	–0.15	0.55	dB

No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
10	CV system frequency response 2	ΔG_{CV22}	CV1 In, CV2 In, CV3 In, CV4 In or CV5 In 10MHz, 0.3Vp-p CW Select each input with I²C bus control and obtain the I/O gain. Then obtain the difference from the I/O gain measured by Test 4.	15	 $20\text{Log}\frac{V_{CV22}}{V_{CV21}}$ * V_{CV21} and V_{CV22} should be the same I/O.	–0.85	–0.15	0.55	dB
11	CV system (Y/C MIX) frequency response 1	ΔG_{CVM12}	Y1 and C1 (CV6) In or Y2 and C2 (CV7) In 10MHz, 0.15Vp-p CW Select each input with I²C bus control and obtain the I/O gain. Then obtain the difference from the I/O gain measured by Test 5.	13, 17	 $20\text{Log}\frac{V_{CVM12}}{V_{CVM11}}$ * V_{CVM11} and V_{CVM12} should be the same I/O.	–1.75	–0.25	1.25	dB
12	CV system (Y/C MIX) frequency response 2	ΔG_{CVM22}	Y1 and C1 (CV6) In or Y2 and C2 (CV7) In 10MHz, 0.15Vp-p CW Select each input with I²C bus control and obtain the I/O gain. Then obtain the difference from the I/O gain measured by Test 6.	15	 $20\text{Log}\frac{V_{CVM22}}{V_{CVM21}}$ * V_{CVM21} and V_{CVM22} should be the same input.	–1.75	–0.25	1.25	dB
13	Y system frequency response	ΔG_{Y12}	Y1 In or Y2 In 10MHz, 0.3Vp-p CW Select each input with I²C bus control and obtain the I/O gain. Then obtain the difference from the I/O gain measured by Test 7.	11	 $20\text{Log}\frac{V_{Y12}}{V_{Y11}}$ * V_{Y11} and V_{Y12} should be the same input.	–0.70	0.00	0.70	dB

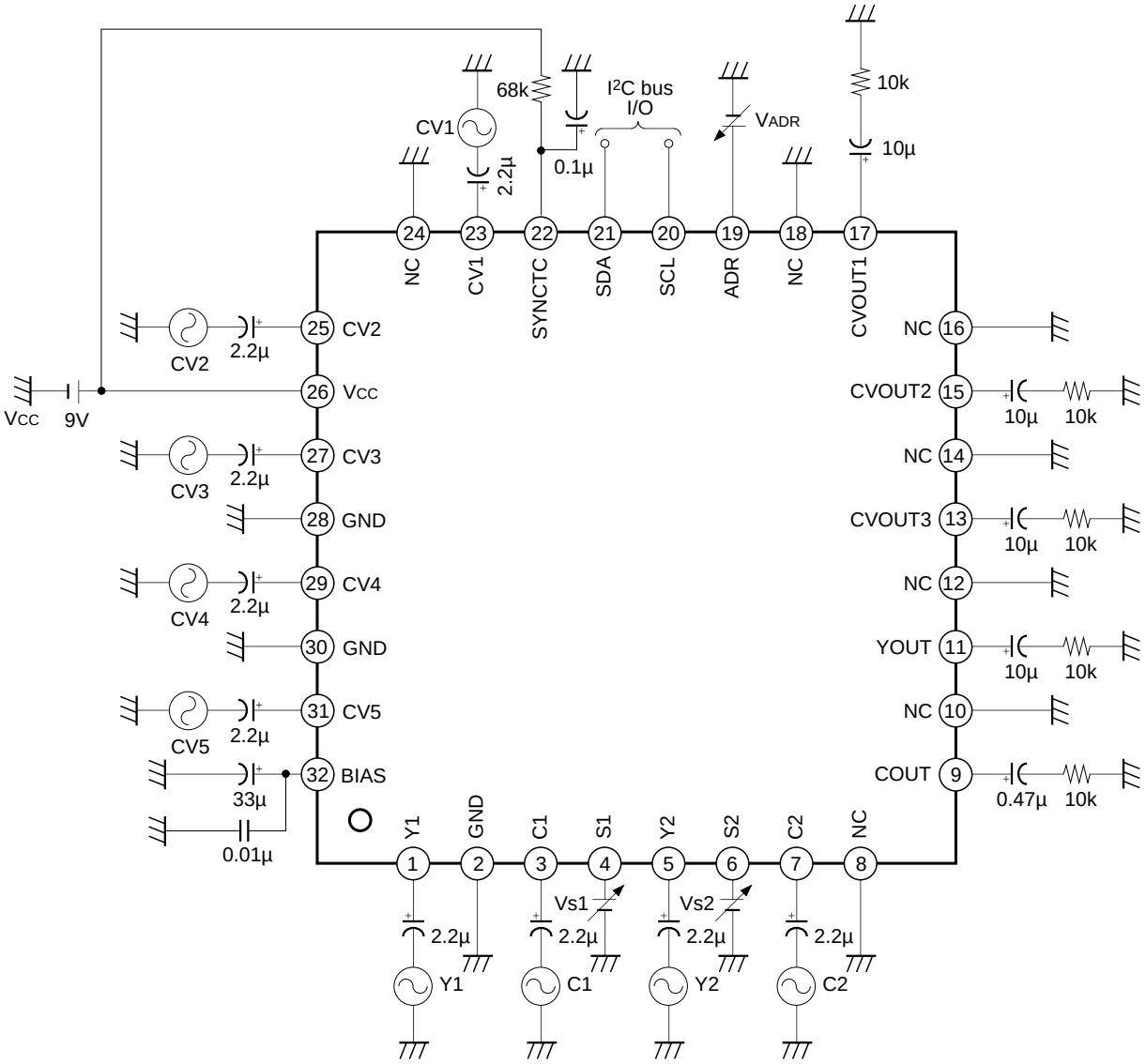
No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
14	CV system input dynamic range	V_{CV13}	CV1 In, CV2 In, CV3 In, CV4 In or CV5 In f = 100kHz CW Select each input with I²C bus control and then increase the input waveform amplitude.	23, 25, 27, 29, 31		2.2			Vp-p
					The input waveform amplitude value when Pins 13, 15 or 17 output waveform distortion factor = 1%.	The value for the PAL composite signal should correspond to an amplitude of approximately 1Vp-p + 3dB.			
15	CV system (Y/C MIX) input dynamic range	V_{CVMY33}	Y1 (CV6) In or Y2 (CV7) In f = 100kHz CW Select each input with I²C bus control and then increase the input waveform amplitude.	1, 5	Y1 or Y2 input waveform 	2.2			Vp-p
					The input waveform amplitude value when Pins 13, 15 or 17 output waveform distortion factor = 1%.	The value for the PAL Y signal should correspond to an amplitude of approximately 1Vp-p + 3dB.			
		V_{CVMC33}	C1 (CV6) In or C2 (CV7) In f = 100kHz CW Select each input with I²C bus control and then increase the input waveform amplitude.	3, 7	C1 or C2 input waveform 	0.95			Vp-p
					The input waveform amplitude value when Pins 13, 15 or 17 output waveform distortion factor = 1%.	The value for the PAL C signal should correspond to an amplitude of approximately 0.66Vp-p + 3dB.			
16	Y system input dynamic range	V_{Y13}	Y1 In or Y2 In f = 100kHz CW Select each input with I²C bus control and then increase the input waveform amplitude.	1, 5		2.2			Vp-p
					The input waveform amplitude value when Pin 11 output waveform distortion factor = 1%.	The value for the PAL Y signal should correspond to an amplitude of approximately 1Vp-p + 3dB.			
17	C system input dynamic range	V_{C13}	C1 In or C2 In f = 100 kHz CW Select each input with I²C bus control and then increase the input waveform amplitude.	3, 7		2.2			Vp-p
					The input waveform amplitude value when Pin 9 output waveform distortion factor = 1%.	The value for the C signal should correspond to an amplitude of approximately 2.2Vp-p.			

No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
18	Cross talk	G_{CRS}	Select the input with I²C bus control and ground that input pin via a capacitor. Input a 4.43MHz, 1Vp-p CW to one input pin system among the remaining 8 input pins (7 input pins for Y/C MIX). Then ground the remaining 7 input pins (6 input pins for Y/C MIX) via capacitors.	9, 11, 13, 15, 17	Read the output waveform value.  $20\text{Log}\frac{V_X}{1Vp\text{-}p}$			–55	dB
19	MUTE (CV system 1, Y system, C system)	G_{M1}	Set this pin to MUTE status with I²C bus control and input a 4.43MHz, 1Vp-p CW to one input pin system. Then ground the remaining 8 input pins via capacitors.	9, 11, 13, 17	Read the output waveform value.  $20\text{Log}\frac{V_X}{1Vp\text{-}p}$			–50	dB
20	MUTE (CV system 2)	G_{M2}	Set this pin to MUTE status with I²C bus control and input a 4.43MHz, 1Vp-p CW to one input pin system. Then ground the remaining 8 input pins via capacitors.	15	Read the output waveform value.  $20\text{Log}\frac{V_X}{1Vp\text{-}p}$			–45	dB

No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
21	SYNC discrimination 11	SYNCD11	CV1 In: Sig-1 	21 (SDA)	Input Sig-1 to CV1 and check that bit 5 "SYNCSEP" of the I²C bus status register is "1" when the Sig-1 sync level is 100mV or more.	100			mV
					The Sig-1 sync level should correspond to approximately –9dB when the 1Vp-p NTSC composite signal sync level (286mV) is set as 0dB.				
22	SYNC discrimination 21	SYNCD21	CV1 In: Sig-2 	21 (SDA)	Input Sig-2 to CV1 and check that bit 5 "SYNCSEP" of the I²C bus status register is "0" when the Sig-2 sync level is 30mV or less.			30	mV
					The Sig-2 sync level should correspond to approximately –19dB when the 1Vp-p NTSC composite signal sync level (286mV) is set as 0dB.				
23	SYNC discrimination 12	SYNCD12	CV1 In: Sig-3 	21 (SDA)	Input Sig-3 to CV1 and check that bit 5 "SYNCSEP" of the I²C bus status register is "1" when the Sig-3 duty is 91% or more (the sync width is 5.72µs or less).	91			%
					Sync is determined to exist when the sync level is 100mV or more and a rectangular wave with a duty of 91% or more is input to CV1.				
24	SYNC discrimination 22	SYNCD22	CV1 In: Sig-4 	21 (SDA)	Input Sig-4 to CV1 and check that bit 5 "SYNCSEP" of the I²C bus status register is "0" when the Sig-4 duty is 84% or less (the sync width is 10.17µs or more).			84	%
					Sync is determined not to exist when a rectangular wave with a duty of 84% or less is input to CV1 even when the sync level is 100mV or more.				

No.	Item	Symbol	Measurement conditions	Measurement pins	Measurement contents	Min.	Typ.	Max.	Unit
25	ADR threshold voltage	$V_{ADR}V_{TH}$	Vary the Pin 19 V_{ADR}.	21	The slave address goes to 92H at high level and 90H at low level.	1.0		3.5	V

Electrical Characteristics Measurement Circuit 1



*1 Unless otherwise specified in the Measurement conditions column of Electrical Characteristics, all ⏦ are GND.

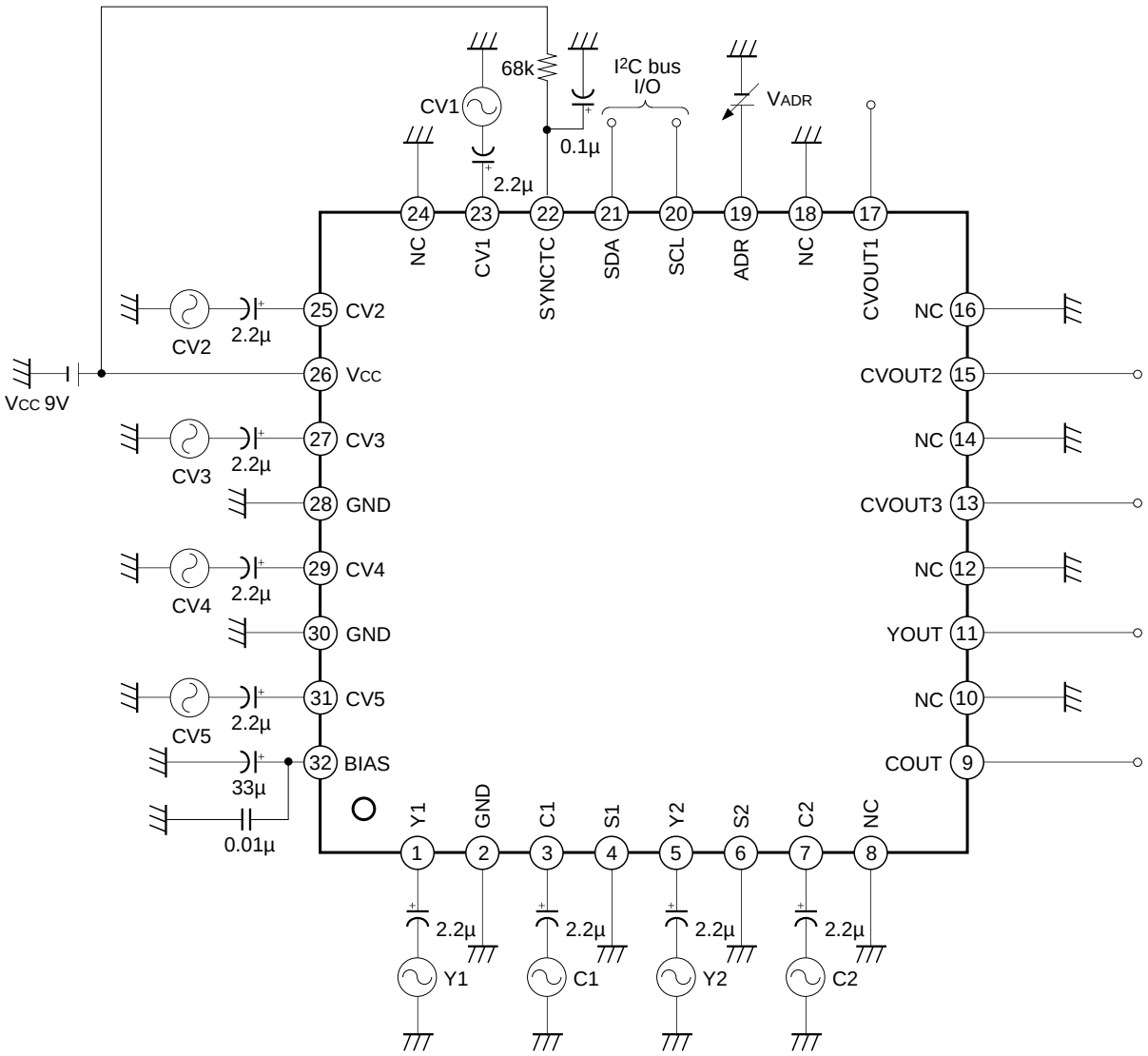
*2 Unless otherwise specified in the Measurement conditions column of Electrical Characteristics, the supply voltages are as follows.

V_{CC} = 9V, V_{S1} = 0V, V_{S2} = 0V

V_{ADR} = 0V when operated with a slave address of 90H.

V_{ADR} = 9V (V_{CC}) when operated with a slave address of 92H.

Electrical Characteristics Measurement Circuit 2 (Cross talk, MUTE)



*1 Unless otherwise specified in the Measurement conditions column of Electrical Characteristics, all ⏦ are GND.

*2 Unless otherwise specified in the Measurement conditions column of Electrical Characteristics, the supply voltages are as follows.

V_{CC} = 9V

V_{ADR} = 0V when operated with a slave address of 90H.

V_{ADR} = 9V (V_{CC}) when operated with a slave address of 92H.

I²C Bus Control Map

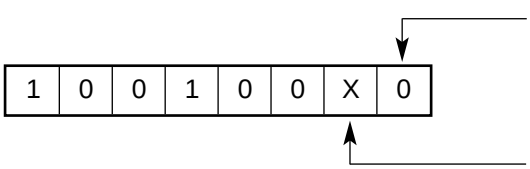
1) Control Register

The CXA2040AQ control system is comprised of 4 bytes of control registers which control the various outputs. The inputs which are to be output are selected by writing the respective input data into the control register.

S	Slave address	A	DATA1	A	DATA2	A	DATA3	A	DATA4	A	P

S: START CONDITION
A: ACKNOWLEDGE
P: STOP CONDITION

• Slave address



R/W bit
This bit is set to "0" when data is to be written into the control registers.

Value set by the address pin

DATA1 Controls the video output 1.
DATA2 Controls the video output 2.
DATA3 Controls the video output 3.
DATA4 Controls the S terminal output.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	X	video select			X	X	X

Each register is set to "0" upon POWER ON.

• Video switch control map

bit5	bit4	bit3	Selected input signal
0	0	0	MUTE
0	0	1	CV1/YC1
0	1	0	CV2/YC2
0	1	1	CV3
1	0	0	CV4
1	0	1	CV5
1	1	0	CV6
1	1	1	CV7

Other conditions: MUTE

2) Status Register

S	Slave address	A	DATA	NA	P

S: START CONDITION
P: STOP CONDITION
A: ACKNOWLEDGE

• Slave address

1	0	0	1	0	0	X	1

R/W bit
This bit is set to "1" when data is to be read into the status registers.

Value set by the address pin

DATA

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PON RES	X	SYNC SEP	X	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL

(1) PONRES
Returns "1" when the CXA2040AQ is POWER ON RESET. Becomes "0" after reading once.

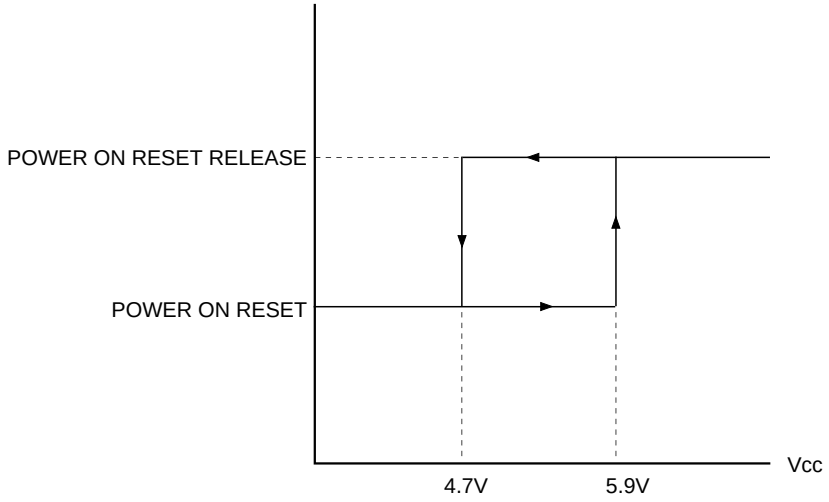
(2) SYNCSEP
"1" returns if sync exists, "0" if sync does not exist.

(3) OPEN/SEL for S1 and S2 is determined by comparing the DC voltages for S1 and S2 pins with two threshold levels.

DC voltages for S1 and S2 pins	S1, S2 OPEN	S1, S2 SEL
2V or less	0	1
4.75 to 7.25V	0	0
9.5 to 12V	1	0

3) POWER ON RESET

The CXA2040AQ incorporates a POWER ON RESET function which sets each control register to "0" upon POWER ON. (Which goes to MUTE status.)
The POWER ON RESET V_{TH} has hysteresis. The POWER ON V_{CC} and released V_{CC} are as shown below. Also, the PONRES bit of the status register is read to determine whether the IC is reset upon POWER ON.



Description of Operation

1) Composite Video System I/Os

There are three systems of composite outputs. Each output switch can select the eight systems of CV1 to CV5 composite video inputs, CV6 and CV7 Y/C MIX (composite video) inputs and MUTE. All composite video inputs are input from the input pins to each switch by DC coupling. CV6 is the composite video signal obtained by inputting Y1 and C1 to an adder and adding Y1 and C1. CV7 is the composite video signal obtained by inputting Y2 and C2 to an adder and adding Y2 and C2. The CV6 and CV7 composite video signals are input from the input pins to each switch by DC coupling. When MUTE is selected, the internal bias DC output (approximately $V_{CC}/2$ [V]) is input to each switch. Only one type of input is selected by the I^2C bus control register. The CVOUT1 and CVOUT3 switches output the signal selected by the I^2C bus at a gain of 0 [dB] with respect to the input signal. The switch output stages are push-pull circuits which output at low impedance. The CVOUT2 switch outputs the signal selected by the I^2C bus amplified to +6 [dB] with respect to the input signal. The switch output stage is a push-pull circuit which outputs at low impedance. The switches are DC coupled from input to output.

2) Y System I/Os

The YOUT switch can select the three systems of Y1, Y2 and MUTE. Y1 and Y2 are input from the input pins to the switch by DC coupling. When MUTE is selected, the internal bias DC output (approximately $V_{CC}/2$ [V]) is input to the switch. Only one type of input is selected by the I^2C bus control register. The YOUT switch outputs the signal selected by the I^2C bus at a gain of 0 [dB] with respect to the input signal. The switch output stage is a push-pull circuit which outputs at low impedance. The switch is DC coupled from input to output.

3) C System I/Os

The COUT switch can select the three systems of C1, C2 and MUTE. C1 and C2 are input from the input pins to the switch by DC coupling. When MUTE is selected, the internal bias DC output (approximately $V_{CC}/2$ [V]) is input to the switch. Only one type of input is selected by the I^2C bus control register. The COUT switch outputs the signal selected by the I^2C bus at a gain of 0 [dB] with respect to the input signal. The switch output stage is a push-pull circuit which outputs at low impedance. The switch is DC coupled from input to output.

4) Sync Discrimination

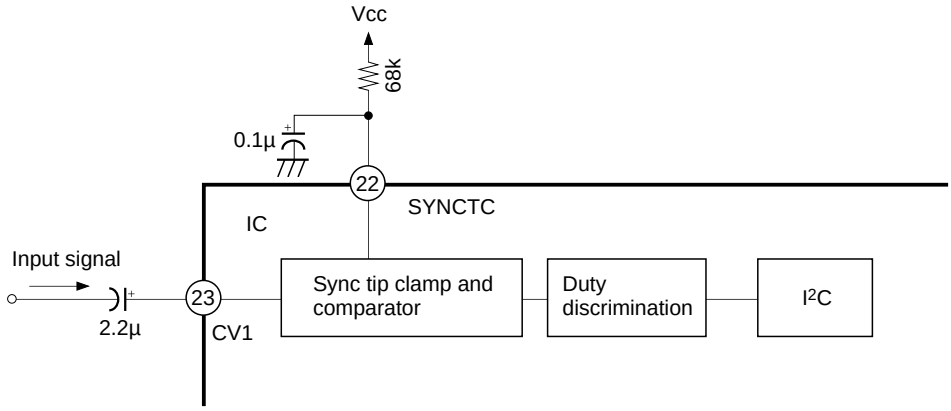
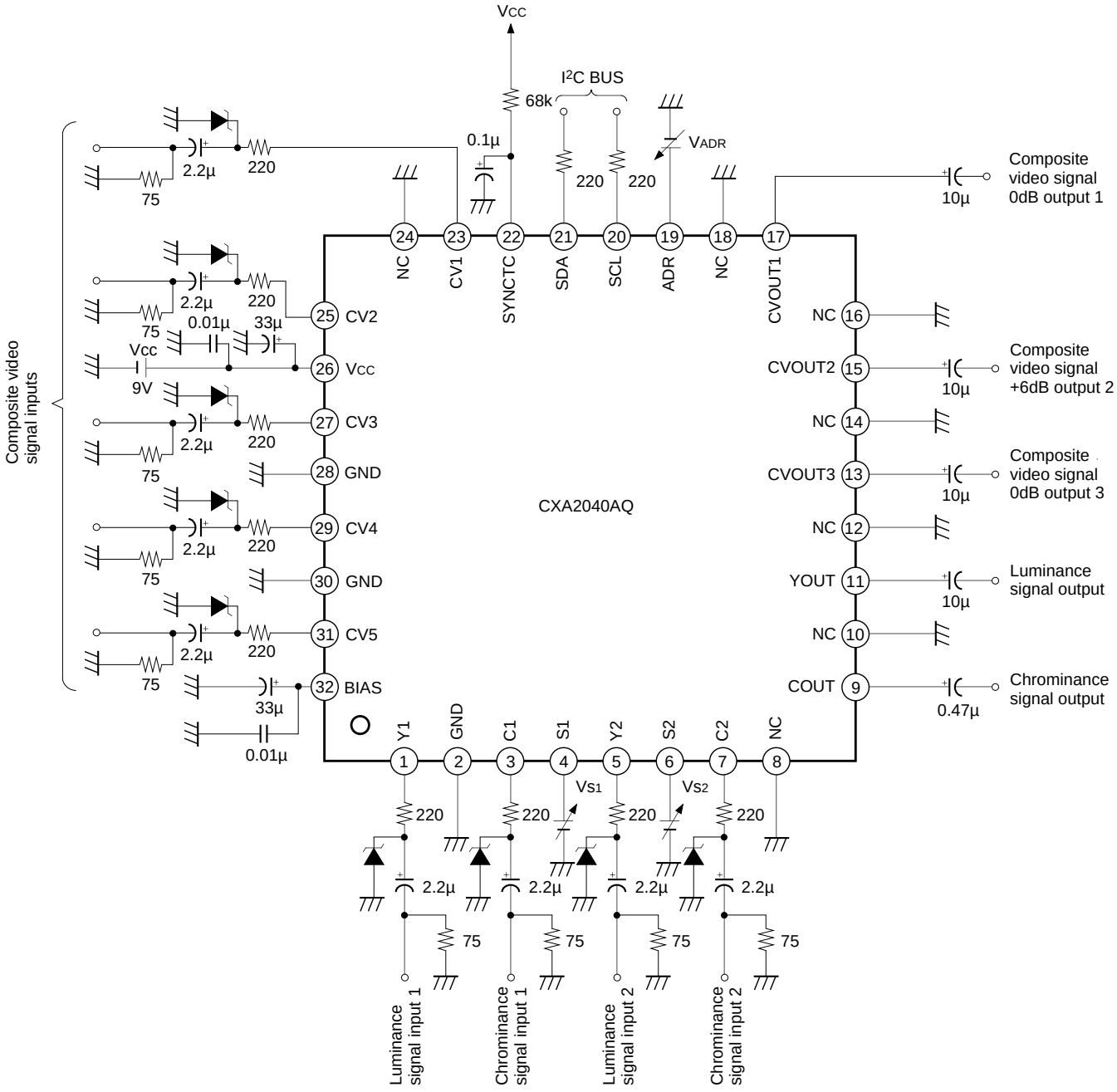


Fig. 1. Sync discrimination circuit block diagram

Fig. 1 shows the block diagram for the sync discrimination circuit. The signal input from Pin 23 (CV1) is sync tip clamped by the external element attached to Pin 22. This signal is compared with a threshold voltage which is larger than the sync tip level. If the signal is smaller than the threshold level, it does not proceed to the following stage. At this time, the IC determines that sync does not exist. If the signal is larger than the threshold level, it proceeds to the duty discrimination block. If the duty is greater than 91%, the duty discrimination block determines that sync exists and sends the data to the I^2C. If the duty is less than 84%, sync is determined not to exist and the data is sent to the I^2C. The duty discrimination block also has a time constant. After sync is determined to exist, the sync status is held for approximately 14H (NTSC signal) even if the IC goes to a status where sync does not exist such as no signal, etc. If there is no signal or sync does not exist for longer than 14H, the status switches from sync exists to sync does not exist.

Application Circuit



*1 Input pins of Pins 1, 3, 5, 7, 25, 27, 29 and 31 are biased to approximately 4.2 to 4.7V (Pin 23 biased to approximately 3.1V). Therefore, care should be taken for the capacitance polarity.

*2 Output pins of Pins 9, 11, 13, 15 and 17 are biased to approximately 3.8 to 4.8V. Therefore, care should be taken for the capacitance polarity.

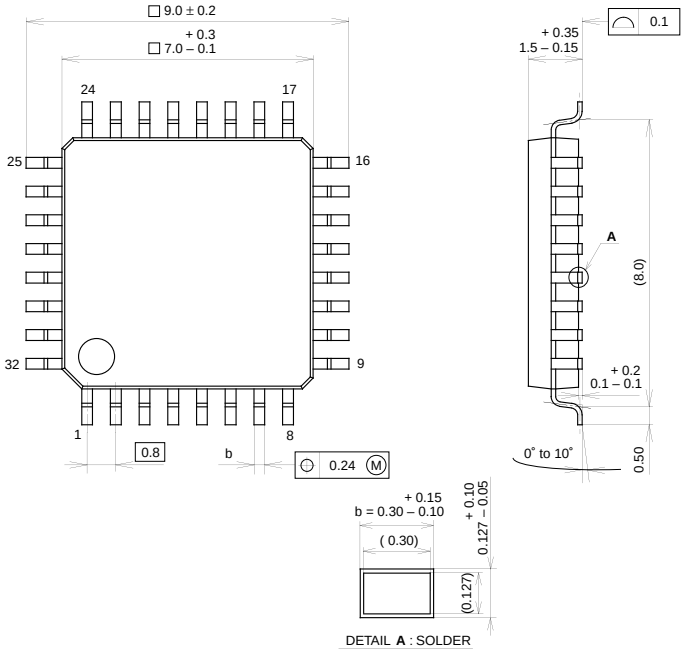
*3 Set V_{ADR} to 0V (GND) when the IC slave address is 90H, or to 9V (V_{CC}) when the IC slave address is 92H.

Notes on Operation

- Connect the power supply side of the by-pass capacitor between the power supply and GND as close to the pin as possible.
- Take care not to allow interference signals to enter Pin 32 (BIAS). If interference signals enter Pin 32, the signal S/N, cross talk and MUTE will deteriorate. Therefore, connect the by-pass capacitor, etc. as close to the pins as possible.
- For dual surface boards, using one side as a solid earth is best.
- Pins 2, 8, 10, 12, 14, 16, 18, 24 and 28 are NC (not connected) pins. Connect these NC pins to GND. If these NC pins are not connected to GND, the cross talk and other desired values indicated in the Electrical Characteristics cannot be obtained.
- Input pins of Pins 1, 3, 5, 7, 25, 27, 29 and 31 are biased between 4.2 and 4.7V. Therefore, care should be taken over the polarity of the coupling capacitor.
- Input pin 23 is clamped to approximately 3.1V. Therefore, care should be taken over the polarity of the coupling capacitor.
- Output pins of Pins 9, 11, 13, 15 and 17 are biased between 3.8 and 4.8V. Therefore, care should be taken over the polarity of the coupling capacitor.

Package Outline Unit: mm

32PIN QFP (PLASTIC)

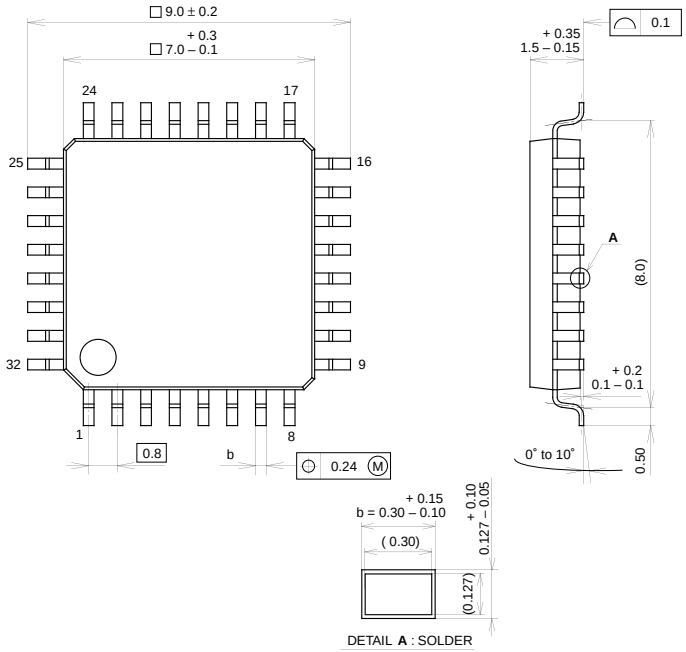


PACKAGE STRUCTURE

SONY CODE	QFP-32P-L01
EIAJ CODE	P-QFP32-7x7-0.8
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.2g

32PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-32P-L01
EIAJ CODE	P-QFP32-7x7-0.8
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.2g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm