# CD4063B Types

## CMOS 4-Bit Magnitude Comparator

### High Voltage Types (20-Volt Rating)

■ CD4063B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063B has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs (A < B, A = B, and A > B) on the least significant comparator are connected to a low, a high, and a low level, respectively.

The CD4063B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix). This device is pin-compatible with the standard 7485 TTL type.

### Features:

■ **Expansion to 8, 12, 16....4N bits by cascading units**
■ **Medium-speed operation:**
   **compares two 4-bit words
   in 250 ns (typ.) at 10 V**
■ **100% tested for quiescent current at 20 V**
■ **Standardized symmetrical output characteristics**
■ **5-V, 10-V, and 15-V parametric ratings**
■ **Maximum input current of 1 $\mu$A at 18 V
   over full package temperature range;
   100 nA at 18 V and 25°C**
■ **Noise margin (full package temperature range)
   range) = 1 V at $V_{DD}$ = 5 V
   2 V at $V_{DD}$ = 10 V
   2.5 V at $V_{DD}$ = 15 V**
■ **Meets all requirements of JEDEC Tentative
   Standard No. 13B, "Standard Specifications
   for Description of 'B' Series CMOS Devices"**

### Applications:

■ **Servo motor controls**  ■ **Process controllers**

**FUNCTIONAL DIAGRAM**

(TOP VIEW)
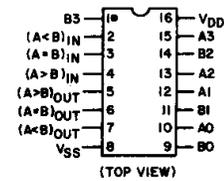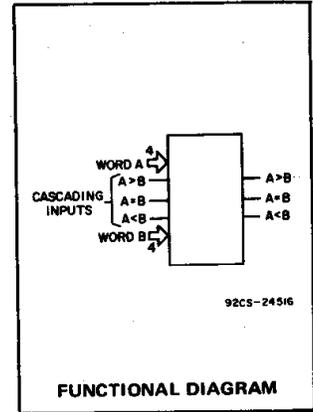
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**TERMINAL ASSIGNMENT**

### MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
   Voltages referenced to $V_{SS}$ Terminal) .................................................................–0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ............................................... –0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ............................................................±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
   For $T_A$ = –55°C to +100°C ............................................................. 500mW
   For $T_A$ = +100°C to +125°C.......................................Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
   FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)......................... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$)..............................................–55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$)..............................................–65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
   At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ............................+265°C

### RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
| --- | --- | --- | --- |
| | Min. | Max. | |
| Supply-Voltage Range (For $T_A$=Full Package-Temperature Range) | 3 | 18 | V |
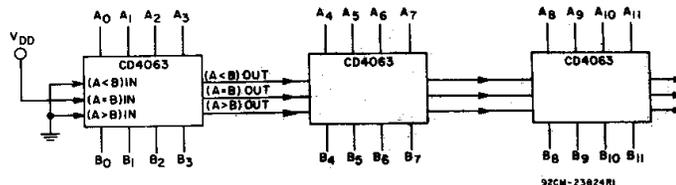
$$I_{P\ TOTAL} = I_P \left(\begin{array}{c}COMPARE\\INPUTS\end{array}\right) + 2 \times I_P \left(\begin{array}{c}CASCADE\\INPUTS\end{array}\right), AT\ V_{DD} = 10V$$
(3 STAGES)

= 250 +(2 x 200) = 650 ns (TYP.)

*Fig. 1 — Typical speed characteristics of a 12-bit comparator.*

# CD4063B Types

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTER-ISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | +25 Min. | +25 Typ. | +25 Max. | |
| Quiescent Device Current, $I_{DD}$ Max. | − | 0,5 | 5 | 5 | 5 | 150 | 150 | − | 0.04 | 5 | μA |
| | − | 0,10 | 10 | 10 | 10 | 300 | 300 | − | 0.04 | 10 | |
| | − | 0,15 | 15 | 20 | 20 | 600 | 600 | − | 0.04 | 20 | |
| | − | 0,20 | 20 | 100 | 100 | 3000 | 3000 | − | 0.08 | 100 | |
| Output Low (Sink) Current, $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | − | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | − | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | − | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | −0.64 | −0.61 | −0.42 | −0.36 | −0.51 | −1 | − | |
| | 2.5 | 0,5 | 5 | −2 | −1.8 | −1.3 | −1.15 | −1.6 | −3.2 | − | |
| | 9.5 | 0,10 | 10 | −1.6 | −1.5 | −1.1 | −0.9 | −1.3 | −2.6 | − | |
| | 13.5 | 0,15 | 15 | −4.2 | −4 | −2.8 | −2.4 | −3.4 | −6.8 | − | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | − | 0,5 | 5 | 0.05 | | | | − | 0 | 0.05 | V |
| | − | 0,10 | 10 | 0.05 | | | | − | 0 | 0.05 | |
| | − | 0,15 | 15 | 0.05 | | | | − | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | − | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | − | |
| | − | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | − | |
| | − | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | − | |
| Input Low Voltage, $V_{IL}$ Max. | 0.5, 4.5 | − | 5 | 1.5 | | | | − | − | 1.5 | V |
| | 1, 9 | − | 10 | 3 | | | | − | − | 3 | |
| | 1.5, 13.5 | − | 15 | 4 | | | | − | − | 4 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5, 4.5 | − | 5 | 3.5 | | | | 3.5 | − | − | |
| | 1, 9 | − | 10 | 7 | | | | 7 | − | − | |
| | 1.5, 13.5 | − | 15 | 11 | | | | 11 | − | − | |
| Input Current $I_{IN}$ Max. | − | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | − | ±$10^{-5}$ | ±0.1 | μA |

**TRUTH TABLE**

| INPUTS | | | | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|
| COMPARING | | | | CASCADING | | | | | |
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A < B | A = B | A > B | A < B | A = B | A > B |
| A3 > B3 | X | X | X | X | X | X | 0 | 0 | 1 |
| A3 = B3 | A2 > B2 | X | X | X | X | X | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 > B1 | X | X | X | X | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | 0 | 0 | 1 | 0 | 0 | 1 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | 0 | 1 | 0 | 0 | 1 | 0 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | 1 | 0 | 0 | 1 | 0 | 0 |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | 1 | 0 | 0 |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | 1 | 0 | 0 |
| A3 = B3 | A2 < B2 | X | X | X | X | X | 1 | 0 | 0 |
| A3 < B3 | X | X | X | X | X | X | 1 | 0 | 0 |

X = Don't Care          Logic 1 ≡ High Level          Logic 0 ≡ Low Level
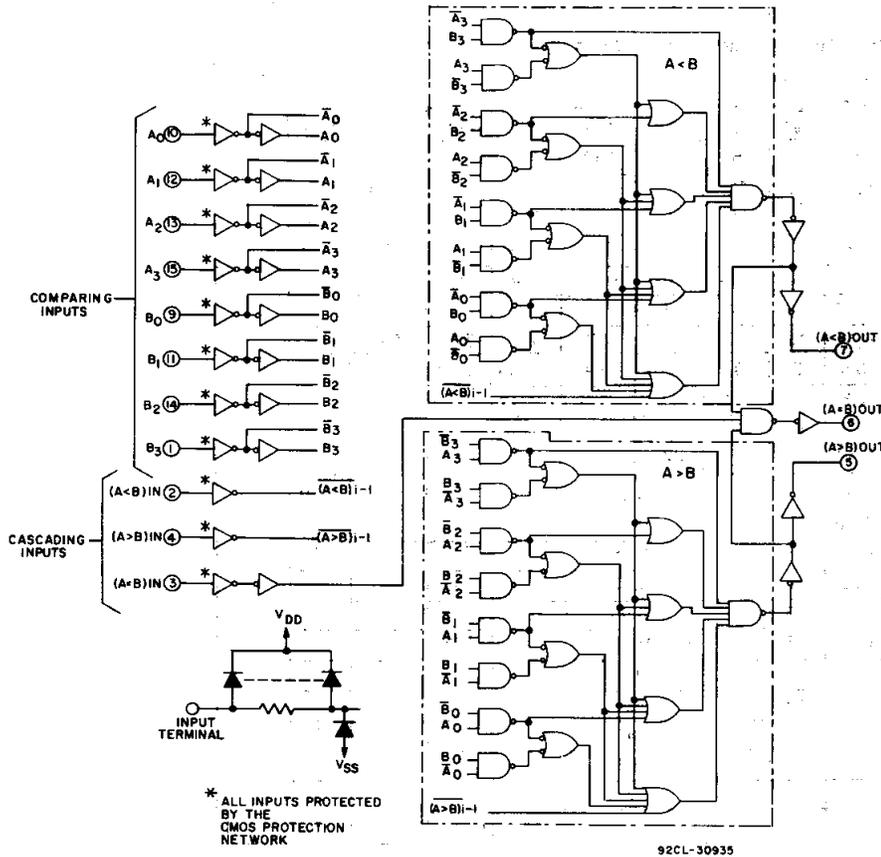
COMMERCIAL CMOS HIGH VOLTAGE ICs
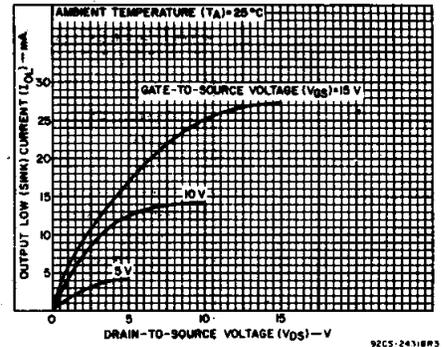
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Fig. 2 — Logic diagram for CD4063B.



Fig. 3 — Typical output low (sink) current characteristics.
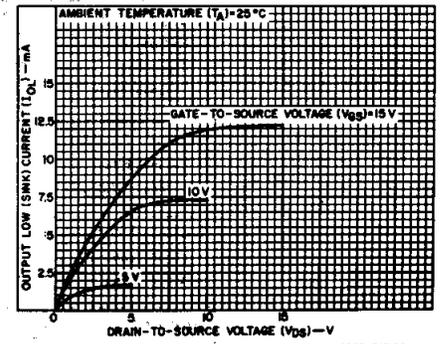


Fig. 4 — Minimum output low (sink) current characteristics.
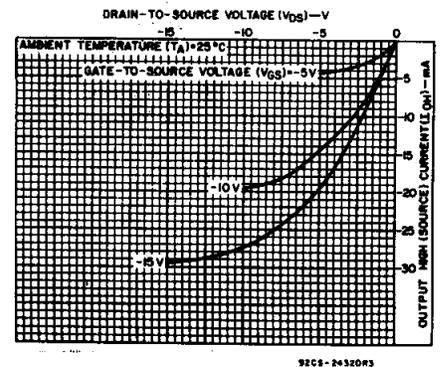


Fig. 5 — Typical output high (source) current characteristics.
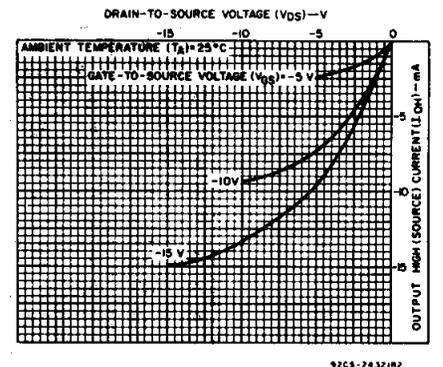


Fig. 6 — Minimum output high (source) current characteristics.

## DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input $t_r$, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200k\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | UNITS |
|---|---|---|---|---|
| | $V_{DD}$ Volts | Typ. | Max. | |
| Propagation Delay Time: Comparing Inputs to Outputs, $t_{PHL}$, $t_{PLH}$ | 5 | 625 | 1250 | ns |
| | 10 | 250 | 500 | |
| | 15 | 175 | 350 | |
| Cascading Inputs to Outputs, $t_{PHL}$, $t_{PLH}$ | 5 | 500 | 1000 | |
| | 10 | 200 | 400 | |
| | 15 | 140 | 280 | |
| Transition Time, $t_{THL}$, $t_{TLH}$ | 5 | 100 | 200 | ns |
| | 10 | 50 | 100 | |
| | 15 | 40 | 80 | |
| Input Capacitance, $C_{IN}$ | Any Input | 5 | 7.5 | pF |

Fig. 7 — Typical propagation delay time vs. load capacitance ("comparing inputs" to outputs).



Fig. 8 — Typical propagation delay time vs. supply voltage ("comparing inputs" to outputs).
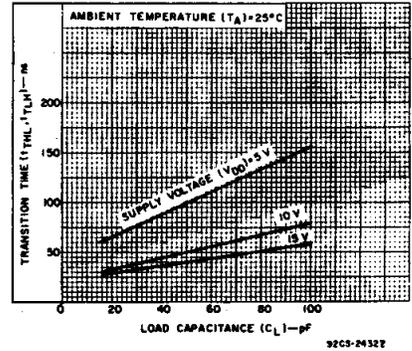


Fig. 9 — Typical transition time vs. load capacitance.
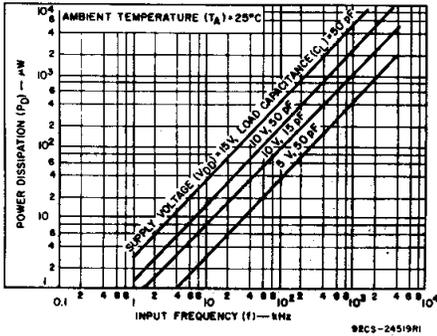


Fig. 10 — Typical power dissipation vs. frequency (see Fig. 12 — dynamic power dissipation test circuit).



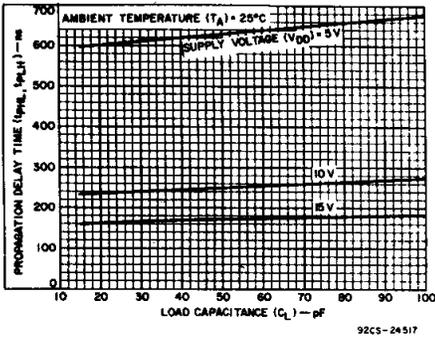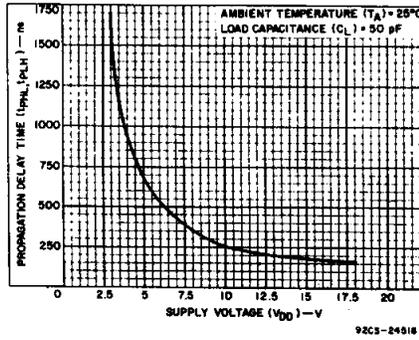Fig. 11 — Input current test circuit.



Fig. 12 — Dynamic power dissipation test circuit.



Fig. 13 — Input-voltage test circuit.



Fig. 14 — Quiescent-device-current test circuit.



Dimensions and pad layout for CD4063BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

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**IMPORTANT NOTICE**

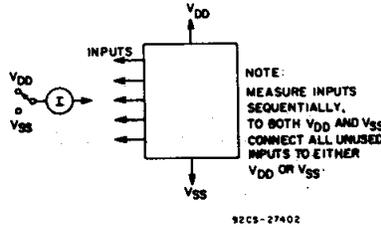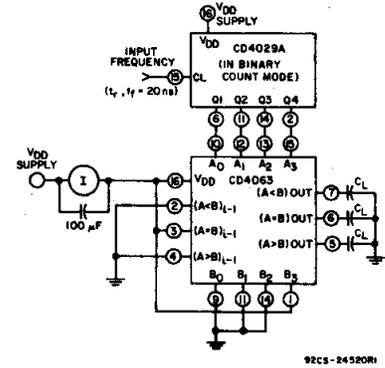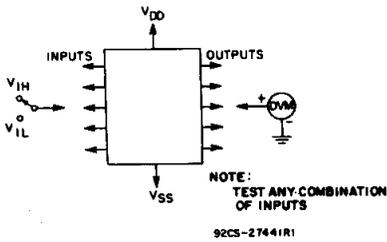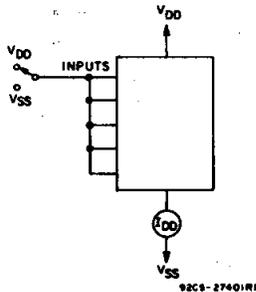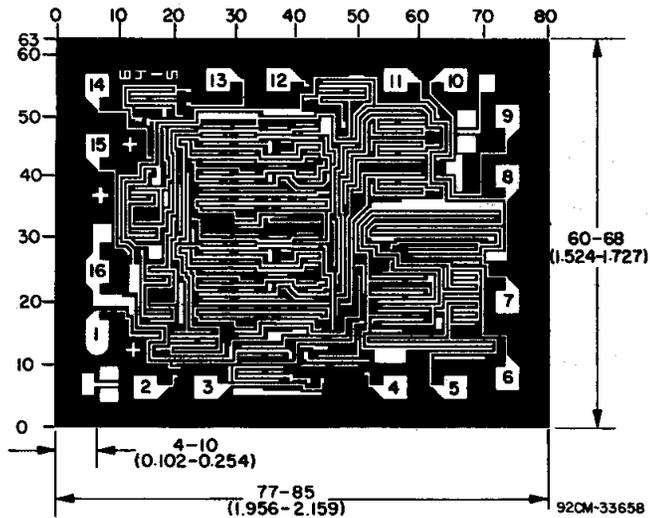Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

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