

## DUPLEX LCD DRIVER

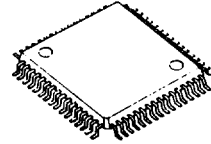
## ■ GENERAL DESCRIPTION

The NJU6432B is a duplex LCD driver to drive segment type LCD panel.

2-common and 53-segment drivers can drive up to 104 segments.

The NJU6432B is useful for the Digital Tuning System or others segment type display driver.

## ■ PACKAGE OUTLINE

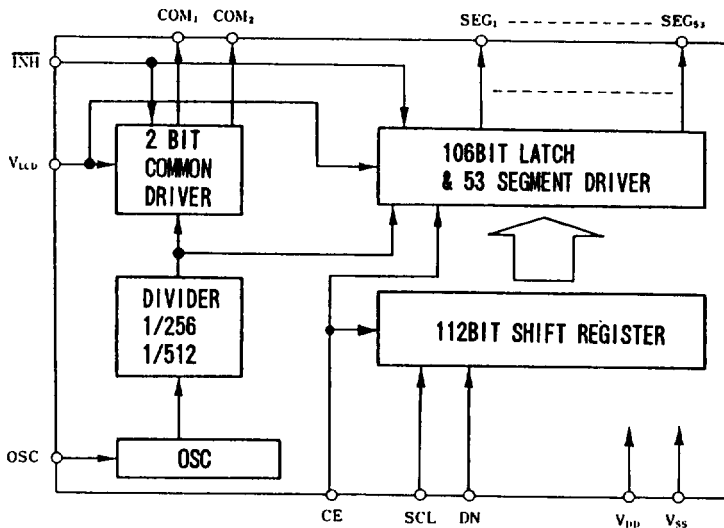


## ■ FEATURES

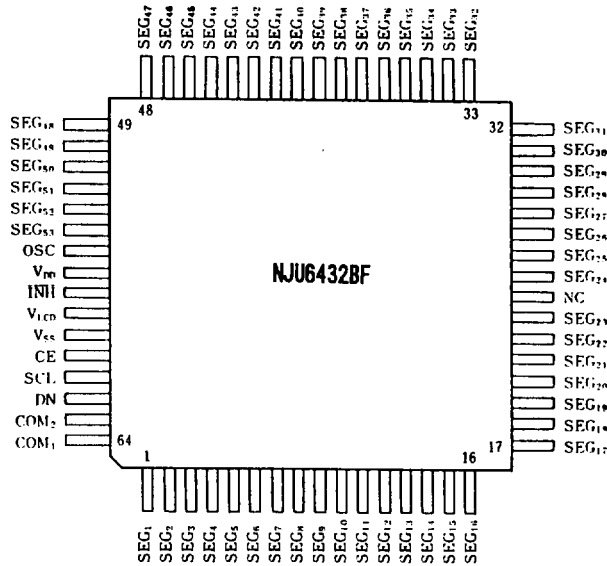
- 53 Segment Drivers
- Duty Ratio 1/2 ;104-Segment Drive
- Serial Data Transmission ( Shift Clock 2MHz max.)
- Display Off Function (INH Terminal)
- Operating Voltage --- 6.5V Max.
- Package Outline --- QFP 64
- C-MOS Technology

NJU6432BF

## ■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION



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## ■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1~23 25~53	SEG <sub>1</sub> ~ SEG <sub>23</sub> SEG <sub>24</sub> ~ SEG <sub>43</sub>	Segment Output Terminal
54	SEG <sub>53</sub>	Normally On Segment Output Terminal(When the "L" level input to the TNH terminal, this segment also turns off.)
55	OSC	Oscillating Terminal
56,59	V <sub>DD</sub> , V <sub>SS</sub>	Power Supply
57	TNH	Display-Off Control Terminal: When "L" level input to this terminal, all of the display turns off including SEG <sub>53</sub> .
58	V <sub>LCD</sub>	Power Supply for LCD Driving
60	CE	Chip Enable Terminal
61	SCL	Serial Data Transmission Clock Terminal
62	DN	Serial Data Input Terminal
63 64	COM <sub>2</sub> COM <sub>1</sub>	Common Output Terminal.
24	NC	Non Connection



■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuits

Oscillation by connecting external resistor and capacitor.  
 This circuits supply the basical clock signal to other circuits like as common driver and segment driver.

(1-2) Driving Circuits

This circuit divide the oscillating frequency by 1/256 and 1/512, and generate the common and segment output timing signals.

(1-3) Shift-Register

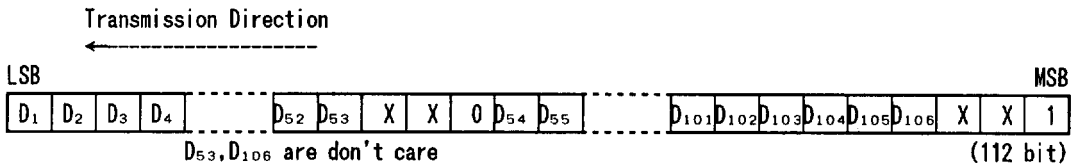
During the CE signal is "H", the data input to this shift-register by synchronizing the shift clock.

(1-4) Latch and Segment Driver

During the CE signal is "L", the data in the shift-register transfer to the latch and the segment driver output the LCD driving waveform according to the latched data.

(2) Data Input Format (The Data Correspond to the Output)

(2-1) Data Input Format



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(2-2) Input Data Correspond to Segment Status

Data D <sub>xxx</sub>	Segment Status
"H"	ON
"L"	OFF

## (2-3) Input Data Correspond to Segment Terminals

Segment	Data	COM <sub>1</sub>	COM <sub>2</sub>
SEG <sub>1</sub>	D <sub>1</sub>	○	
	D <sub>2</sub>		○
SEG <sub>2</sub>	D <sub>3</sub>	○	
	D <sub>4</sub>		○
SEG <sub>3</sub>	D <sub>5</sub>	○	
	D <sub>6</sub>		○
SEG <sub>26</sub>	D <sub>51</sub>	○	
	D <sub>52</sub>		○
SEG <sub>27</sub>	D <sub>54</sub>	○	
	D <sub>55</sub>		○
SEG <sub>49</sub>	D <sub>98</sub>	○	
	D <sub>99</sub>		○
SEG <sub>50</sub>	D <sub>100</sub>	○	
	D <sub>101</sub>		○
SEG <sub>51</sub>	D <sub>102</sub>	○	
	D <sub>103</sub>		○
SEG <sub>52</sub>	D <sub>104</sub>	○	
	D <sub>105</sub>		○
SEG <sub>53</sub>	ON	○	
	ON		○

## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Voltage	V <sub>DD</sub>	- 0.3 ~ + 7.0	V
Operating Voltage	V <sub>LCD</sub>	- 0.3 ~ V <sub>DD</sub> +0.3	V
Input Voltage (1)	V <sub>IN</sub>	- 0.3 ~ + 7.0	V
Input Voltage (2)	V <sub>IN</sub>	- 0.3 ~ V <sub>DD</sub> +0.3	V
Output Voltage (2)	V <sub>O</sub>	- 0.3 ~ V <sub>DD</sub> +0.3	V
Output Current (3)	I <sub>O</sub>	100	μA
Output Current (4)	I <sub>O</sub>	1.0	mA
Power Dissipation	P <sub>D</sub>	300	mW
Operating Temperature	T <sub>opr</sub>	- 30 ~ + 85	°C
Storage Temperature	T <sub>stg</sub>	- 40 ~ + 125	°C

- \* 1) CE, SCL, DN Terminals
- \* 2) OSC Terminal during OFF-output
- \* 3) SEG<sub>1</sub>~SEG<sub>53</sub> Terminals
- \* 4) COM<sub>1</sub>, COM<sub>2</sub> Terminals


**ELECTRICAL CHARACTERISTICS**
**DC Characteristics**

 (Ta=-30~+85°C. V<sub>DD</sub>=6.5V, V<sub>SS</sub>=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V <sub>DD</sub>	V <sub>DD</sub> Terminal	2.5		6.5	V
Supply Voltage	V <sub>LCD</sub>	V <sub>LCD</sub> Terminal	2.5		V <sub>DD</sub>	V
Operating Current	I <sub>DD</sub>	V <sub>DD</sub> Terminal			1	mA
Operating Current	I <sub>LCD</sub>	V <sub>LCD</sub> Terminal			2	mA
"H" Input Voltage	V <sub>IH</sub>	T <sub>NH</sub> Terminal	0.7V <sub>DD</sub>		6.5	V
"L" Input Voltage	V <sub>IL</sub>	T <sub>NH</sub> Terminal	0		0.3V <sub>DD</sub>	V
"H" Input Voltage	V <sub>IH</sub>	CE,SCL, DN Terminals	0.8V <sub>DD</sub>		6.5	V
"L" Input Voltage	V <sub>IL</sub>	CE,SCL, DN Terminals	0		0.2V <sub>DD</sub>	V
Oscillator Resistor	R <sub>osc</sub>	OSC Terminal		51		kΩ
Oscillator Capacitor	C <sub>osc</sub>	OSC Terminal		680		pF
Oscillator Frequency	f <sub>osc</sub>	OSC Terminal	25	50	100	kHz
"H" Input Current	I <sub>IH</sub>	V <sub>IN</sub> =6.5V, CE, SCL, DN, T <sub>NH</sub> Terminals			5	μA
"L" Input Current	I <sub>IL</sub>	V <sub>IN</sub> =0V, CE, SCL, DN, T <sub>NH</sub> Terminals			5	μA
"H" Output Voltage	V <sub>OH</sub>	I <sub>O</sub> =-10μA SEG <sub>1</sub> ~SEG <sub>53</sub> Terminals	V <sub>LCD</sub> -1.0			V
"L" Output Voltage	V <sub>OL</sub>	I <sub>O</sub> =10μA SEG <sub>1</sub> ~SEG <sub>53</sub> Terminals			1.0	V
"H" Output Voltage	V <sub>OH</sub>	I <sub>O</sub> =-100μA COM <sub>1</sub> , COM <sub>2</sub> Terminals	V <sub>LCD</sub> -0.6			V
"L" Output Voltage	V <sub>OL</sub>	I <sub>O</sub> =100μA COM <sub>1</sub> , COM <sub>2</sub> Terminals			0.6	V
Middle Level Voltage	V <sub>MID</sub>	I <sub>O</sub> =±100μA, V <sub>LCD</sub> =6.5V	2.65	3.25	3.85	V
		I <sub>O</sub> =±100μA, V <sub>LCD</sub> =3.0V	0.9	1.5	2.1	
Hysteresis Voltage	V <sub>H</sub>	V <sub>DD</sub> =5V, CE,SCL, DN Terminals	0.3			V

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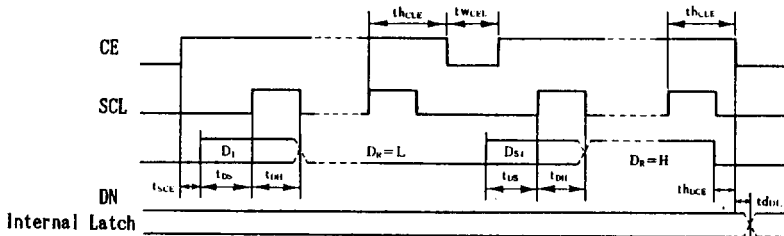


## AC Characteristics

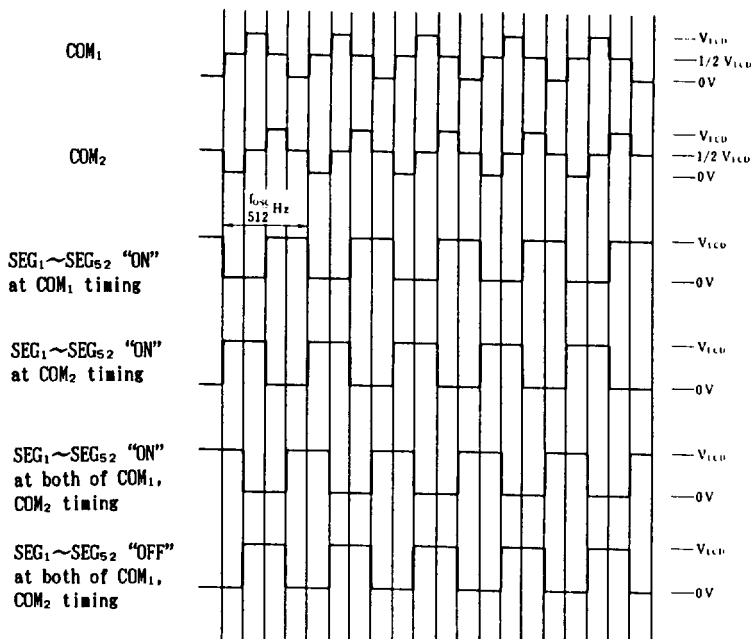
 (T<sub>a</sub>=-30~+85°C, V<sub>DD</sub>=6.5V, V<sub>SS</sub>=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t <sub>WCLL</sub>	SCL Terminal	0.25			μs
"H" Clock Pulse Width	t <sub>WCLH</sub>	SCL Terminal	0.25			μs
Data Set-up Time	t <sub>DS</sub>	SCL, DN Terminals	0.25			μs
Data Hold Time	t <sub>DH</sub>	SCL, DN Terminals	0.25			μs
CE Set-up Time	t <sub>SCE</sub>	CE, DN Terminals	1			μs
CE Hold Time (1)	t <sub>HDCE</sub>	CE, DN Terminals	1			μs
CE Hold Time (2)	t <sub>HCLE</sub>	CE, SCL Terminals	1.25			μs
Data Latch Delay Time	t <sub>dDLP</sub>				1	μs
"L" Clock Enable Pulse Width	t <sub>WCLE</sub>	CE Terminal	4			μs

## • Input Timing Characteristics


 The data is latched at D<sub>R</sub>=H and falling edge of the CE signal condition.

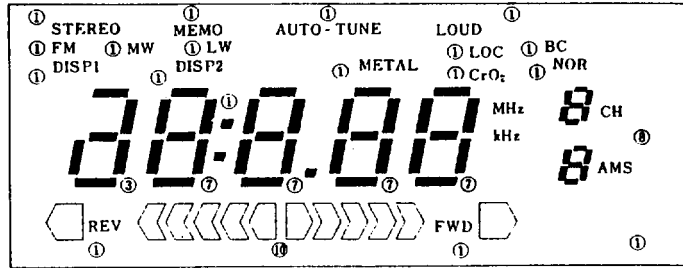
## • Output Timing Characteristics





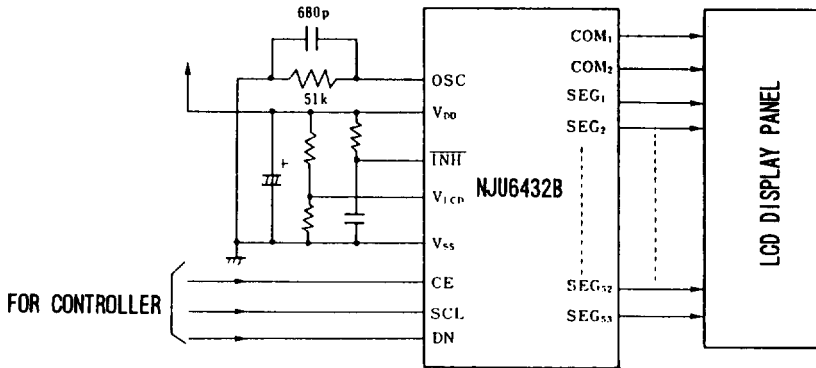
■ DISPLAY EXAMPLE

Example: 71 segments (MAX. 104 segments)



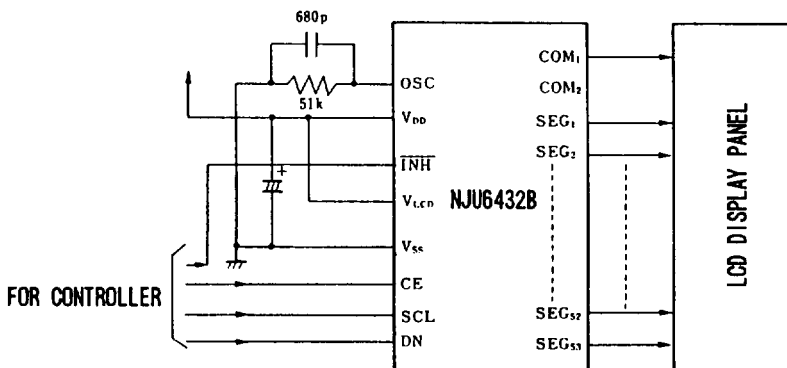
■ APPLICATION CIRCUITS

① In case of  $V_{LCD} < V_{DD}$



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② In case of  $V_{LCD} = V_{DD}$



(Note) After rising edge of  $V_{DD}$  voltage, the display data is not guaranteed and which blinking is meaningless display. Therefore, keep  $\overline{TNH}$  terminal to Low Level by the display data transferred is needed.