TOSHIBA

GaAℓAs IRED & PHOTO-IC

TLP651

Unit in mm

Digital Logic Ground Isolation

Line Receiver

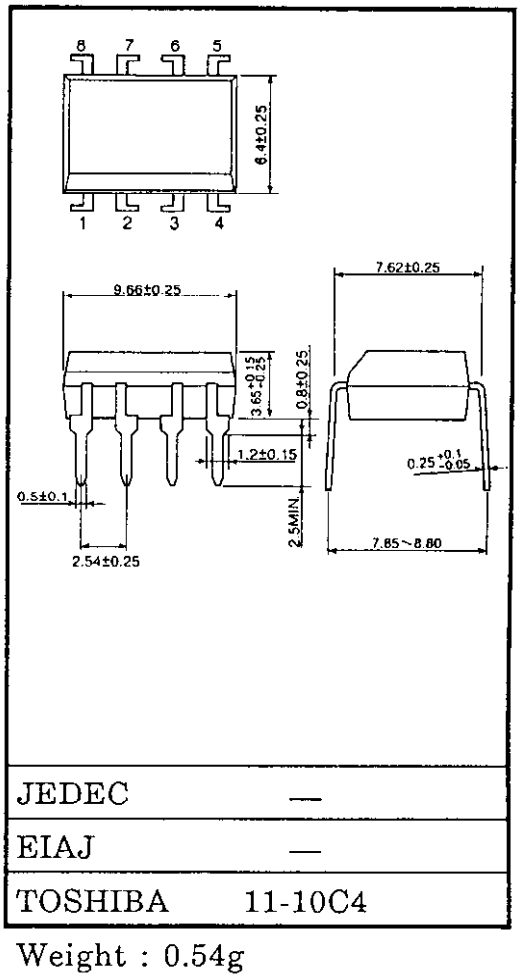
Microprocessor System Interfaces

Switching Power Supply Feedback Control

Analog Signal Isolation

The Toshiba TLP651 consists of a GaAℓAs high-output light emitting diode and a high speed detector of one chip photo diode-transistor. This unit is in an 8-lead DIP package. TLP651 has an internal base connection. This base pin should be used for analog applications or to enable operations. If the base pin is open, the output signal will be noisy depending on environmental conditions. In this case, TLP650 is suitable.

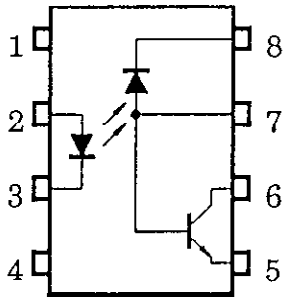
- Isolation Voltage : 5000V_{rms} (Min.)
- Switching Speed : t_{pHL} = 0.3μs (Typ.)
  : t_{pLH} = 0.5μs (Typ.) (R_L = 1.9kΩ)
- TTL Compatible
- UL Recognized : UL1577, File No. E67349



JEDEC	—
EIAJ	—
TOSHIBA	11-10C4

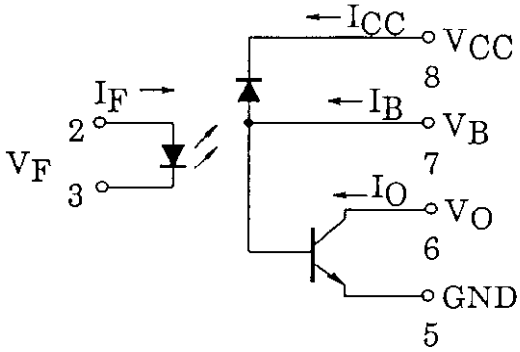
Weight : 0.54g

Pin Configuration (Top View)



1 : N.C.
2 : ANODE
3 : CATHODE
4 : N.C.
5 : EMITTER
6 : COLLECTOR
7 : BASE
8 : V_{CC}

Schematic



Supplementary Information	Page (s)
Lead Form Options	31-32
Tape and Reel	39-40
Current Transfer Ratio	29-31

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Maximum Ratings (Ta = 25°C)

CHARACTERISTIC			SYMBOL	RATING	UNIT
LED	Forward Current	(Note 1)	I_F	25	mA
	Forward Current Derating	(Note 2)	I_{FP}	50	mA
	Peak Transient Forward Current	(Note 3)	I_{FPT}	1	A
	Reverse Voltage		V_R	5	V
	Diode Power Dissipation	(Note 4)	P_D	45	mW
DETECTOR	Output Current		I_O	8	mA
	Peak Output Current		I_{OP}	16	mA
	Output Voltage		V_O	-0.5~15	V
	Supply Voltage		V_{CC}	-0.5~15	V
	Base Current		I_B	5	mA
	Emitter-Base Reverse Voltage		V_{EB}	5	V
	Output Power Dissipation	(Note 5)	P_O	100	mW
Operating Temperature Range			T_{opr}	-55~100	°C
Storage Temperature Range			T_{stg}	-55~125	°C
Lead Soldering Temperature (10 sec.)		(Note 6)	T_{sol}	260	°C
Total Package Power Dissipation			P_T	250	mW
Isolation Voltage (AC, 1 min, R.H. ≤ 60%)		(Note 7)	BV_S	5000	V_{rms}

Note 1: Derate 0.8mA above 70°C.
Note 2: 50% duty cycle, 1ms pulse width. Derate 1.6mA/°C above 70°C.
Note 3: Pulse width ≤ 1μs, 300pps.
Note 4: Derate 0.9mW/°C above 70°C.
Note 5: Derate 2mW/°C above 70°C.
Note 6: Soldering portion of lead: up to 2mm from the body of the device.
Note 7: Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

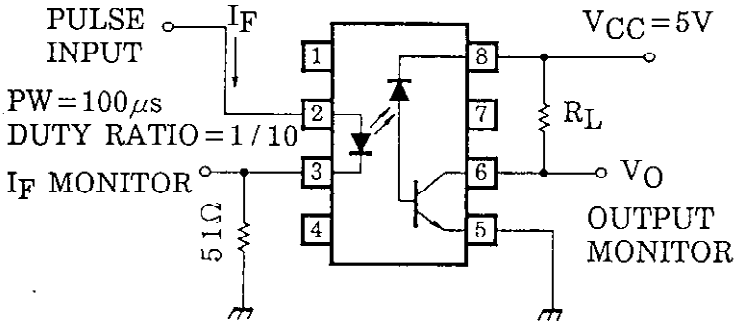
Electrical Characteristics (Ta = 25°C)

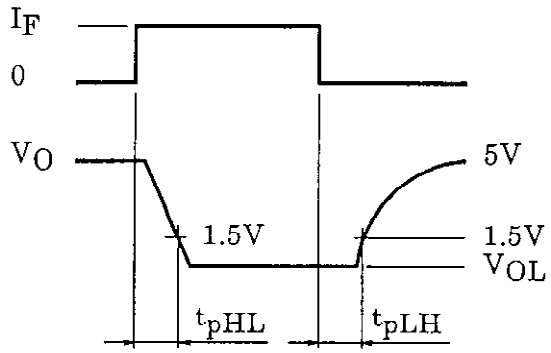
CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN.	TYP.	MX.	UNIT
LED	Forward Voltage	V_F	I_F = 16mA		–	1.65	1.85	V
	Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta Ta$	I_F = 16mA		–	-2	–	mV/°C
	Reverse Current	I_R	V_R = 5V		–	–	10	μA
	Capacitance Between Terminal	C_T	V_F = 0, f = 1MHz		–	45	–	pF
DETECTOR	High Level Output Current	$I_{OH(1)}$	I_F = 0mA, V_{CC} = V_O = 5.5V		–	3	500	nA
		$I_{OH(2)}$	I_F = 0mA, V_{CC} = V_O = 15V		–	–	5	μA
		I_{OH}	I_F = 0mA, V_{CC} = V_O = 15V Ta = 70°C		–	–	250	μA
	High Level Supply Voltage	I_{CCH}	I_F = 0mA, V_{CC} = 15V		–	0.01	1	μA
COUPLED	Current Transfer Ratio	I_O/I_F	I_F = 16mA V_{CC} = 4.5V V_O = 0.4V	Ta = 25°C	10	30	–	%
				Rank: 0	19	30	–	
				Ta = 0~70°C	5	–	–	
				Rank: 0	15	–	–	
	Low Level Output Voltage	V_{OL}	I_F = 16mA, V_{CC} = 4.5V, I_O = 1.1mA (Rank 0: I_O = 2.4mA)		–	–	0.4	V
	Isolation Resistance	R_S	R.H. ≤ 60%, V_S = 500V_{DC} (Note 7)		–	10^{12}	–	Ω
	Capacitance Between Input to Output	C_S	V_S = 0, f = 1MHz (Note 7)		–	0.8	–	pF

Switching Characteristics (Ta = 25°C)

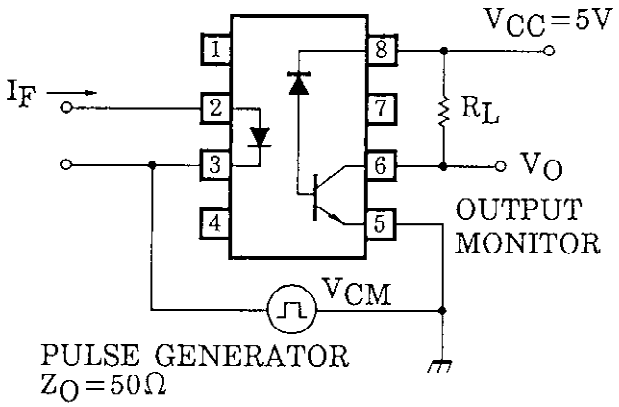
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MX.	UNIT
Propagation Delay Time (H→L)	t_{pHL}	1	I_F = 0→16mA, V_{CC} = 5V,		–	0.2	0.8	μs
			R_L = 4.1kΩ	Rank 0: R_L = 1.9kΩ	–	0.3	0.8	
Propagation Delay Time (L→H)	t_{pLH}		I_F = 16→0mA, V_{CC} = 5V,		–	1.0	2.0	μs
			R_L = 4.1kΩ	Rank 0: R_L = 1.9kΩ	–	0.5	1.2	
Common Mode Transient Immunity at Logic High Output (Note 8)	C_{MH}	2	I_F = 0mA, V_{CM} = 200Vp-p R_L = 4.1kΩ (Rank 0: R_L = 1.9kΩ)		–	400	–	V/μs
Common Mode Transient Immunity at Logic Low Output (Note 8)	C_{ML}		I_F = 16mA, V_{CM} = 200Vp-p R_L = 4.1kΩ (Rank 0: R_L = 1.9kΩ)		–	-1000	–	V/μs

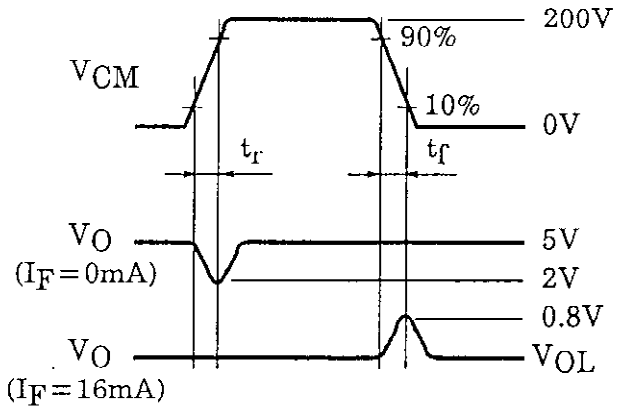
TEST CIRCUIT 1 : Switching Time Test Circuit





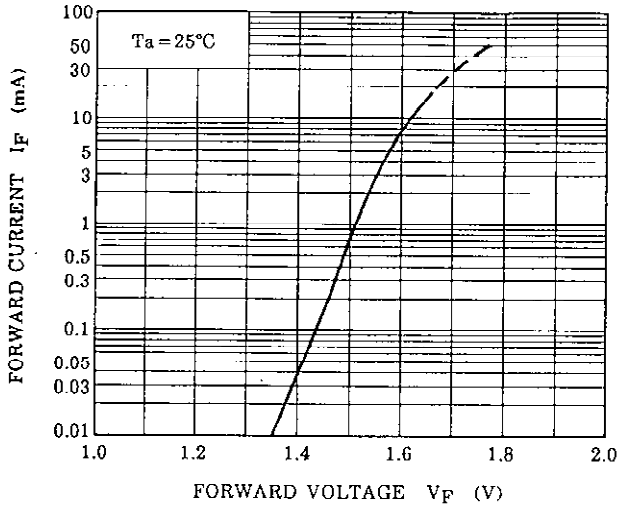
TEST CIRCUIT 2 : Common Mode Noise Immunity Test Circuit



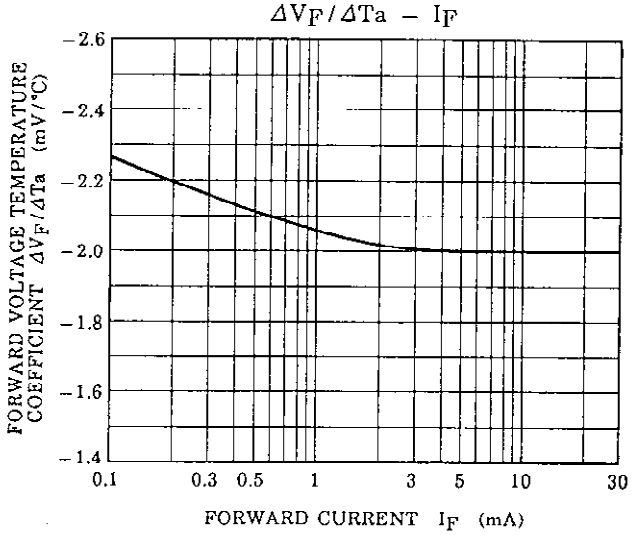


$$CM_H = \frac{160\,(V)}{t_r\,(\mu s)},\ CM_L = \frac{160\,(V)}{t_f\,(\mu s)}$$

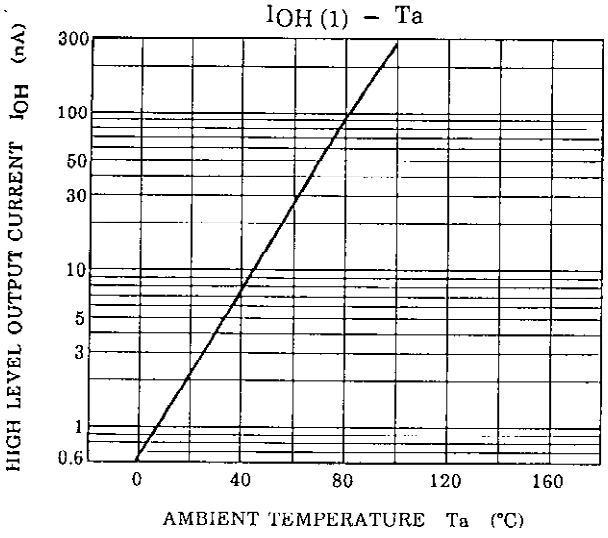
$I_F - V_F$



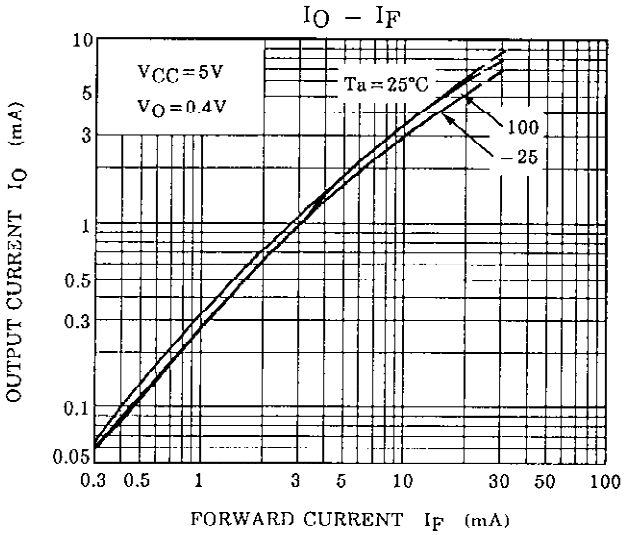
$\Delta V_F / \Delta Ta - I_F$



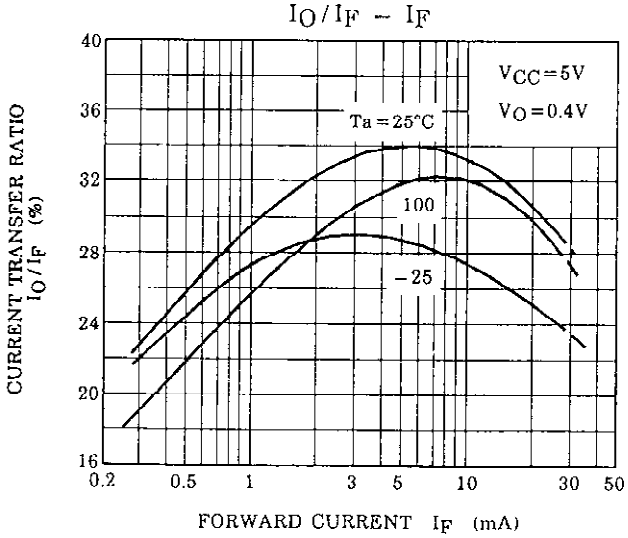
I_{OH} (1) – Ta



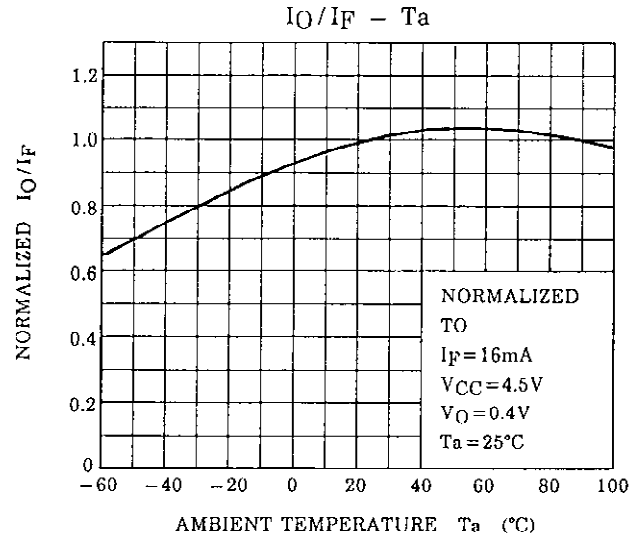
$I_O - I_F$



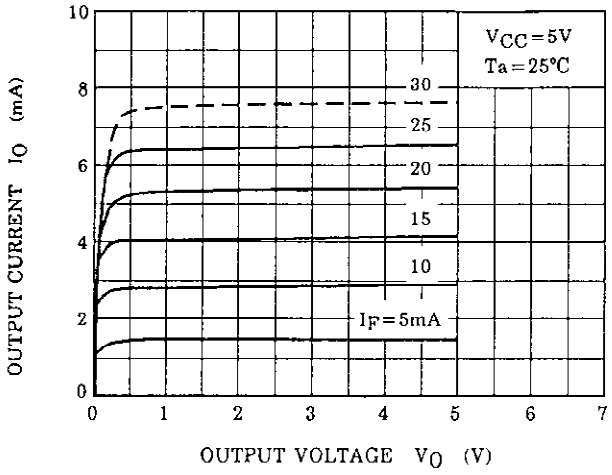
$I_O / I_F - I_F$



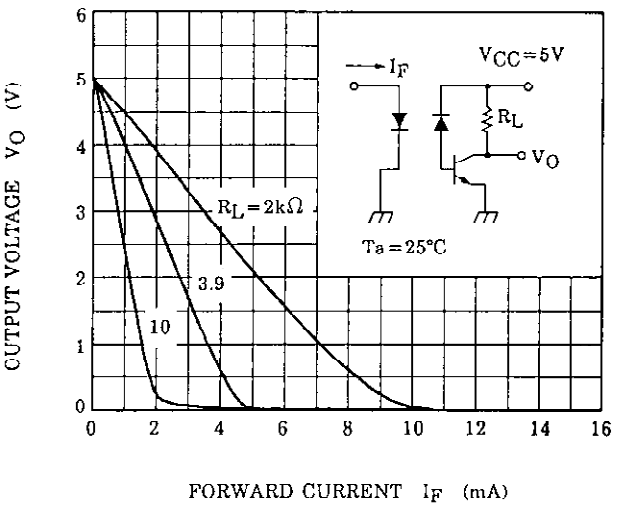
I_O / I_F – Ta



$I_O - V_O$



$V_O - I_F$



$t_{pHL}, t_{pLH} - R_L$