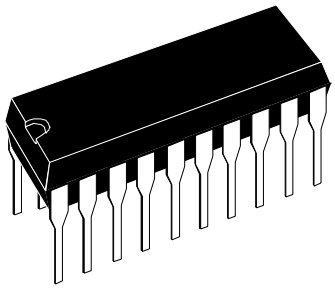
TEA6415C

Bus-Controlled Video Matrix Switch

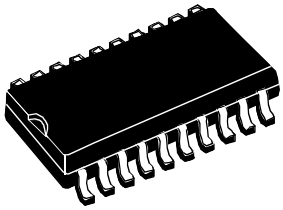
Main Features

- **20 MHz Bandwidth**
- **Cascadable with another TEA6415C (Internal Address can be changed by Pin 7 Voltage)**
- **8 Inputs (CVBS, RGB, Chroma, ...)**
- **6 Outputs**
- **Possibility of Chroma Signal for each Input by switching off the Clamp with an external Resistor Bridge**
- **Bus Controlled**
- **6.5 dB Gain between any Input and Output**
- **-55 dB Crosstalk at 5 MHz**
- **Full ESD Protection**



DIP 20
(Plastic Dual In-line Package

ORDER CODE: TEA6415C



SO 20
(Plastic Small Outline Package)

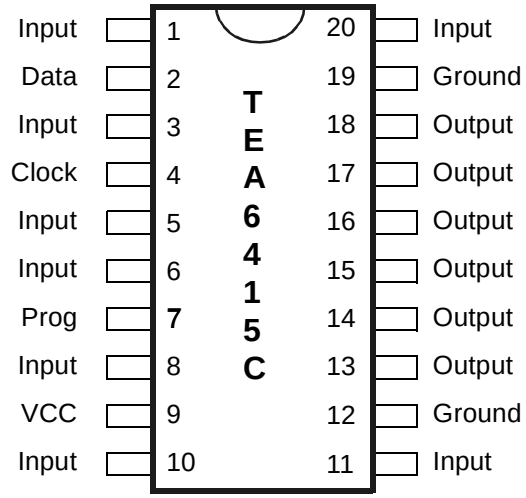
ORDER CODE: TEA6415CD

Description

The main function of the TEA6415C is to switch 8 video input sources on the 6 outputs.

Each output can be switched to only one of the inputs, whereas any single input may be connected to several outputs.

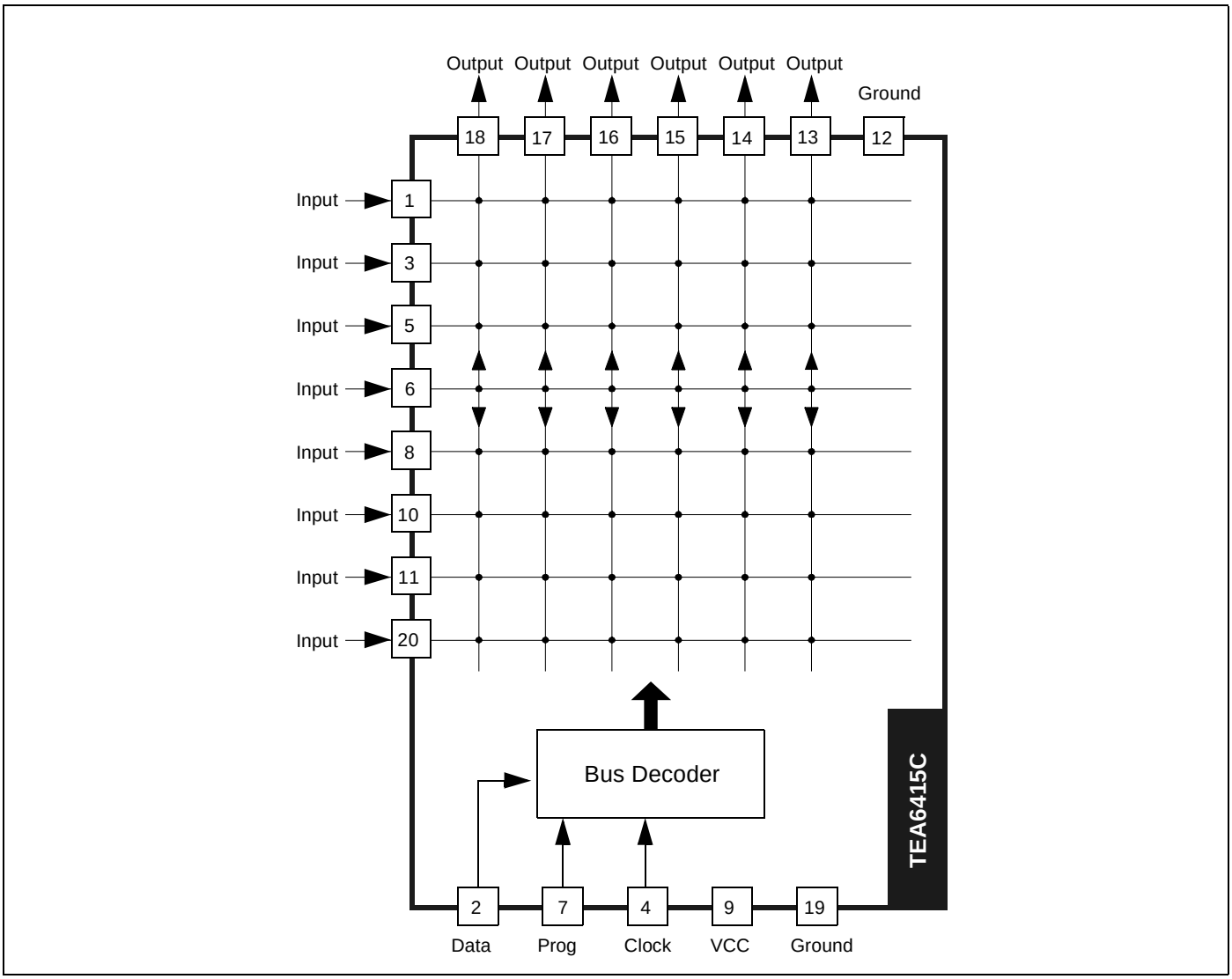
All switching possibilities are controlled through the I^2C bus.



This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

1 General Description

Figure 1: TEA6415C Block Diagram



The main function of the TEA6415C is to switch 8 video input sources on the 6 outputs.

Each output can be switched to only one of the inputs, whereas any single input may be connected to several outputs. The lowest level of each signal is aligned on each input (bottom of sync pulse for CVBS or Black Level for RGB signals).

The nominal gain between any input and output is 6.5 dB. For Chroma signals, the alignment is switched off by forcing, with an external 5 V_{DC} resistor bridge on the input. Each input can be used as a normal input or as a Chroma input (with external resistor bridge). All the switching possibilities are changed through the I²C bus.

Driving a 75 Ω load requires an external transistor.

The switches configuration is defined by words of 16 bits: one word of 16 bits for each output channel.

So, 6 words of 16 bits are necessary to determine the starting configuration upon power-on (power supply: 0 to 10V). But a new configuration needs only the words of the changed output channels.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 9)	12	V
T_A	Operating Ambient Temperature Range	0 to +70	°C
T_{STG}	Storage Temperature Range	-20 to +150	°C

2.2 Thermal Data

Symbol	Parameter		Value	Unit
R_{thJA}	Junction-to-Ambient Thermal Resistance	DIP20 SO20	80 100	°C/W

2.3 Supply

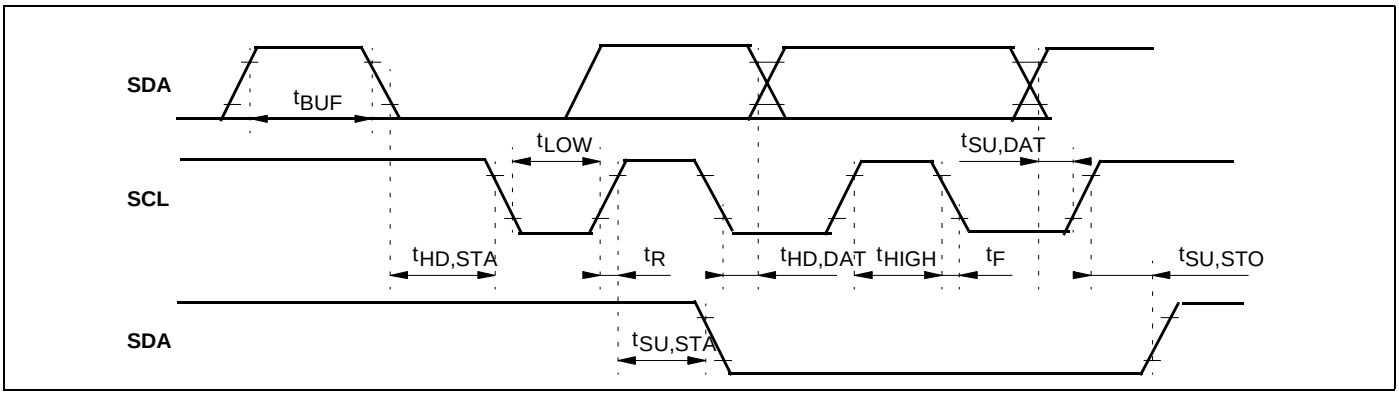
(T_A = 25 °C , V_{CC} = 10 V , R_{LOAD} = 10 kW , C_{LOAD} = 3 pF (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (Pin 9)	8	10	11	V
I_{CC}	Power Supply Current (without load on outputs; V_{CC} = 10 V)	20	30	40	mA
Inputs					
	Signal Amplitude (CVBS signal)			2	V_{PP}
	Input Current (per output connected, input voltage = 5 V_{DC}) (This current is multiplied by 6 when all outputs are connected on the input)		1	3	µA
	DC Level	3.3	3.6	3.9	V
	DC Level Shift (temperature from 0 to 70°C)		5	100	mV
Outputs (V_{IN} = 1 V_{PP} for all dynamic tests) Pins 13,14, 15, 16, 17 and 18					
	Dynamic	4.5	5.5		V_{PP}
	Output Impedance		25	50	Ω
	Gain	6	6.5	7	dB
	Bandwidth -1dB attenuation -3dB attenuation	7	 15 20		MHz
	Crosstalk f = 3.58 MHz f = 5 MHz		 - 55 - 60	 - 45 - 50	dB
	DC level	2.4	2.75	3.1	V
I^2C Bus Input: DATA, CLOCK and PROG (Pins 2, 4 and 7)					
	Threshold Voltage	1.5	2	3	V

2.4 I²C Bus Characteristics

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
SCL					
V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} + 0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	- 10	+ 10	µA
f_{SCL}	Clock Frequency		0	100	kHz
t_R	Input Rise Time	1.5 V to 3 V		1000	ns
t_F	Input Fall Time	3 V to 1.5 V		300	ns
C_I	Input Capacitance			10	pF
SDA					
V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} + 0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	- 10	+ 10	µA
C_I	Input Capacitance			10	pF
t_R	Input Rise Time	1.5 V to 3 V		1000	ns
t_F	Input Fall Time	3 V to 1.5 V		300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA		0.4	V
t_F	Output Fall Time	3 V to 1.5 V		250	ns
C_L	Load Capacitance			400	pF
TIMING					
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
$t_{SU,\ DAT}$	Data Set-up Time		250		ns
$t_{HD,\ DAT}$	Data Hold Time		0	340	ns
$t_{SU,\ STO}$	Set-up Time from Clock High to Stop		4.0		µs
t_{BUF}	Start Set-up Time following a Stop		4.7		µs
$t_{HD,\ STA}$	Start Hold Time		4.0		µs
$t_{SU,\ STA}$	Start Set-up Time following Clock Low-to High Transition		4.7		µs

Figure 2: I²C Bus Timing



2.5 I²C Bus Selections

The I²C chip address is defined by the first byte. The second byte defines the input/output configuration.

Chip Address byte (1st byte of transmission)

86 (hex)	1000 0110 (bin)	When PROG pin is connected to Ground
06 (hex)	0000 0110 (bin)	When PROG pin is connected to V_{CC}

Input/Output Selection byte (2nd byte of transmission)

Table 1: I²C Bus Output Selections

Output Address (MSB)	Input Address (LSB)	Selected Output	
00000	XXX	Pin 18	Output is selected by the 5 MSBs.
00100	XXX	Pin 14	
00010	XXX	Pin 16	
00110	–––	Not Used	
00001	XXX	Pin 17	
00101	XXX	Pin 13	
00011	XXX	Pin 15	
00111	–––	Not Used	

Table 2: I²C Bus Input Selections

Output Address (MSB)	Input Address (LSB)	Selected Input	
00XXX	000	Pin 5	Input is selected by the 3 LSBs.
00XXX	100	Pin 8	
00XXX	010	Pin 3	
00XXX	110	Pin 20	
00XXX	001	Pin 6	
00XXX	101	Pin 10	
00XXX	011	Pin 1	
00XXX	111	Pin 11	

Example: 00100 101 connects pin 10 (input) to pin 14 (output) (equals 25 in hexadecimal)

2.6 Input/Output Pin Configuration Input Configuration

Figure 3: Input Configuration

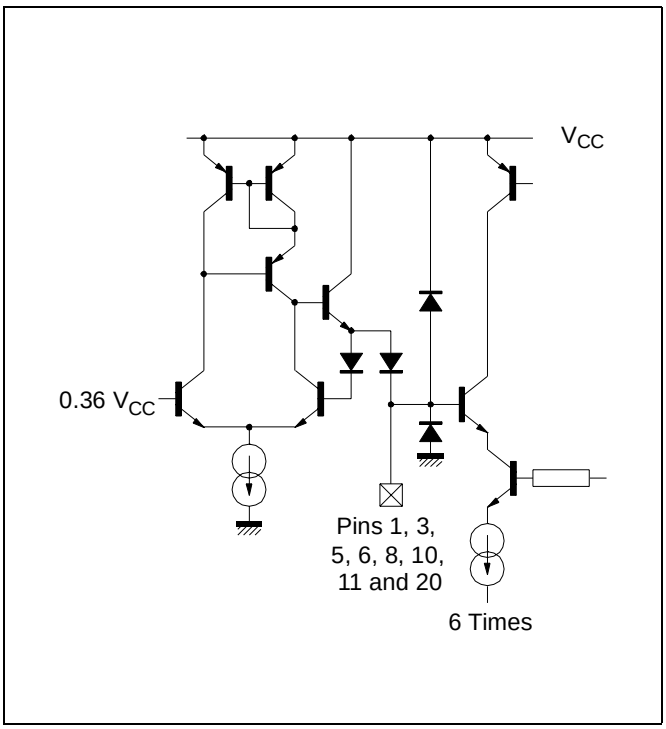


Figure 4: Output Configuration

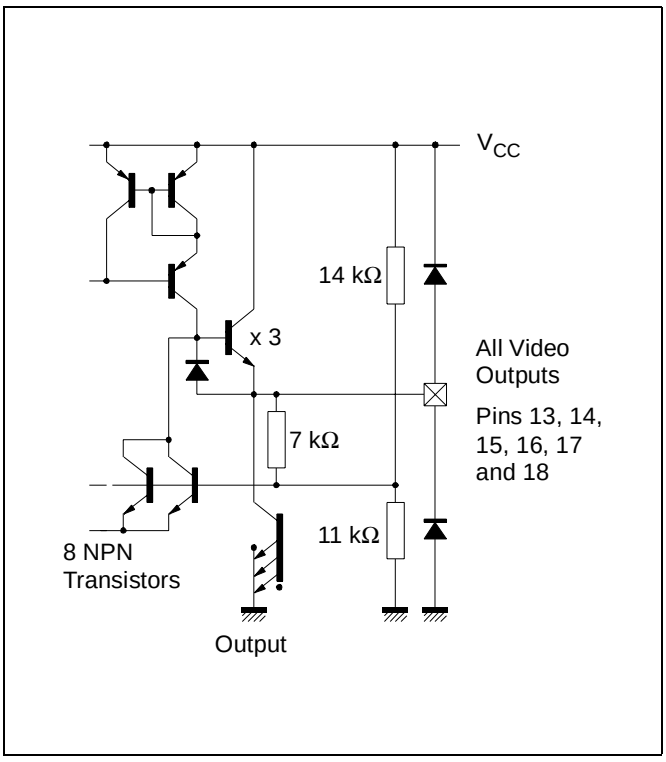


Figure 5: Bus I/O Configuration

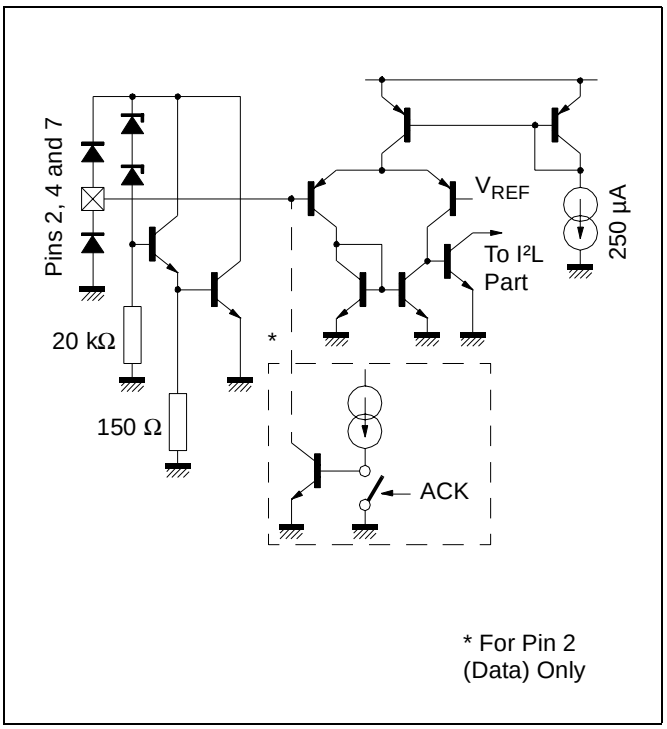
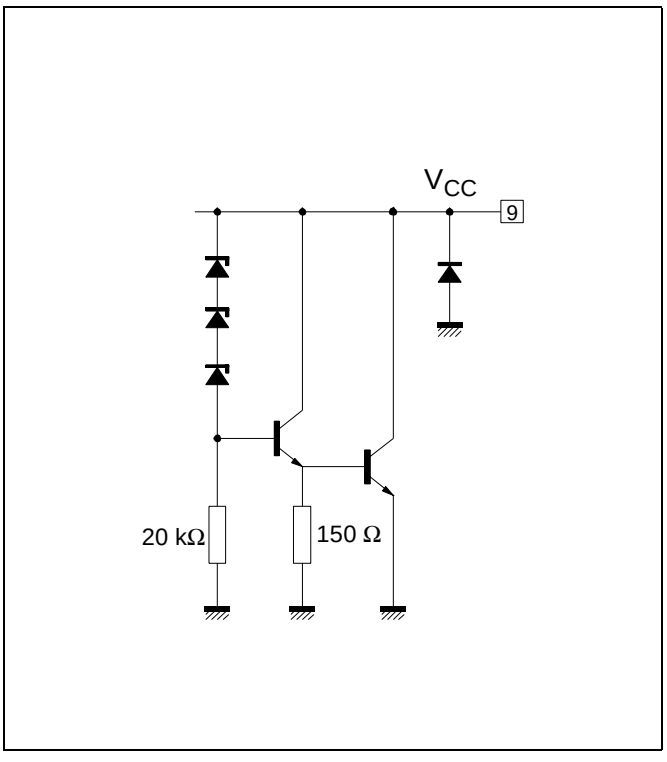


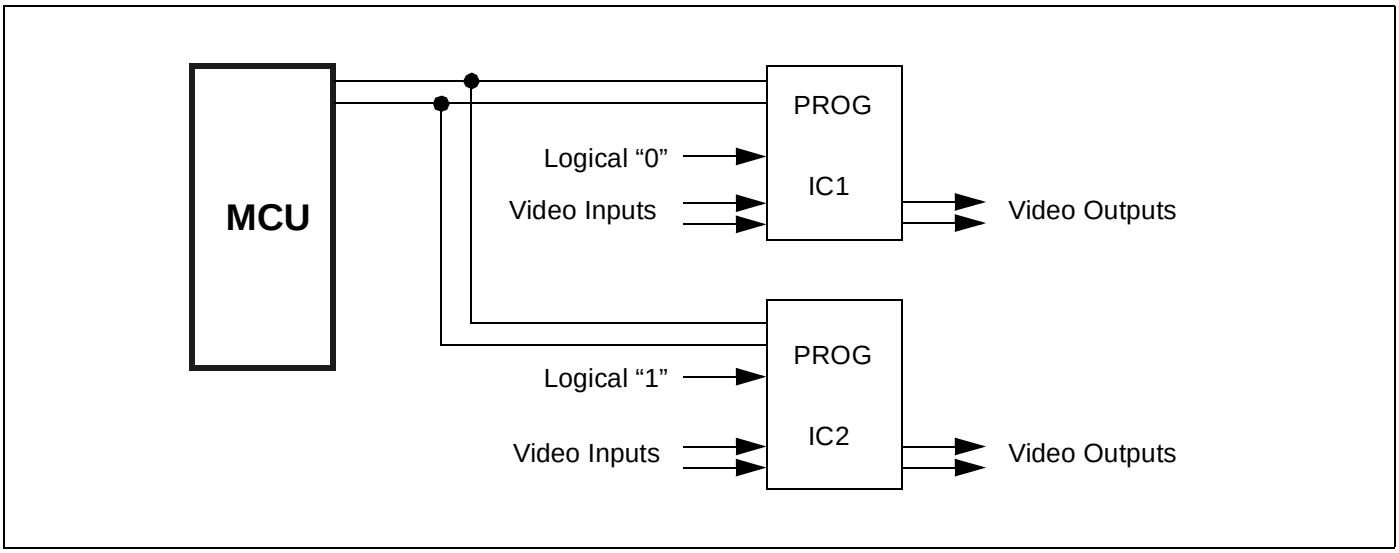
Figure 6: VCC Pin Configuration



2.7 Using a Second TEA6415C

The programming input pin (PROG) allows two TEA6415C circuits to operate in parallel and to select them independently through the I²C bus by modifying the address byte. Consequently, the switching capabilities are doubled, or IC1 and IC2 can be cascaded.

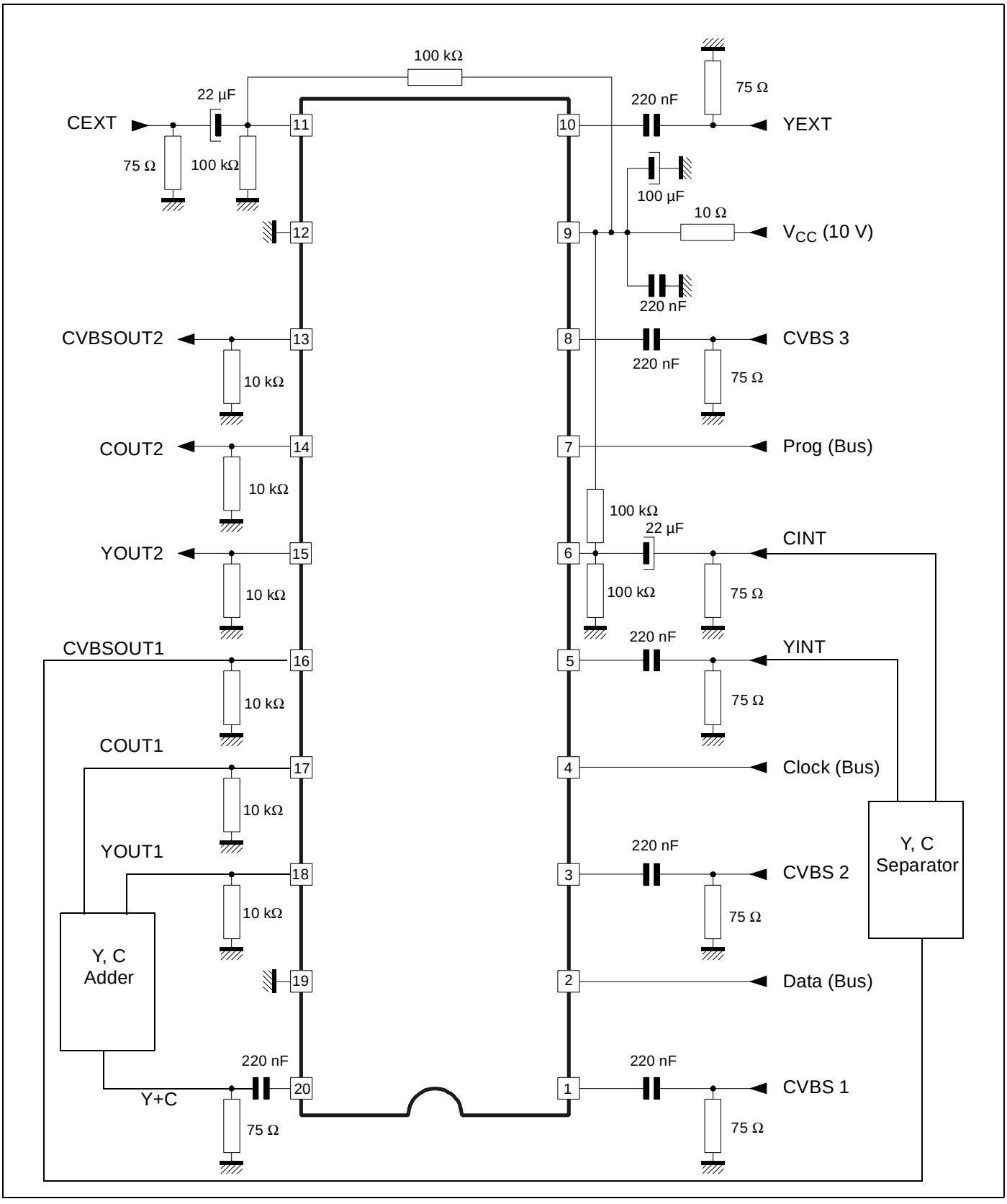
Figure 7: Cascadable TEA6415C Configuration



2.8 Crosstalk Improvement

1. Whenever an input is not used, it must be bypassed to ground through a 220 nF capacitor.
2. Performances can be greatly improved in regards to input crosstalk by using the application example described in the figure below.

Figure 8: Application Diagram Example



3 Package Mechanical Data

Figure 9: 20-Pin Plastic Dual In-Line Package, 300-mil Width

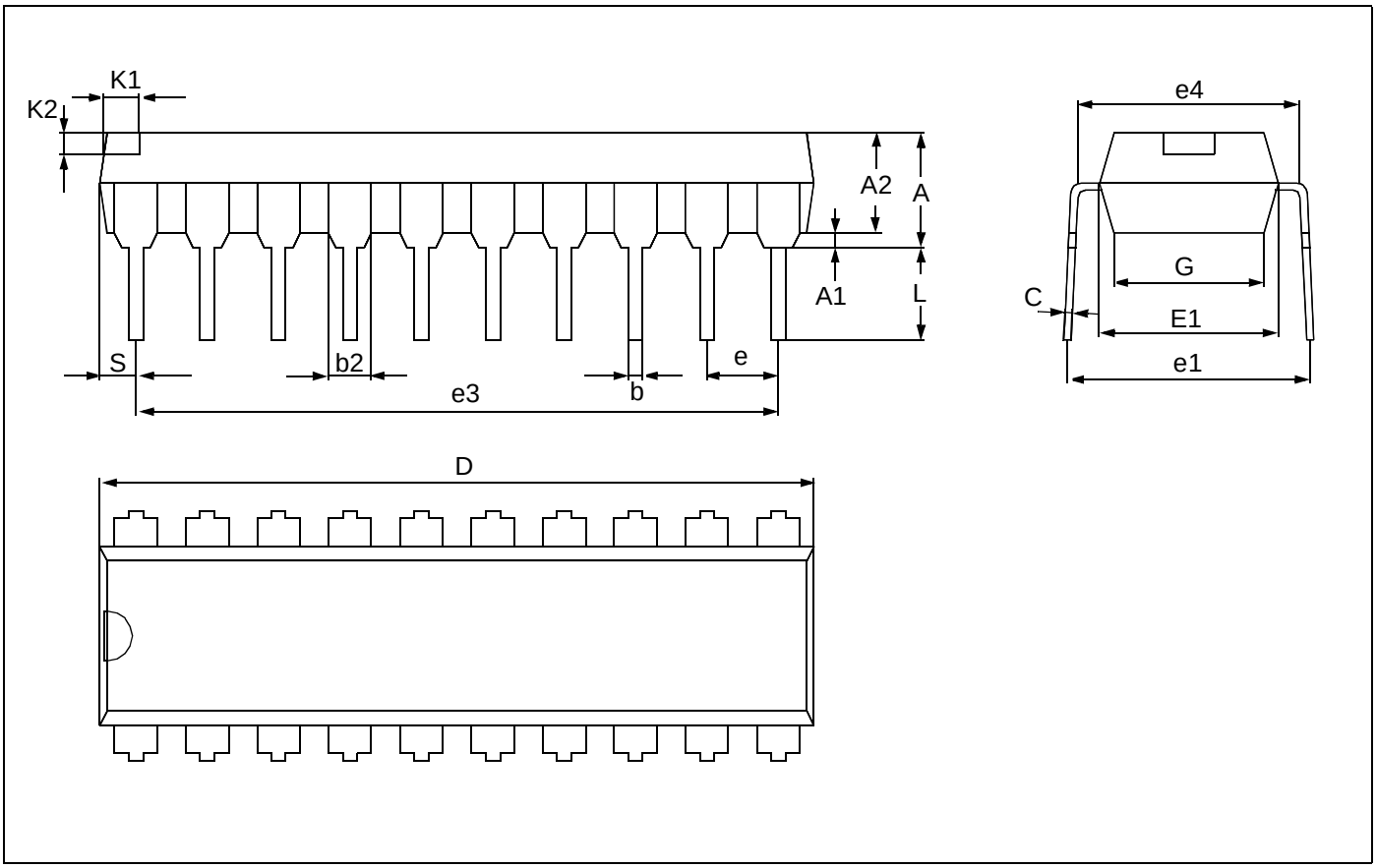


Table 3: DIP20 Package

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	24.89		26.92	0.980		1.060
e		2.54			0.100	
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150
	Number of Pins					
N	20					

Figure 10: 20-Pin Plastic Small Outline Package, 300-mil Width

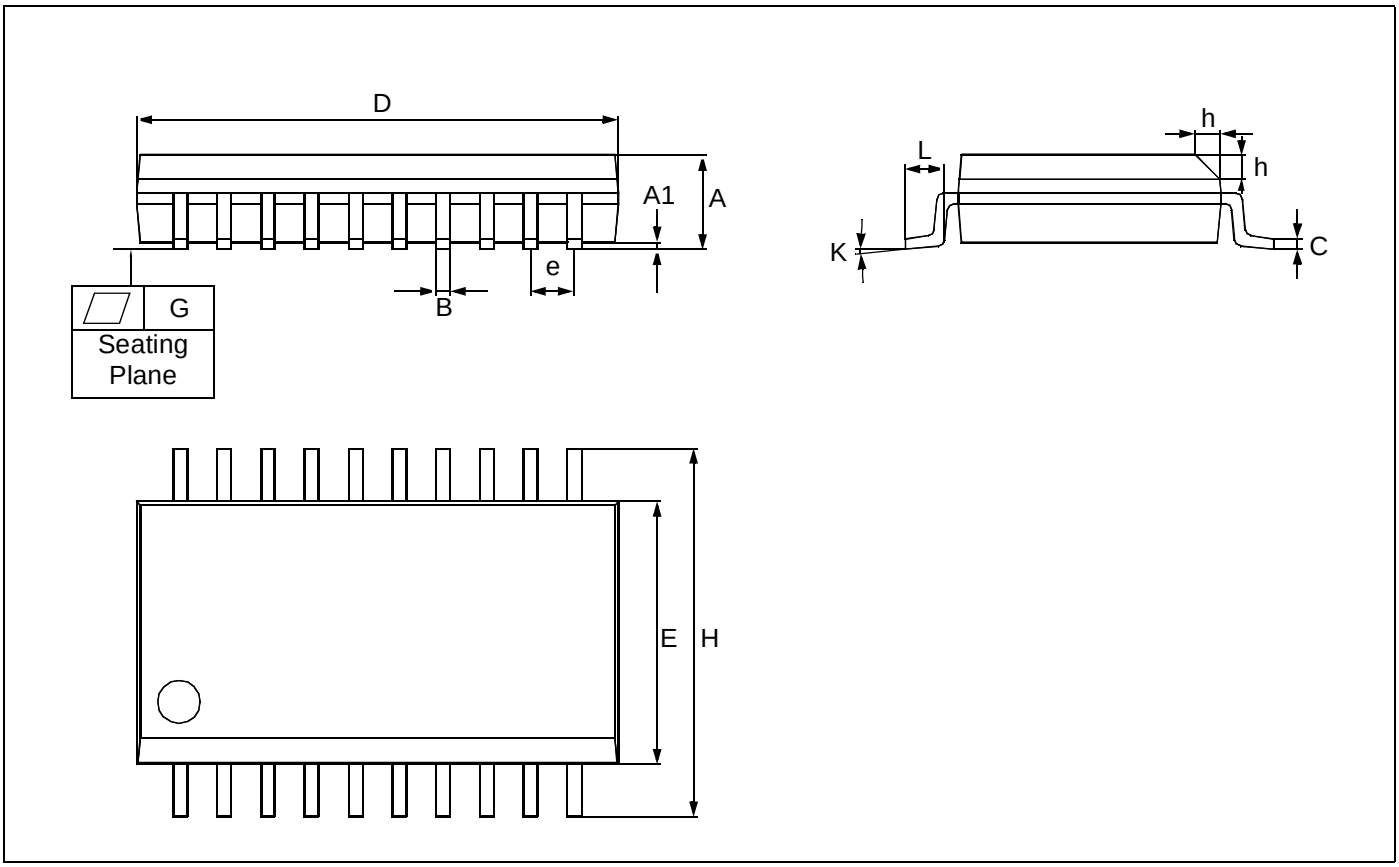


Table 4: SO20 Package

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35		2.65	0.0926		0.1043
A1	0.10			0.0040		
B	0.33		0.51	0.0130		0.0200
C			0.32			0.0125
D	4.98		13.00	0.1961		0.5118
E	7.40		7.60	0.2914		0.2992
e		1.27			0.050	
H	10.01		10.64	0.394		0.419
h	0.25		0.74	0.010		0.029
K	0°		8°	0°		8°
L	0.41		1.27	0.016		0.050
G			0.10			0.004
	Number of Pins					
N	20					

NOTES:

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