Ordering number: EN2704B

Monolithic Linear IC

SANYO No. 2704B

LA6324N, 6324NM

High-Performance Quad Operational Amplifier

Overview

The LA6324 consists of four independent, high-performance, internally phase compensated operational amplifiers that are designed to operate from a single power supply over a wide range of voltages. These four operational amplifiers are packaged in a single package. As in case of conventional general-purpose operational amplifiers, operation from dual power supplies is also possible and the power dissipation is low. It can be applied to various uses in commercial and industrial equipment including all types of transducer amplifiers and DC amplifiers.

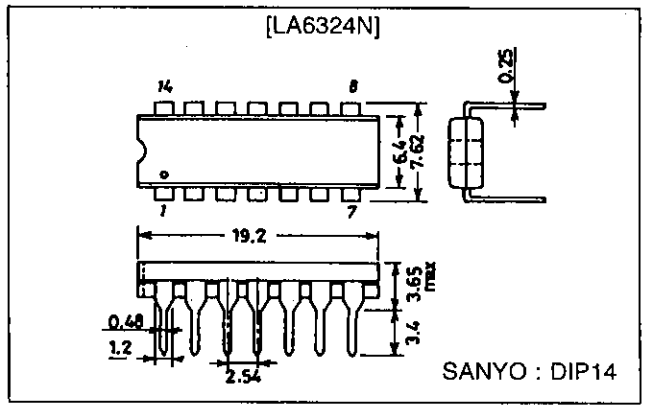
Features

- No phase compensation required
- Wide operating voltage range:
  3.0 V to 30.0 V (single supply)
  ±1.5 V to ±15.0 V (dual supplies)
- Highly resistant to dielectric breakdown
- Input voltage range includes the neighborhood of GND level and output voltage range V_{OUT} is from 0 to V_{CC} – 1.5 V.
- Small current dissipation:
  I_{CC} = 0.6 mA typ/V_{CC} = +5 V, R_L = ∞

Package Dimensions

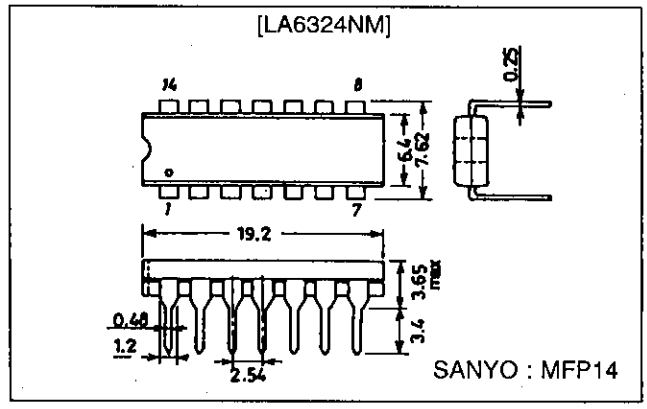
unit : mm

3003A-DIP14



unit : mm

3034A-MFP14



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		32	V
Differential input voltage	V_{ID}		32	V
Maximum input voltage	V_{IN} max		–0.3 to +32	V
Allowable power dissipation	Pd max	LA6324N	720	mW
		LA6324NM	330	mW
Operating temperature	Topr		–30 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

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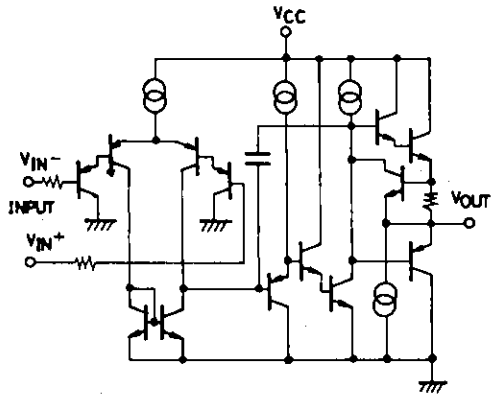
Operating Characteristics at Ta = 25°C, V_{CC} = +5 V

Parameter	Symbol	Conditions	Test circuit	min	typ	max	Unit
Input offset voltage	V_{IO}		1		±2	±7	mV
Input offset current	I_{IO}	$I_{IN}(+) / I_{IN}(-)$	2		±5	±50	nA
Input bias current	I_B	$I_{IN}(+) / I_{IN}(-)$	3		45	250	nA
Common-mode input voltage range	V_{ICM}		4	0		V_{CC} – 1.5	V
Common-mode rejection ratio	CMR		4	65	80		dB
Voltage gain	VG	V_{CC} = 15 V, $R_L \geqq 2$ kΩ	5	25	100		V/mV
Output voltage range	V_{OUT}			0		V_{CC} – 1.5	V
Supply voltage rejection ratio	SVR		6	65	100		dB
Channel separation	CS	f = 1 k to 20 kHz	7		120		dB
Current drain	I_{CC}		8		0.6	2	mA
	I_{CC}	V_{CC} = 30 V	8		1.5	3	mA
Output current (Source)	I_O source	V_{IN}^+ = 1 V, V_{IN}^- = 0 V	9	20	40		mA
Output current (Sink)	I_O sink	V_{IN}^+ = 0 V, V_{IN}^- = 1 V	10	10	20		mA

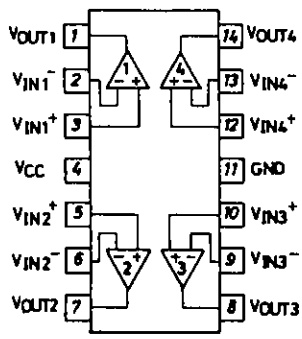
Equivalent Circuit

(1 unit)



Pin Assignment

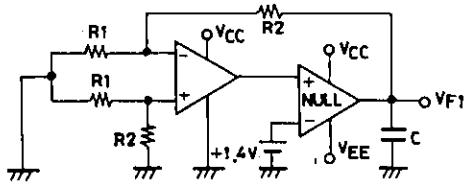
(LA6324N, 6324NM)



Top view

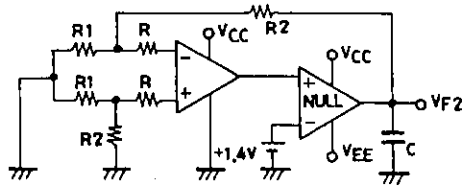
Test Circuit

1. Input offset voltage V_{IO}



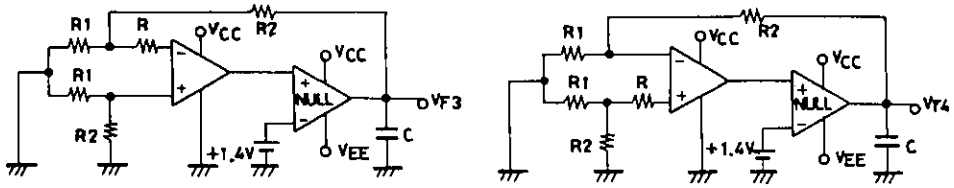
$$V_{IO}=\frac{V_{F1}}{1+R2/R1}$$

2. Input offset current I_{IO}



$$I_{IO}=\frac{V_{F2}-V_{F1}}{R\,(1+R2/R1)}$$

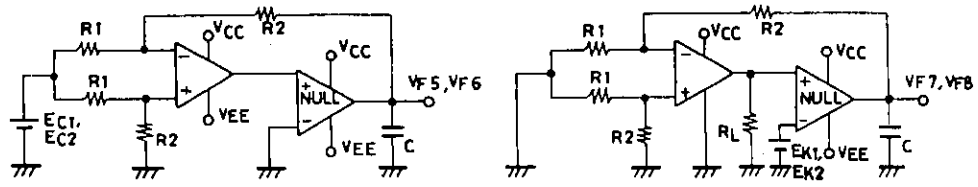
3. Input bias current I_B



$$I_B=\frac{V_{F4}-V_{F3}}{2R\,(1+R2/R1)}$$

4. Common-mode rejection ratio CMR
   Common-mode input voltage range V_{ICM}

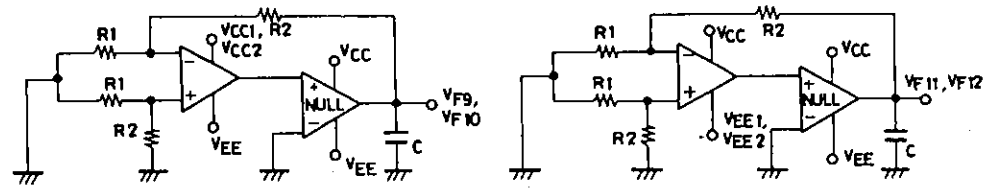
5. Voltage gain VG



$$CMR=20\log\left|\frac{(E_{C1}-E_{C2})\,(1+R2/R1)}{V_{F5}-V_{F6}}\right|$$

$$VG=\frac{(E_{K1}-E_{K2})\,(1+R2/R1)}{V_{F8}-V_{F7}}$$

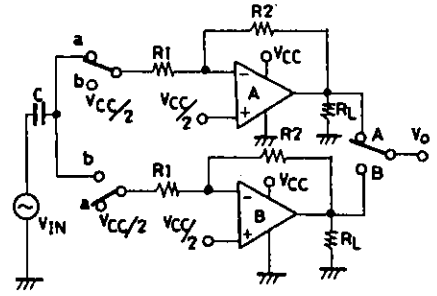
6. Supply voltage rejection ratio SVR



$$SVR\,(+)=20\log\left|\frac{(1+R2/R1)\,(V_{CC1}-V_{CC2})}{V_{F9}-V_{F10}}\right|$$

$$SVR\,(-)=20\log\left|\frac{(1+R2/R1)\,(V_{EE1}-V_{EE2})}{V_{F11}-V_{F12}}\right|$$

7. Channel separation CS



SW: a

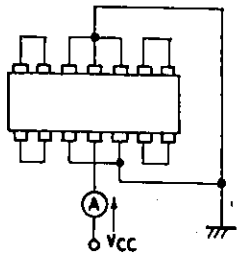
$$CS\,(A\rightarrow B)=20\log\frac{R2}{R1}\frac{V_{OA}}{V_{OB}}$$

SW: b

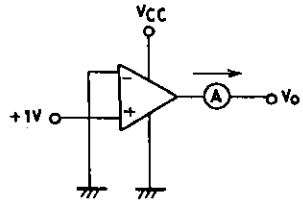
$$CS\,(B\rightarrow A)=20\log\frac{R2}{R1}\frac{V_{OB}}{V_{OA}}$$

These apply also to other channels.

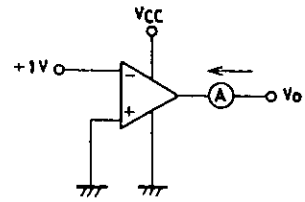
8. Current drain I_{CC}

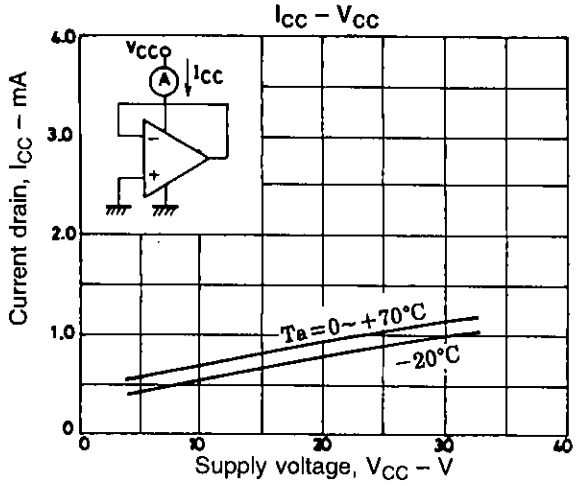


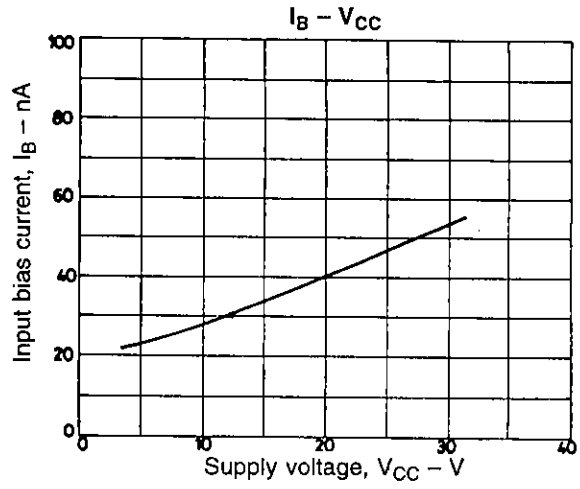
9. Output current I_O source

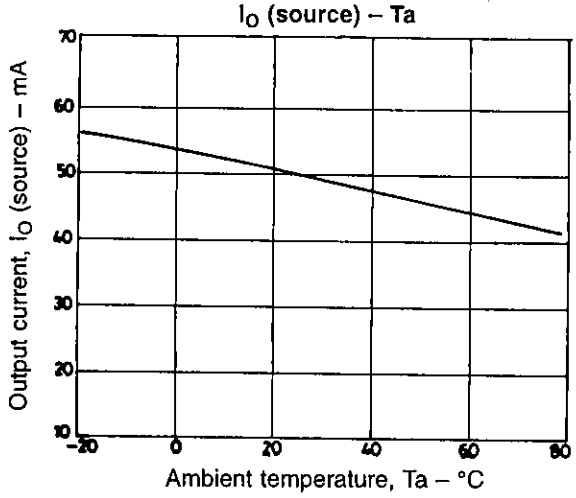


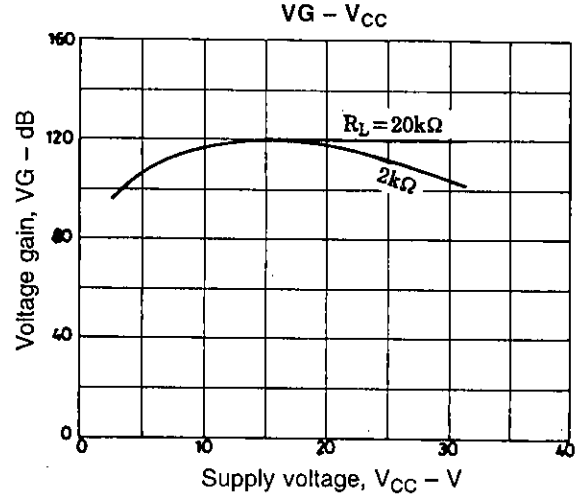
10. Output current I_O sink

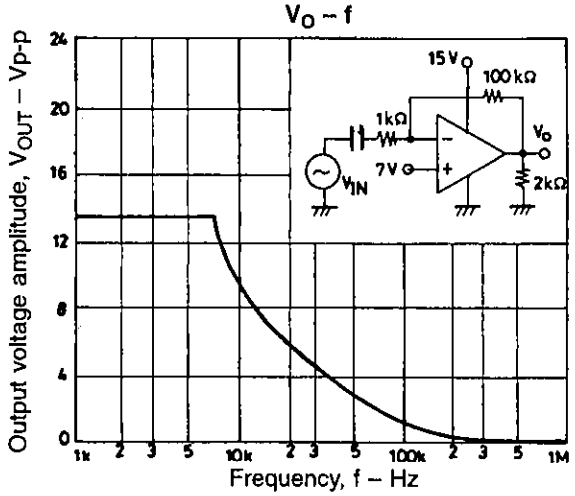


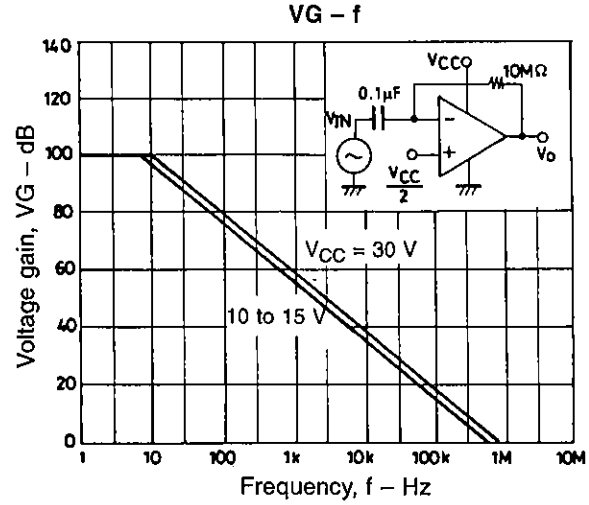


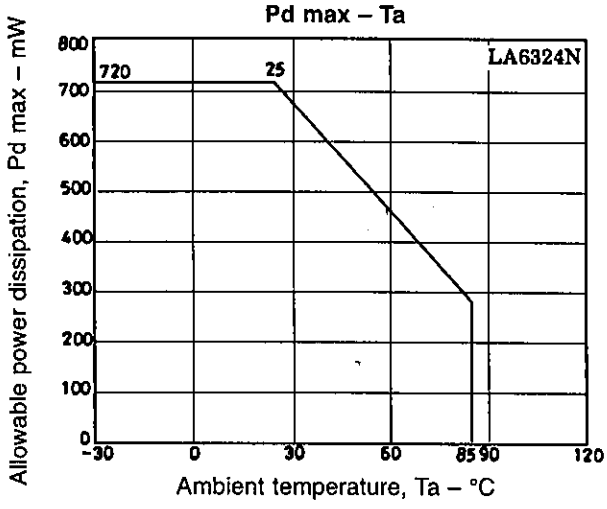


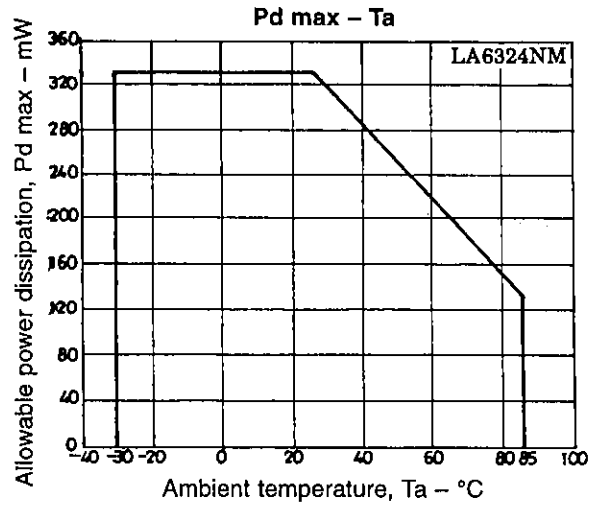






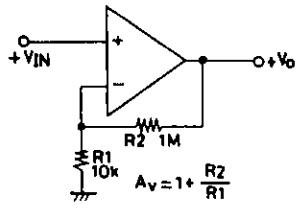




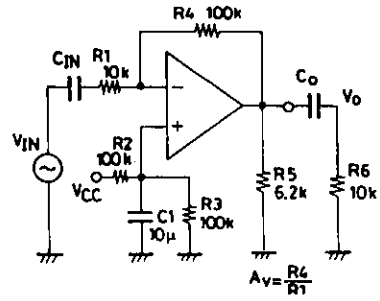


Sample Application Circuits

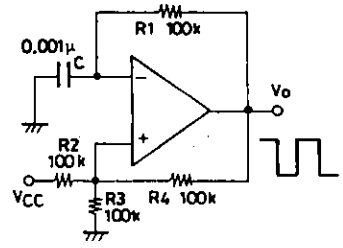
Noninverting DC amplifier



Rectangular wave oscillator



Inverting AC amplifier



Unit (resistance: Ω, capacitance: F)