Packet and Page Teletext data reception using the SAA5250

Authors: *J.R. Kinghorn* *Philips Product Concept & Applications Lab, Southampton England*
A. Guenot *Philips Semiconductors, Paris France*

Revised: *M. T. Schneider* *Philips Product Concept & Applications Lab, California*

SUMMARY

Two methods of transmitting serial data in World System Teletext (WST) format are available. These are the independent data line or 'Packet 31' method, and the page format technique. For universal application in a subscription Teletext environment the receiving equipment must be able to accept both forms of transmission. The Multistandard acquisition circuit CIDAC (SAA5250) or ***C****MOS* ***I****nterface for* ***D****ata* ***A****cquisition and* ***C****ontrol*, is available to simplify the receiver design.

INTRODUCTION

Recently there has been a great upsurge in interest in using Teletext to transmit serial data. This can be achieved without interfering with the normal Teletext service, and the data can be used for many purposes. For instance, a nationwide one way data distribution service could provide customer support for a computer software manufacture, sending both new product announcements, software updates and bug fixes automatically.

At the receiving end, a variety of terminal equipment types can be envisaged depending on the application. A common requirement, however, is for a 'black box' which can be connected to an aerial input signal and deliver a parallel data output to a desktop computer. This unit can be largely transparent to the application, being the equivalent of a data link in a conventional wired computer installation. A block diagram of such an adapter unit is shown in Figure 1**.**

The UHF or VHF aerial signal is passed through the conventional television receiving circuitry of tuner, I.F., and demodulator stages to produce a baseband composite video signal (CVBS). This is applied to the Teletext data slicer and acquisition decoder, which provides a data output to the host computer rather than the usual text display output.

The Teletext decoder can use a microprocessor to format the data output and provide control of the system. Tuning in the local broadcast station and selection of the required service can be done through the controls on the adapter unit, or alternatively by sending commands from the host computer through a suitable interface logic. Facilities for descrambling the data and access control can be provided in the software of the adapter unit or in the host computer according to the particular requirements of a service.

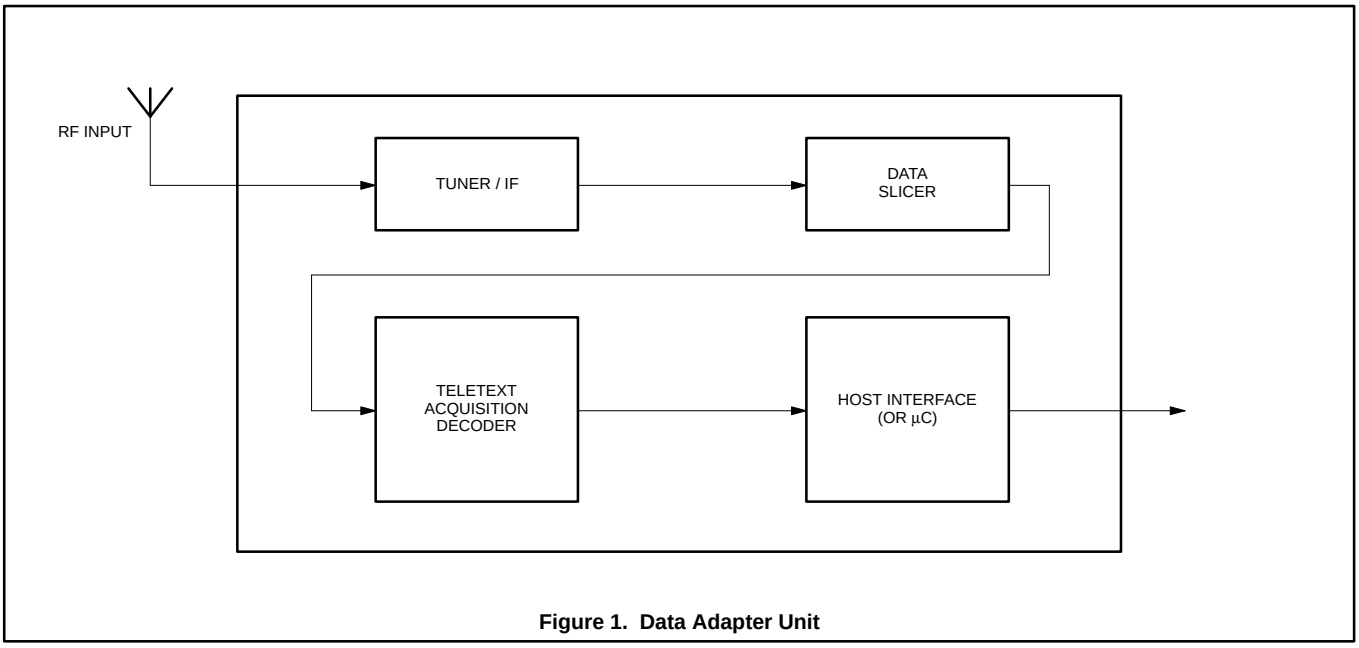


Figure 1. Data Adapter Unit

Packet and Page Teletext data reception using the SAA5250

The Teletext Decoder

As mentioned earlier, the requirements for a Teletext decoder to receive serial data are quite different from a conventional decoder in a television set, or set-top decoder. To begin with, an RGB text display output is not usually required as perfectly adequate character generating capacity is available on the host computer's display. The data output is the main requirement, demanding reasonably direct access to the acquisition memory from the host. Facilities for access control and descrambling the data may be needed, together with special error-checking algorithms.

As a further complication, two entirely different transmission methods are used for serial data; the page format method and the independent data line or 'packet 31' method. Each of these methods has its advantages and disadvantages, but it appears likely that both will be used commercially.

If only page format data reception is required, a standard Teletext decoder chip can be used with appropriate control software, see Reference 1. However, the adapter designer may require a universal decoder capable of operating on either form of transmission. For reasons of economy, duplication of circuitry should be avoided if possible. On the other hand, good performance (i.e. speed) and adaptability may be prerequisites in a competitive design.

The multistandard acquisition circuit CIDAC (SAA5250) provides a solution to these problems. Originally designed for the reception of the French ANTIOPE and the World System Teletext formats, it is equally capable of acquiring data using the independent data line transmission technique. The device can be programmed to operate in various modes and two of these are suitable for the independent data line and the page format transmissions respectively. A block diagram of a multistandard Teletext decoder for serial data is shown in Figure 2.

Composite video is supplied to a standard Philips data slicer (SAA5231 or SAA5191) circuit which performs adaptive data slicing and supplies serial data and clock to the CIDAC (SAA5250). The other section of the data slicer is concerned with display timing synchronization is not used. All of the CIDAC timing is derived from the 5.7273Mhz (6.9375Mhz in 625 line) data clock. Acquisition of the data is performed by the CIDAC circuit (SAA5250).

The received data is buffered in a standard low cost 2K x 8 static RAM connected to the CIDAC. The chip performs appropriate prefix processing according to the operating mode selected, and the storage of particular packets of data is under software control. Data is retrieved from the RAM via CIDAC's parallel interface to a host interface or a microcontroller.

If a microcontroller is used, the microcode is responsible for formatting the data into the form required to interface with the host computer (i.e. an RS-232 serial interface at 9600 baud). The microcontroller itself can be one of several standard types, 8051, 8049, 6801, 6805, etc. Any controls (i.e. to select the service) can be implemented locally in the decoder using port pins of the microcontroller; alternatively if the output interface is made bi-directional, selections can be made using the host computer externally. Access controls and descrambling are dealt with using the appropriate software in the decoder's microcontroller acting on the corresponding received data.

Alternatively, these functions may be performed by the host computer, with the decoder simply acting as a transparent data link and no microcontroller is used in this configuration. The same hardware configuration can be used as a receiver for downloadable software, or as a standard acquisition unit for normal World System Teletext or pages with the host computer used as the display unit.

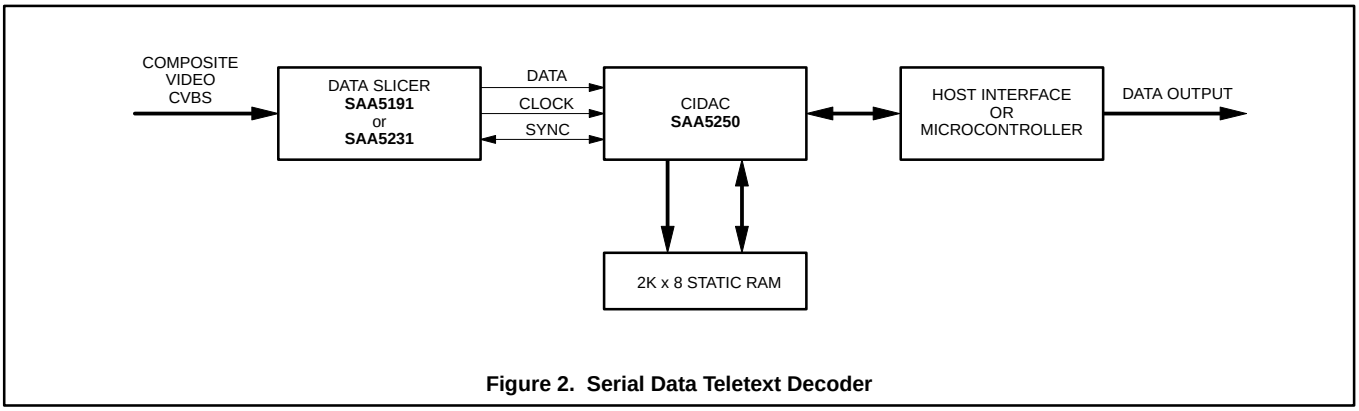


Figure 2. Serial Data Teletext Decoder

Packet and Page Teletext data reception using the SAA5250

The CIDAC Circuit

The CIDAC itself performs the acquisition functions and interfaces with the memory and host. A block diagram of the device is shown in Figure 3.

The received serial data from the data slicer is checked for framing code (which is programmed from the host) during a line timing window derived from the VCS sync signal. This timing window can be moved within limits under software control to compensate for the different framing code delays. After detection of the framing code, the information is converted into 8 bit parallel form. In addition, the VAL OUT output (pin 2) will reflect the position of the programmed framing window.

The functions performed by the data depend on the operating mode selected, and are controlled by the sequence controller circuit.

Some data bytes are *Hamming* protected, and these are passed through Hamming correction logic. Most of the operating modes have hardware recognition of a channel or *magazine*, so the appropriate input data is compared with the requested magazine number in the channel comparator. This ensures that only data from the selected magazines is loaded into memory, and that the acquisition process is not burdened with irrelevant data.

The format counter is used to count the number of bytes loaded into memory on each data line; this value can be loaded by the software. In long and short Didon (ANTIOPE) modes this information is taken from the broadcast format byte via the format transcoder.

Storage of the data in memory also depends on the selection of *slow* or *fast* mode. In slow mode, all data from the selected magazine is stored in memory regardless of any further conditions. It is then up to the host software to search for the appropriate data by looking for a start-of-page flags, packet number recognition, etc. This method is suitable for modest operating speeds such as the packet 31 system, in which the host has no difficulty in keeping up with the overall data throughput.

Alternatively if fast mode is chosen, data is only stored after recognition by the CIDAC hardware of an appropriate 'start-of-page' flag. This flag depends on the system; codes SOH, RS for Didon, a bit in the PS byte for NABTS, or row 0 (page header) for World System Teletext. Using fast mode considerably simplifies the host's task in page recognition, so the position of the data to be checked becomes defined in memory. Fast mode is implemented by page flag detection circuitry in the sequence controller.

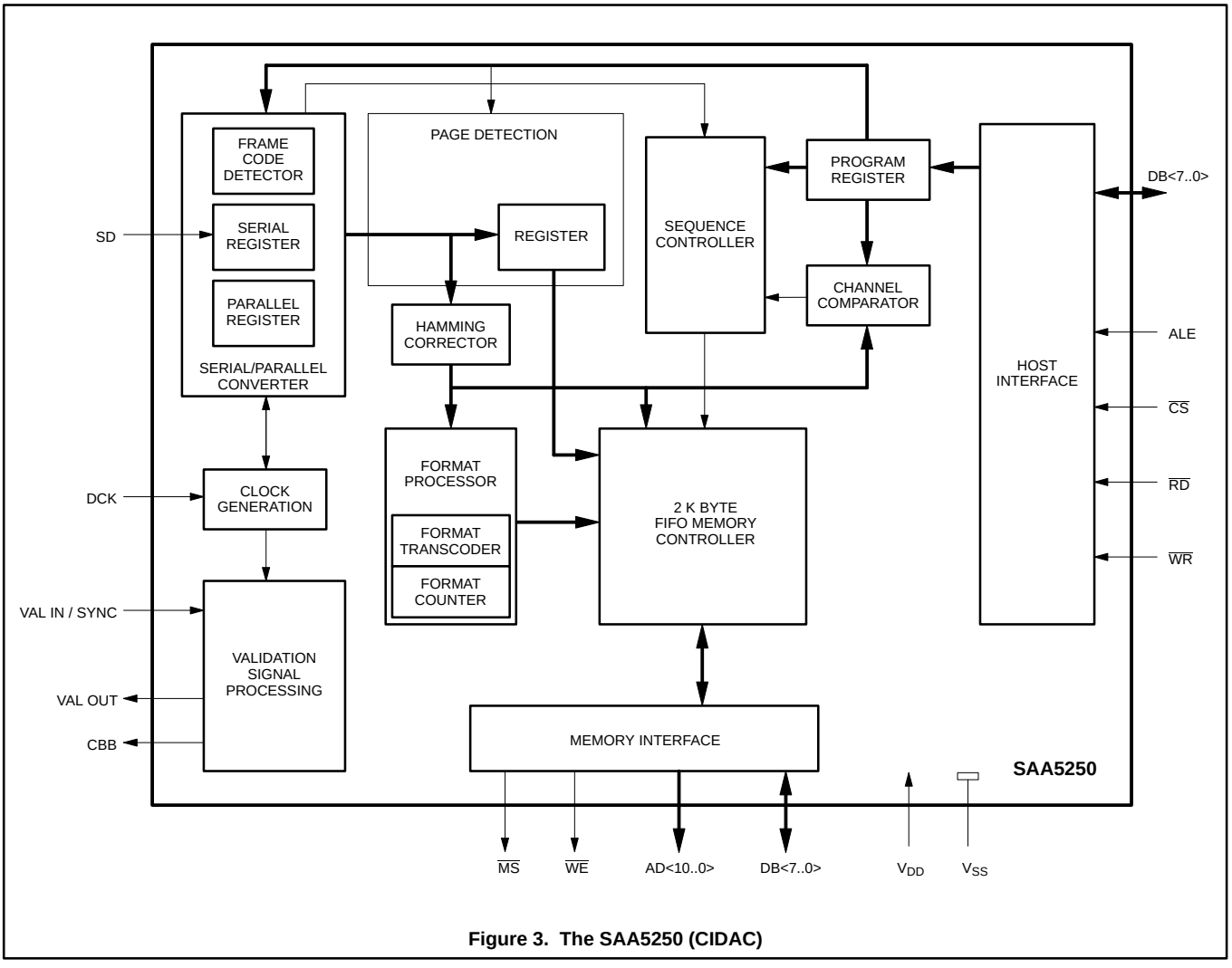


Figure 3. The SAA5250 (CIDAC)

Packet and Page Teletext data reception using the SAA5250

Fast mode is suitable for the page format data transmission method, as the data may be mixed up with a large number of normal teletext pages and interleaved in time. With a suitably fast host, slow mode could be used but it should be remembered that the number of data lines transmitted might increase over time. Also, genuine full channel operation will be impossible in slow mode.

The external 2K x 8 static RAM is used as a first-in-first-out (FIFO) memory so that the transmission order is carefully preserved. Flags associated with the FIFO controller allow the host to see whether the FIFO is empty, has a character for reading, or it is full. Writing to the memory depends on the reception of transmitted data. And a read cycle occurs when it's requested by the host.

The CIDAC memory interface has interleaved read and write cycles clocked at the transmission rate, so in principle the host could read the data as fast as it is coming into the FIFO (Approx. one byte/microsecond). Any standard 2K x 8 Static RAM (i.e. 6116) can be connected to the memory interface and the timing requirements are not very critical.

The interface to the host is an 8 bit parallel bus together with the appropriate handshaking control signals. Data and address are multiplexed on the bus in accordance with normal microprocessor practice. A feature of the CIDAC is the support of a MOTEL (**Mo**torola/In**tel**) parallel (programmable) host interface.

The Intel protocol (i.e., 8051, 8049, etc.) latches the address with ALE, and has separate RD* and WR* pulses for reading and writing respectively. The Motorola protocol (i.e. 6801, 6805) has an AS pulse for latching addresses, a DS pulse every cycle, and a R/W* signal to distinguish read and write cycles.

CIDAC distinguishes between these two protocols by looking at the state of the RD (DS) line during the ALE (AS) pulse and switches over automatically as necessary. This facility permits many types of host interfaces to be connected to CIDAC without extensive interface bus translation components. Communication between the host and CIDAC is *always* initiated by the host.

Since CIDAC does not provide an interrupt function to the host, the host must poll to CIDAC to see when new data has arrived. However, the designer can generate a field interrupt easily by adding only a small amount of external logic.

Various write registers in CIDAC allow the selection of the operating mode, and the loading of the channel number. There are two registers which can be read by the host; the data register (which contains the next byte of data read from the FIFO memory by the CIDAC hardware), and a status register to indicate whether the FIFO memory is empty, normal, or full.

The rate of reading the FIFO depends *entirely* on the host, as it is asynchronous compared to the transmission. However, the software designer must ensure that, on average, the host reads the FIFO at least as fast as the data is arriving, otherwise the buffer can overflow.

Packet and Page Teletext data reception using the SAA5250

Data Formats

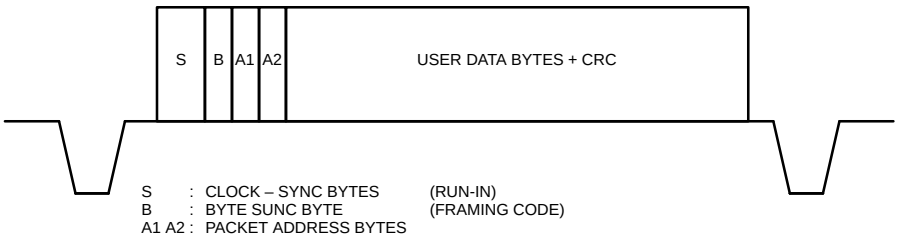
CIDAC is capable of receiving data in various formats, with options for Didon (ANTIOPE), NABTS, and World System Teletext reception. For the purpose of this paper, however, only two operating modes need concern us. These comprise the 'Didon medium prefix slow' mode, used for 'packet 31' transmissions and 'WST fast' mode for page format data reception (previously known as the UK 'CEEFAX' Teletext format).

These data formats are shown in Figure 4.

The Didon medium prefix format (Figure 4a) has simply two channel address bytes after the framing code, followed by user data. The channel bytes are each 8/4 Hamming protected and use the same algorithm for Didon and WST.

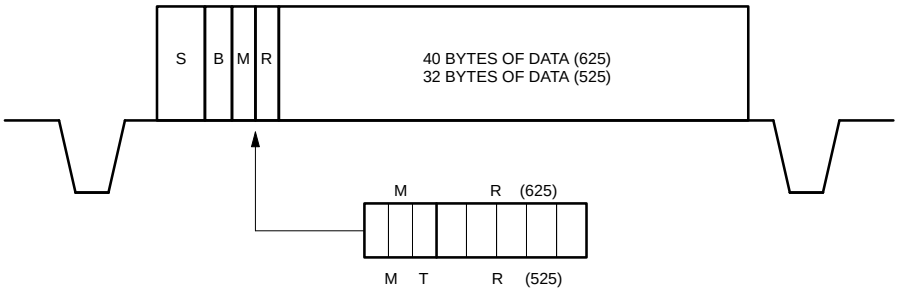
For reception of World System Teletext, CIDAC has a 'WST fast' mode (Figure 4b) with three bits of the first byte used as a channel address or 'magazine' number. The remaining bit and subsequent byte form five bits corresponding to the row address. Detection of the Row 0 (page header) in fast mode is the page flag indicating the storage of subsequent data in the FIFO.

The reception software **must** examine the data at the start of the sequence to determine the page number. If the data is not the desired page, the software arranges a re-initialization of CIDAC to search for the next page header.



S : CLOCK – SYNC BYTES (RUN-IN)
B : BYTE SUNC BYTE (FRAMING CODE)
A1 A2 : PACKET ADDRESS BYTES

(a) DIDON Medium Prefix



S : CLOCK – SYNC BYTES (RUN-IN)
B : BYTE SUNC BYTE (FRAMING CODE)
M, R : MAGAZINE & ROW ADDRESS GROUP
(Tabulation bit also included in 525 line operation)

(b) WST Prefix

Figure 4.

Packet and Page Teletext data reception using the SAA5250

Receiving Datacast

Let us consider the use of CIDAC for receiving packet 31 transmissions in more detail. The Datacast specification (Reference 2) defines four independent data channels using message bits XX01 in the first byte following the framing code. With the second byte set to 1111, this is equivalent to packet 31, or magazine 8,1,2, or 3 in conventional (WST) teletext terms. The format is show in Figure 5.

It will be recalled that CIDAC checks the first two bytes after the framing code in Didon medium Prefix mode, so this provides the means to select the data channel required. All subsequent bytes are stored in the FIFO and need to be processed by the host software. The Format Type byte (**FT**) indicates whether the Packet Repeat (**RI**) or Continuity Indicator (**CI**) bytes are present. Next, the packet Address Length byte (**AL**) indicates to the host how many bytes following are used to identify the packet address.

Following the bytes allotted for the packet address comes the optional Repeat Indicator (**RI**). The RI value indicates the number of times the packet has been transmitted (i.e. first, second, third, etc., repeat of packet). The Continuity Indicator (**CI**) , which is again optional, increments at each transmission of a packet to a given address. This allows the host software to detect the omission of a packet in the sequence.

Following the 'prefix' bytes, there is a sequence of between 28 to 32 (36 in 625 line) user data bytes used to convey the serial data. The data can be represented as either 8 or 7 bit (with parity) data. CIDAC can be set up to enable or disable the parity checking feature. When parity is enabled, the last bit of each byte is used by the software to detect a parity error in the data.

A 16 bit cyclic redundancy check (**CRC**) follows the user data at the end of the packet. This allows the integrity of the user data and the continuity indicator (**CI**) byte to be checked for any errors that may have occurred in transmission. As for the host software, the functions it needs to perform during packet 31 reception fall into three broad categories of operation, they are:

Initialization

The initialization process for the CIDAC will need to select the proper operating mode. An example might be:

– Didon medium prefix slow mode
– No parity checking
– The desired data channel
– A framing code value
– Sync delay time & sync pulse width.

This procedure will cause CIDAC to acquire all packet 31 transmissions for a specified data channel.

Recognition

A software routine must be written to handle the recognition of the desired packet address in the data stream. This involves checking the Address Length (**AL**) and packet address bytes to identify the desired service. If a correspondence is not found, the routine can rapidly unload the incorrect user data bytes from the FIFO (without processing it), before the next data packet arrives and the checking process is restarted.

Formatting & Error Checking

The last step is to handle the formatting and error checking functions once the desired data packet is located. To do this, the routine has to:

– Check the Format Type (FT)
– The Repeat Indicator (RI) byte
– The Continuity Indicator (CI) byte
– Handle CRC check on the Data

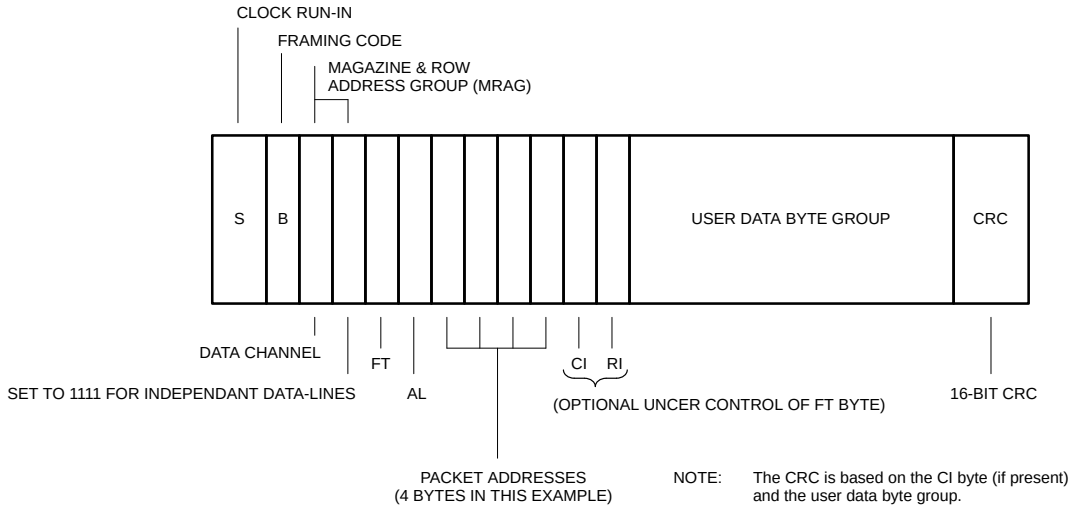


Figure 5. The Datacast Format

Packet and Page Teletext data reception using the SAA5250

If the Repeat Indicator is in use, the software should arrange temporary buffering of the multiple transmissions of data and make a choice on the basis of the comparisons, plus the CRC check, as to which data is valid. The data must only be sent to the host once from the decoder if the proper data sequence is to be preserved. The Repeat Indicator is used by the software routine to ensure that repeated data is not sent out to the host again. A simplified flow chart can be found in Figure 6.

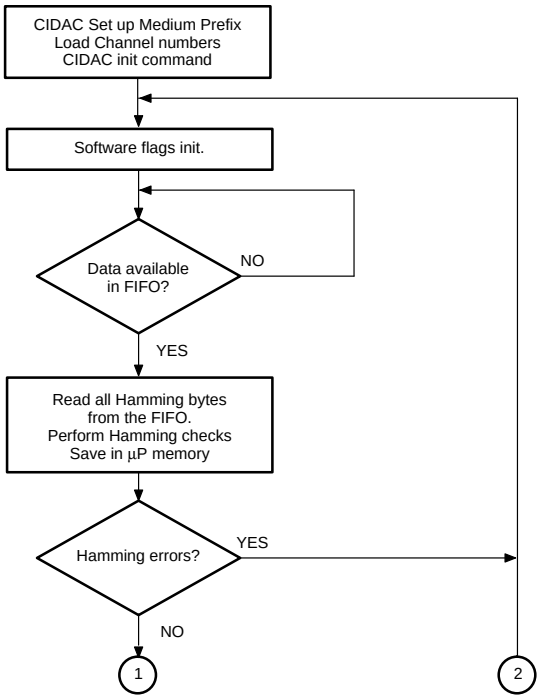


Figure 6. CIDAC Acquisition Flowchart (1 of 2)

Packet and Page Teletext data reception using the SAA5250

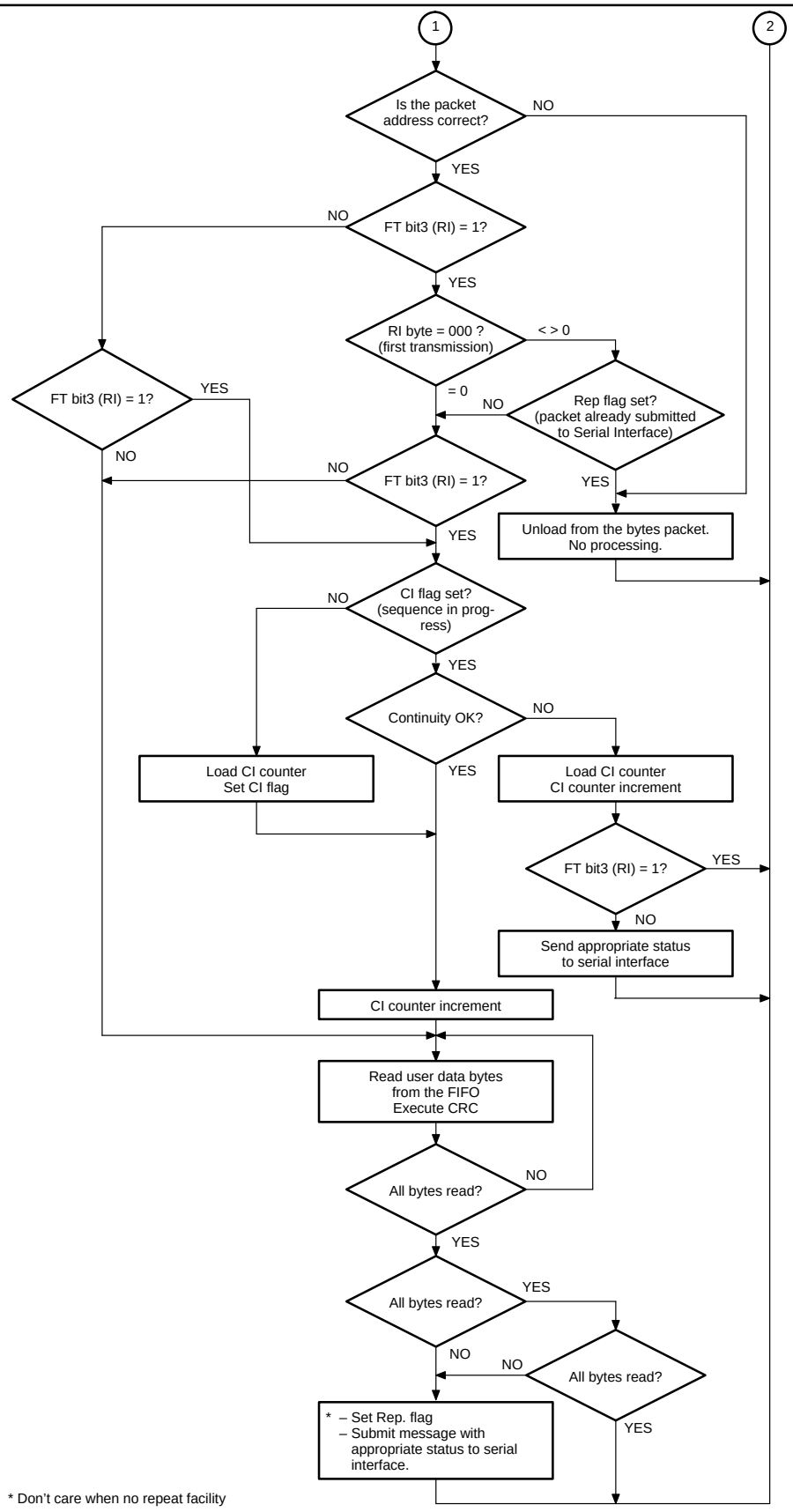


Figure 6. CIDAC Acquisition Flowchart (2 of 2)

Packet and Page Teletext data reception using the SAA5250

CONCLUSION

The CIDAC decoder can form the basis of an acquisition only Teletext decoder operating on both the 'page format' and the 'Packet31' types of transmission. With suitable software, a high performance and efficient design can be achieved.

REFERENCES

1. Tarrant, David R. 'Data Link Using Page-Format Teletext Transmissions', IERE, Electronic Delivery of Data and Software Conference. September 1986.
2. BBC Datacast Technical Specification, 1985.

Special Note: The SAA5243 (CCT) mentioned in Reference 1 is no longer in production. A suitable replacement can be found in the table below:

625 line only

SAA 5244A
SAA 5246A
SAA 5247
SAA 5248
SAA 5249
SAA 5254
SAA 5280

All of the above parts include a built-in data slicer, therefore no need for a SAA5231 data slicer.

525/625 line

SAA 9042 + SAA 5191
SAA5296

RECOMMENDED READING

'World System Teletext and Data Broadcasting System Technical Specification'. December 1987, United Kingdom Department of Trade and Industry, London England.

'Digital Video Signal Processing'. June 1988. Philips Components publication No. 9398 063 30011

Data Sheets for the Philips SAA5191 & SAA5231 Data Slicers (available from your local Philips Semiconductors Salesman).

Data Sheet for the SAA5250 CMOS Interface for Data Acquisition and Control (CIDAC).

Data Book of the I^2C controlled television tuner front-end Modules, Philips Components publication No. 9398 182 50011

Packet and Page Teletext data reception using the SAA5250

APPENDIX A

CIDAC Operating Modes for World System Teletext

1. **WST (CEEFAX) Teletext Mode**

   Set up Magazine number in the 3 LSB's of Register 1.

   SLOW mode: All data from magazine stored.

   FAST mode: All data from magazine stored once Row 0 is detected.

2. **DIDON Medium Prefix Mode (packet 31)**

   Set up magazine number in the 3 LSB's of Register 1.

   Set up Row number in 4th LSB of Register 1 and the 4 LSB's of Register 2.

   SLOW mode: All data from magazine with a specific packet number is stored.

   FAST mode: Not valid for World System Teletext reception.

3. **No Prefix Mode**

   No set up.

   All data of every magazine and packet number is stored.

APPENDIX B

CIDAC Register Address Mapping

Below is the addressing definition for access to the CIDAC registers.

ADDRESS						ADDRESS CIDAC REGISTER
R	W	CS	DB2	DB1	DB0	
H	L	L	L	L	L	Write Register R0
H	L	L	L	L	H	Write Register R1
H	L	L	L	H	L	Write Register R2
H	L	L	L	H	H	Write Register R3
H	L	L	H	L	L	Write Register R4
H	L	L	H	L	H	Write Register R5
H	L	L	H	H	L	Write Register R6 (used for CIDAC init only)
H	L	L	H	H	H	Write Register R7
L	H	L	L	L	L	Read Status Register
L	H	L	L	L	H	Read Data Register
L	H	L	L	H	L	Not Used
L	H	L	L	H	H	Not Used

Packet and Page Teletext data reception using the SAA5250

APPENDIX C

CIDAC Register Organization

CIDAC WRITE REGISTERS

FUNCTION	REGISTER	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
mode & parity	00	X	X	X	mode	parity	prefix2	prefix1	prefix0
format	01	val	fmt2	fmt1	fmt0	fstdgt3	fstdgt2	fstdgt1	fstdgt0
channel number	02	thdgt3	thdgt2	thdgt1	thdgt0	scdgt3	scdgt2	scdgt1	scdgt0
hamming	03	X	X	max5	max4	max3	max2	max1	max0
frame code	04	val7	val6	val5	val4	val3	val2	val1	val0
sync process	05	pol	del6	del5	del4	del3	del2	del1	del0
init register [1]	06	X	X	X	X	X	X	X	X
burst blanking	07	X	X	bst5	bst4	bst3	bst2	bst1	bst0

NOTE:
1. This is a fictitious register. Only the address needs to be accessed to reset CIDAC.

CIDAC READ REGISTERS

FUNCTION	REGISTER	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
FIFO status	00	X	X	X	X	X	DB2	DB1	DB0
FIFO data	01	D7	D6	D5	D4	D3	D2	D1	D0
NOT USED	02	X	X	X	X	X	X	X	X
NOT USED	03	X	X	X	X	X	X	X	X

APPENDIX D

Suggested Data Slicer Components for 625/525 Line Operation

The examples in this application note were designed for operation in both 625 and 525 line Teletext systems. Depending on which line standard is chosen, some of the peripherals commonly around the data slicer need to be adjusted for proper operation. The table below shows these values:

PIN NUMBER	PIN NAME	VALUE WITH SAA5250		VALUE WITH SAA9042	
SAA5191 OR SAA5231		525 LINE	625 LINE	525 LINE	625 LINE
5	Store Amplitude	560 pF	470 pF	560 pF	470 pF
8	Data Timing	470 pF	390 pF	330 pF	270 pF
9	Store Phase	270 pF	220 pF	120 pF	100 pF
11	Crystal	11.4545 MHz	13.875 MHz	11.4545 MHz	13.875 MHz
12	Clock Filter	39 pF	27 pF	39 pF	27 pF

Packet and Page Teletext data reception using the SAA5250

CRYSTAL SPECIFICATION

Quartz Crystal **11.4545MHz** (525 line)
13.875MHz (625 line)

Nominal Frequency	11.4545 MHz
Frequency Tol @ 25°C	+/– 50ppm
Temperature Stability	+/– 30ppm
Temperature Range	–20 to +70°C
Load Capacitance (CL)	15pF
Shunt capacitance (Co)	5 pF typical, 7pF Max.
Motion Capacitance (C1)	19 fF typical
Resonance resistance (Rr)	10 Ohms typical, Max. 60 Ohms
Aging	+/– 5ppm/year
Mode of operation	Fundamental
Drive Level	100 µWatts Correlation

SUPPLIERS

The crystals above can be ordered from the Philips Components Passives Group, the part numbers are:

4322 143 04890 (13.875MHz)

For 11.454, contact Philips Passives.

The Component Passive group can be reached at (803) 772–2500.

The crystals are also available from Ecliptek inc. Their part numbers are:

ECX – 2384 – 11.454MHz

ECX – 2383 – 13.875MHz

ECX – 2382 – 13.500MHz (not used with the SAA5250, but listed for reference)

Ecliptek can be reached at (714) 433–1200. The contact sales representative is Mr. Rodney Mills.