SIEMENS

TV Stereo Decoder with Matrix — TDA 6600-2

Preliminary Data — **Bipolar IC**

The TDA 6600-2 includes an advanced decoder for the identification signals for the multichannel TV sound systems according to the dual-carrier system as well as a matrix switched by the decoder to provide the L-R-information.

Features

- Increased switching reliability and recognition by means of two PLLs for stereo (117 Hz) and / or dual channel (274 Hz)
- Separate bandwidth selection for dual-tone (pins 17-18) and stereo (pins 14-15)
- Separate setting for the PLL time constants for dual-tone (pin 10) and stereo (pin 11)
- Adjustable cut level for dual-tone (pin 8) and stereo (pin 9)
- Cross-talk rejection independent of external component accuracy
- Adjustment to minimal cross-talk level through external DC voltage
- Suitable for TV sets with a 15625-Hz signal.

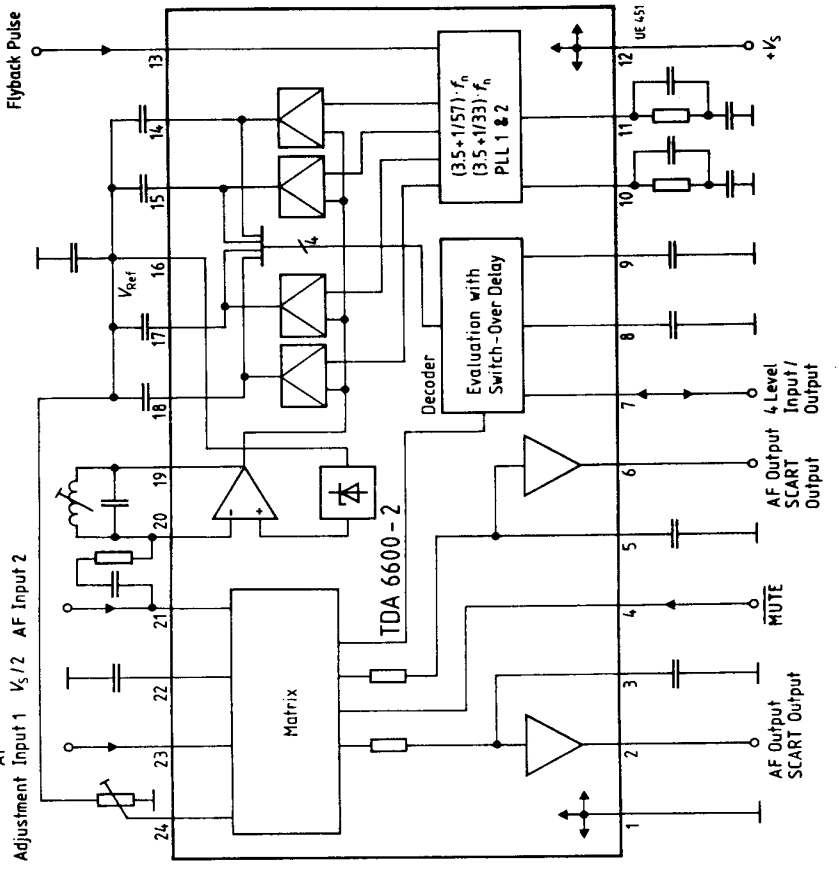
Type	Ordering Code	Package
TDA 6600-2	Q67000-A8210	P-DIP-24

Circuit Description

The circuitry has two functional sections:

1. A pilot frequency decoder including the following circuitries:
   Two phase locked loops for generating the required comparison frequencies (54.96 kHz and 54.8 kHz) from the line frequency. The phase detectors of the control loops operate in a frequency range of 117 Hz and/or 274 Hz.
   Four demodulators to evaluate the 54-kHz pilot signal. The capacitors at the mixer outputs determine the bandwidth (and thus the signal-to-noise ratio) of the pilot tone recognition.
   An evaluation circuitry for decoding "stereo", "dual sound", and "mono" from the mixer output levels. In order to assure interference-free operation in case of high noise level input signals, the individual signals "stereo" and "dual sound" are delayed via an externally adjustable integrator. The subsequent digital evaluation provides the information "mono", "dual sound", or "stereo" to the matrix and the 4 level input/output (to drive the TDA 6200). If this four level input/output is connected to ground externally (e.g. by the TDA 6200), the decoder will recognize this signal as "forced mono".
2. A stereo matrix with deemphasis and SCART output switched by the pilot frequency decoder. The SCART output can be disabled by a MUTE signal (coincidence).

Block Diagram

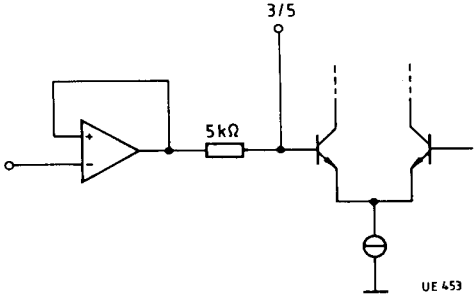


Pin Functions

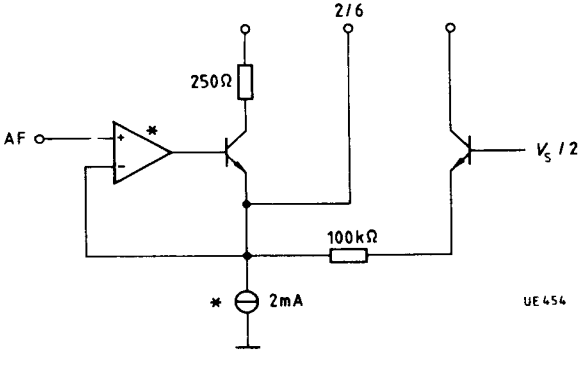
Pin No.	Function
1	Ground
2	AF output/SCART output left channel
3	Deemphasis left channel
4	$\overline{\text{MUTE}}$ input
5	Deemphasis right channel
6	AF output/SCART output right channel
7	4 level input/output
8	Integrator (dual sound)
9	Integrator (stereo)
10	PLL filter (dual sound)
11	PLL filter (stereo)
12	+ V_S (supply voltage)
13	Input line flyback pulse
14	Mixer output (stereo)
15	Mixer output (stereo)
16	Reference voltage
17	Mixer output (dual sound)
18	Mixer output (dual sound)
19	54-kHz filter
20	54-kHz input
21	AF input 2
22	V_S / 2
23	AF input 1
24	Crosstalk adjustment

Pin Descriptions and Functions

De-Emphasis (pin 3, 5)

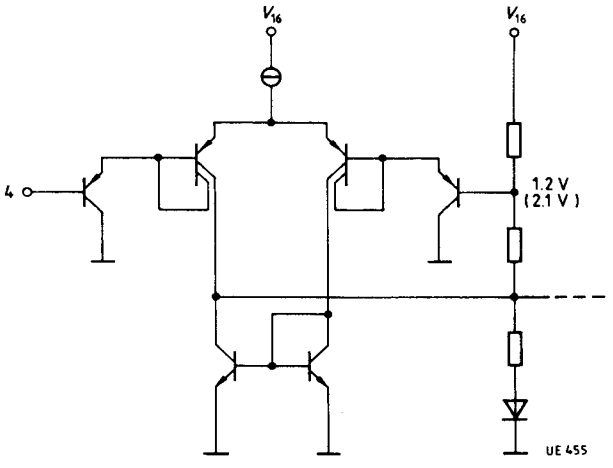


AF Output (pin 2, 6)

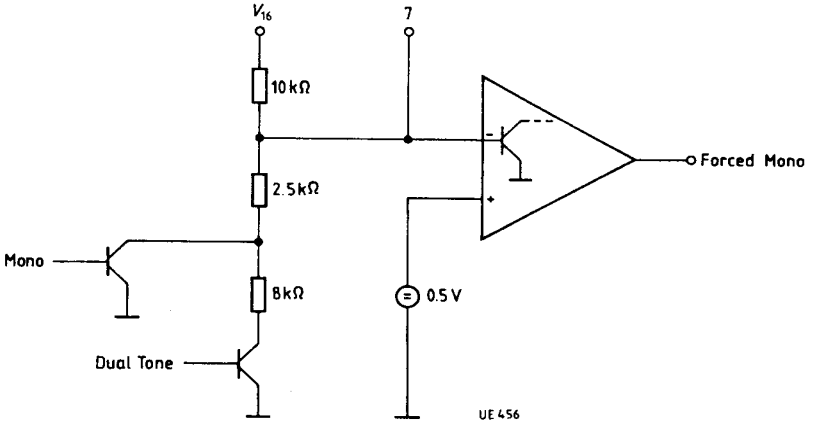


*With $\overline{\text{MUTE}}$ the power supply is switched OFF

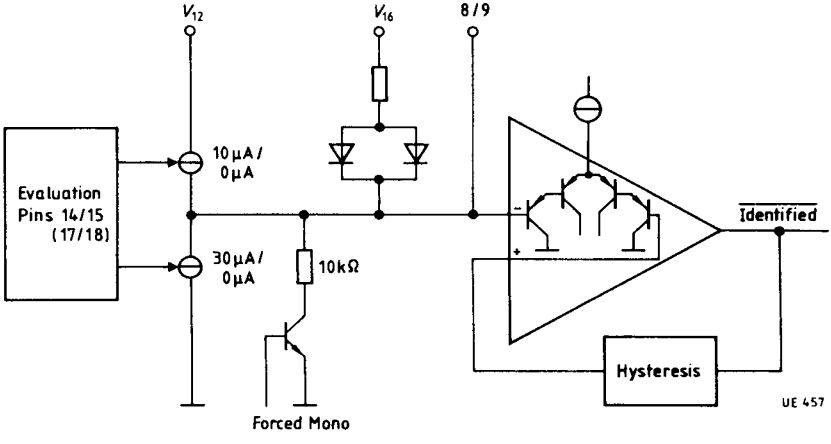
$\overline{\text{MUTE}}$ Schmitt-Trigger (pin 4)



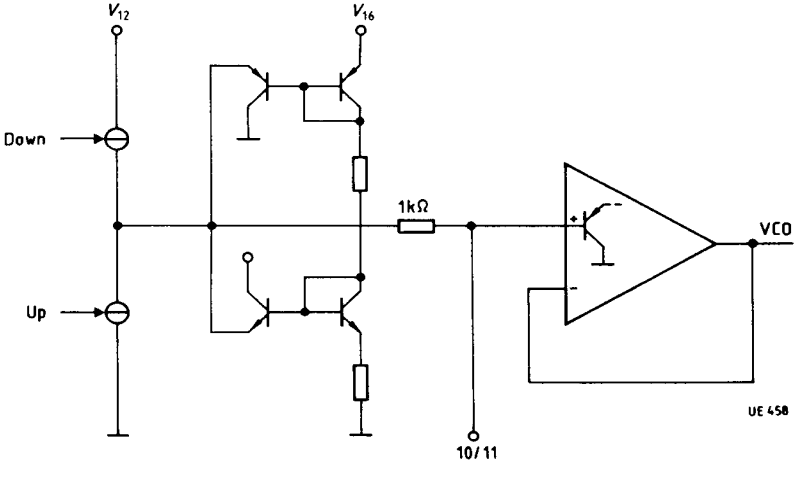
4 Level Input / Output (pin 7)



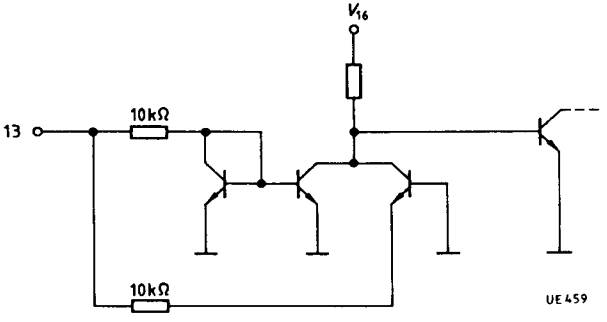
Integrator (pin 8, 9)



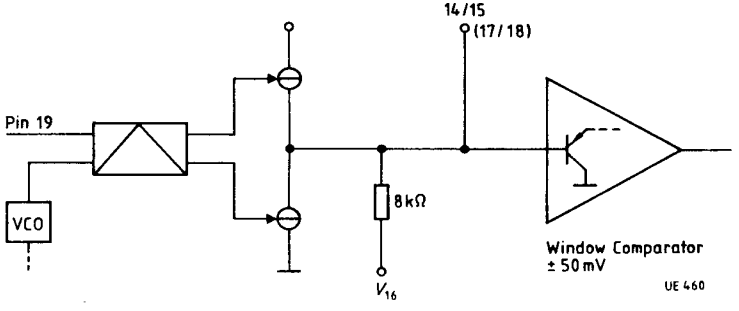
PLL Filter Point (pin 10, 11)



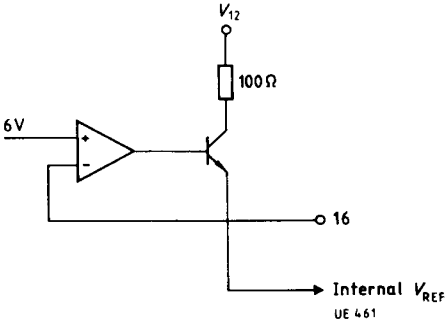
Synchronizing Pulse Input (pin 13)



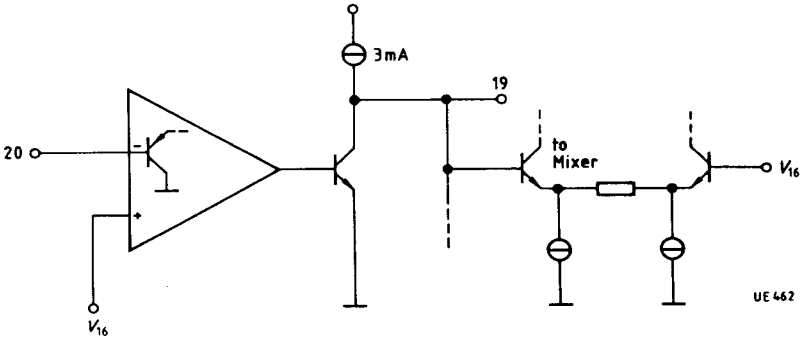
Mixer Outputs (pin 14, 15, 17, 18)



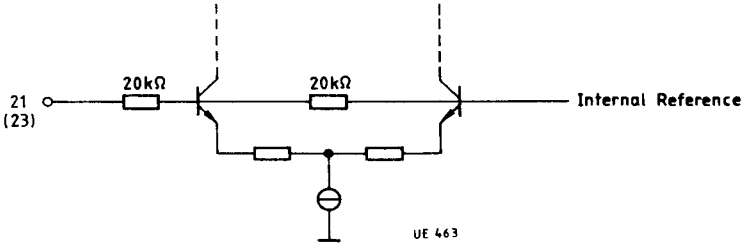
Reference Voltage (pin 16)



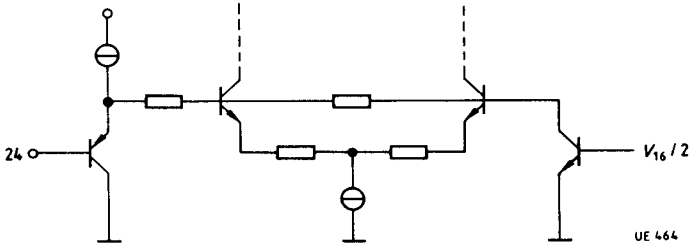
Operational Amplifier (pin 20, 19)



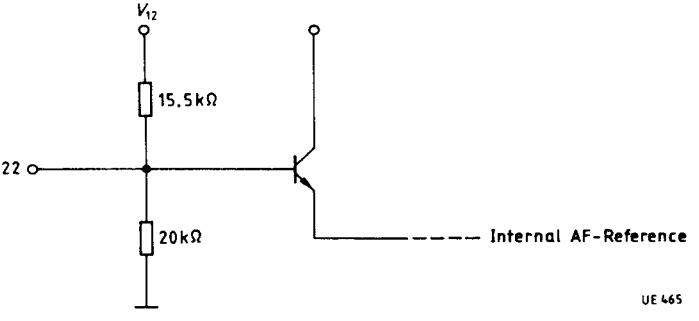
AF Inputs, Channels 1 and 2 (pin 21, 23)



Stereo Compensation (pin 24)



V_S/ **2** (pin 22)



Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	– 0.5	16.5	V
Input Voltage				
Line flyback pulse	V_{13}	$-V_S$	$+V_S$	V
54-kHz input; MUTE	V_{20}; V_4	– 0.5	$+V_S$	V
AF input 1, 2	V_{23}; V_{21}	– 0.5	$+V_S$	V
Crosstalk adjustment	V_{24}	– 0.5	$+V_S$	V
Output Voltage				
Deemphasis L, R	V_3; V_5	– 0.5	$+V_S$	V
V_S / 2; 4 level input/output	V_{22}; V_7	– 0.5	$+V_S$	V
Reference voltage	V_{16}		8	V
Mixer outputs	V_{14}; V_{15} V_{17}; V_{18}	– 0.5	$+V_S - 2$	V
Output Currents				
AF output L, R	I_2; I_6	– 4	4	mA
Integrators	I_8; I_9	– 1	1	mA
PLL filter	I_{10}; I_{11}	– 1	1	mA
Reference voltage	I_{16}	– 4	4	mA
54-kHz filter	I_{19}	– 4	4	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistances (system-air) (system-case)	 $R_{th\,SA}$ $R_{th\,SC}$	 64		K/W

Operating Range

Supply voltage	V_S	10	15.8	V
Temperature range	T_A	0	70	°C

Characteristics
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current consumption	I_{12}	20	36	50	mA		1
Reference voltage	V_{16}	5.4	6	6.6	V		1
$V_S/2$	V_{22}	6.1	6.8	7.4	V	V_S = 12 V	1
Matrix Section							
Max. AF input voltage	$V_{21};V_{23}$	2			V_{rms}	$THD \leq 2\%$ f_I = 1 kHz	2
Total harmonic distortion factor	THD_2 / THD_6			1	%	V_I = 1 V_{rms} f_I = 1 kHz	2
Gain (V_{OFF} / V_{ON})	$V_2;V_6$		0		dB	$V_{24} = V_{16}/2$ V_I = 300 mV, 1 kHz without deemphasis capacitor	2
Adjustable gain difference channel1/channel2	ΔV		± 6		dB	V_I = 300 mV, 100 Hz V_{24} = 0 V/ V_{16} without deemphasis capacitor	2

Characteristics (cont;d)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Crosstalk Attenuation							
Mono		60	75		dB	decoder recognizes mono V_{I23}= 0V V_{I21}= 2Vrms 1kHz	2
Dual sound		60	75		dB	decoder recog. dual sound $V_{I use}$ = 0Vrms $V_{I interfer}$ = 2Vrms 1 kHz	2
Stereo		30	40		dB	decoder recognizes stereo $V_{I23} = V_{21} / 2$ V_{I21} = 2 Vrms 1 kHz crosstalk adjusted to	3
Input current pin 24 (stereo adjustment)	$-I_{24}$		3	15	µA	$V_{24} = V_{16}$	1
MUTE input level "HIGH" (AF is switched on)	V_4	2.5			V		2
"LOW"	V_4	0		0.7	V		2

Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Input current pin 4	$-I_4$			10	µA	V_4 = 0 V	2
Signal-to-noise voltage unweighted according DIN 45405	V_2, V_6		50	100	µV rms	$V_{24} = V_{16}$ / 2 V_4 = 6 V $V_{I\,21} = V_{I\,23}$ =0V rms (decoder recognizes mono or dual tone)	2
Signal-to-noise voltage unweighted according DIN 45405	V_2, V_6		90	140	µV rms	$V_{24} = V_{16}$ / 2 V_4 = 6 V $V_{I\,21} = V_{I\,23}$=0V rms (decoder recognizes stereo)	2
Signal-to-noise ratio measured with mono or dual tone	SNR	69	75		dB	$V_{I\,rms}$= 300 mV; V_4 = 6 V: $V_{24} = V_{16}$ / 2	2
DC jump of output voltage during switch-over of decoder	V_2, V_6			300	mV		2

Design-Related Data

Input impedance	$R_{I\,21;23}$	20	40		kΩ	
Output impedance	$R_{Q\,2;6}$			200	Ω	V_4 = 6 V
Output impedance	$R_{Q\,2;6}$		100		kΩ	V_4 = 0 V
Deemphasis resistance	$R_{3;5}$	3.5	5	6.5	kΩ	

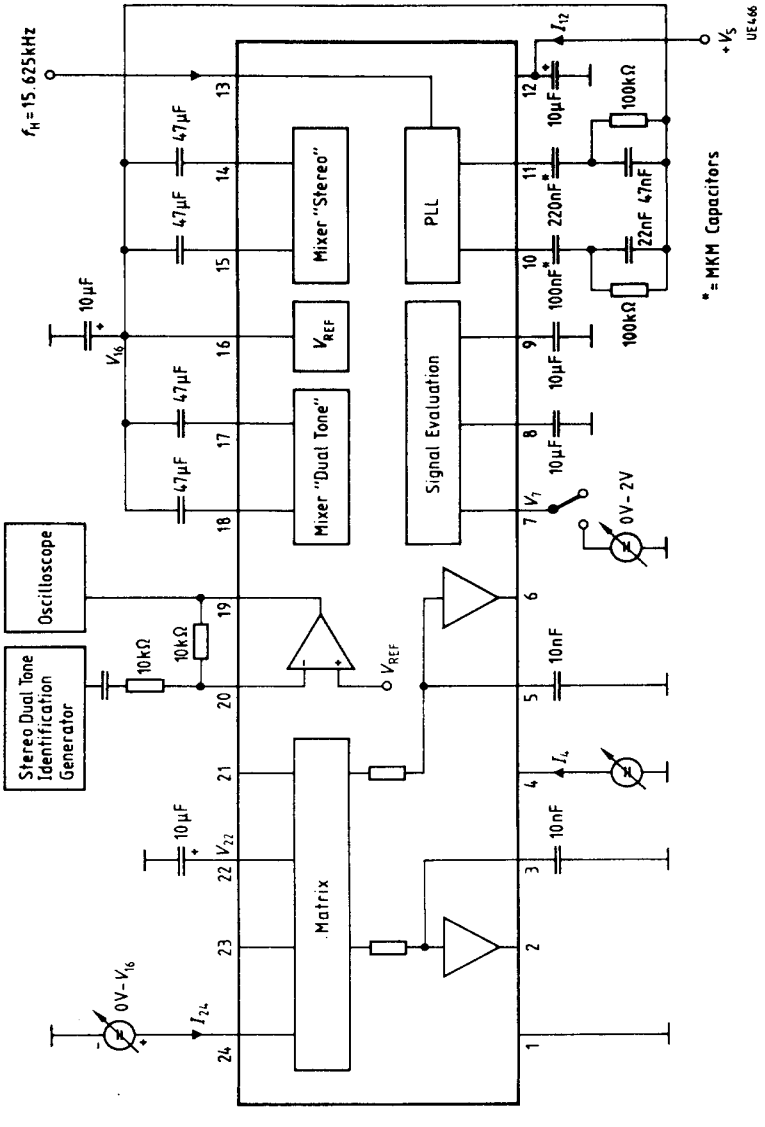
Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Decoder Section							
Identification sensitivity	V_{19}	71			mV rms	Pin 19: Pilot frequency is modulated with identification frequency at 50% modulation depth. The mean value of the pilot frequency is indicated at which the decoder will safely recognize "stereo" and/or "dual sound".	1
Identification sensitivity (lower limit)	V_{19}	0		11	mV rms	Pin 19: Pilot frequency is modulated with identification frequency at 50% modulation depth. The mean value of the pilot frequency will safely remain in the "mono" mode	1

Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Max. permissible mixer input voltage	$V_{I\,19max}$			600	mV_{pp}		1
Signal delay through integrators	$t_{8/9}$		700		ms		4
4 Level Input / Output							
Output current	I_7			1	mA	V_7 = 0 V	1
Output voltage at "Stereo"	V_7	5.3	6		V		1
Output voltage at "Dual Sound"	V_7	2.6	3.1	3.6	V		1
Output voltage at "Mono"	V_7	1.1	1.3	1.6	V		1
Forced mono identification	V_7	0		0.6	V	voltage externally injected	1
Pulse width of forced mono	t_7	500			µs		1
Threshold gating pulse input	V_{13}	± 1.5		± 3.5	V		1
Design Related Data							
Mixer output resistance	$R_{14;15}$		8		kΩ		
4 level output impedance	$R_{17;18}$ R		8	 15	kΩ		

Test Circuit 1



Test Circuit 2

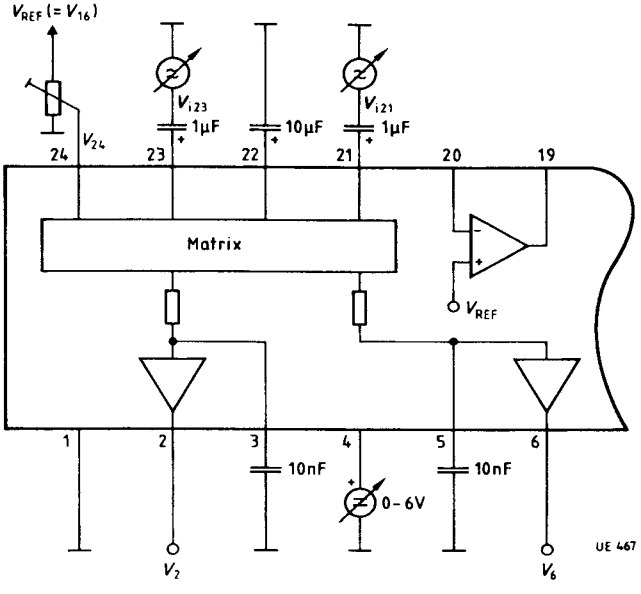


Diagram illustrating circuit layout between pin 7 and 20 identical to test circuit 1

Test Circuit 3

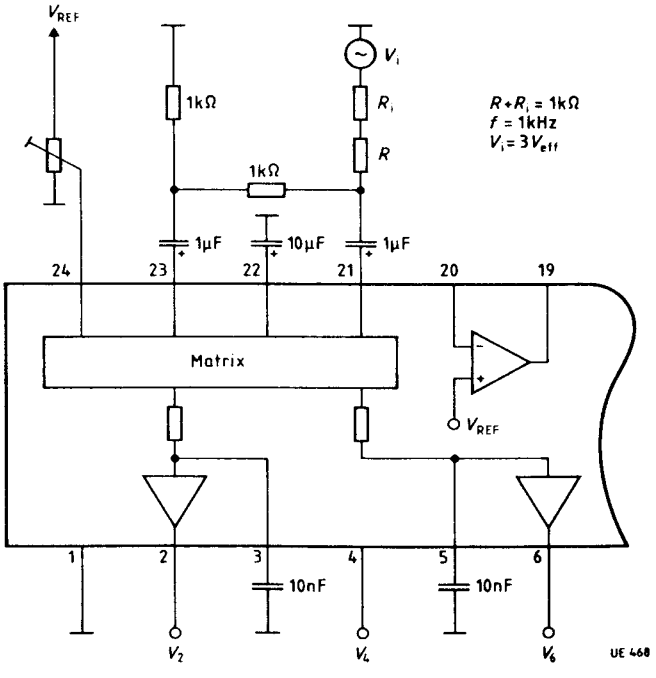
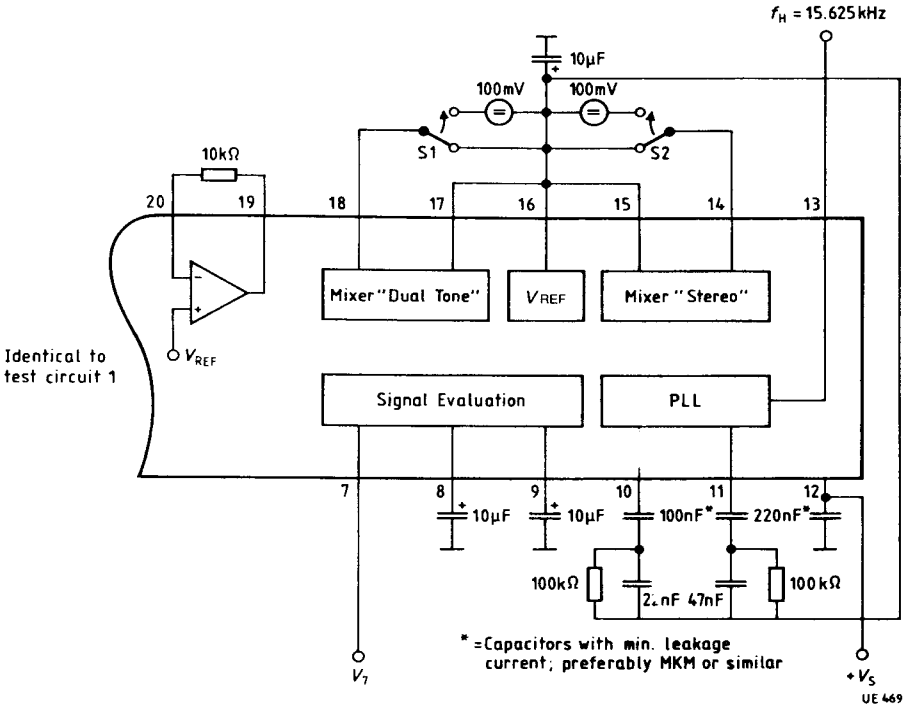


Diagram illustrating circuit layout between pin 7 and 20 identical to test circuit 1

Test Circuit 4



Application Circuit