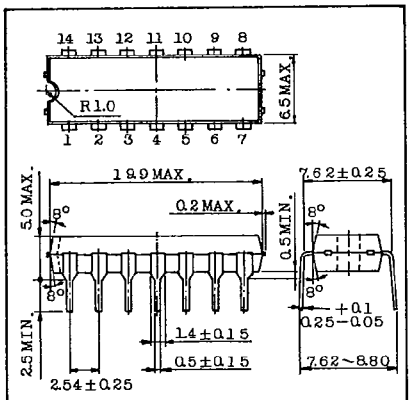
TA7089P

BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

GENERAL PURPOSE VOLTAGE REGULATOR.

- Low Output Impedance : Z_o =40mΩ (Typ.)
- High Ripple Rejection : RR=48dB(Typ.)
- Build in Current Limitting Circuit
- Low Drop Out Voltage : $|V_{IN}-V_{OUT}|$=1.8V
- High Output Current : I_{OUT}=200mA(Max.)
- Output Current Up to 5A Can be Supplied by Connecting External Transistor.
- The TA7089P is Easily Mounted on a Printed Circuit Board, and is Provided with 14 Pin Output, 7 Pin GND and 1 Pin Input for Application as a Power Supply for Digital IC.

Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

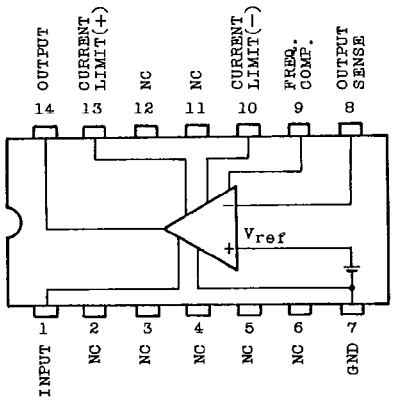
JEDEC	–
TOSHIBA	5-21D

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Input Voltage	V_{IN}	35	V
Terminal Voltage 8	V_8	7	V
Output Current	I_{OUT}	-200	mA
Power Dissipation	P_D	600	mW
Operating Temperature	T_{opr}	-30 ~ 75	°C
Storage Temperature	T_{stg}	-55 ~ 125	°C

PIN CONNECTION

TOP VIEW



ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{IN}	1	-	7	-	35	V
Output Voltage	V_{OUT}	1	$7 < V_{IN} < 35V$ $I_{OUT}=50mA$	3.3	0	33	V
Drop Output Voltage	$\lvert V_{IN}-V_{OUT} \rvert$	1	$R_{SC}=0$, $I_{OUT}=200mA$	2.0	1.8	-	V
Reference, Voltage	V_{ref}	1	$7 < V_{IN} < 35V$ $I_{OUT}=0mA$	2.7	3.0	3.3	V
Bias Current	I_B	1	$7 < V_{IN} < 35V$ $V_{OUT}=0mA$	1.5	3	6	mA
Ripple Rejection	RR	2	$V_{IN}=14V$, f=1kHz $V_{OUT}=10V$, $I_{OUT}=50mA$	40	48	-	dB
Output Voltage Temperature Coefficient	TC_{VO}	1	-	-	±0.02	-	%/°C
Output Current	I_{OUT}	1	-	-	-	-200	mA
Output Impedance	Z_o	3	$V_{IN}=14V$, f=1kHz $V_{OUT}=10V$, $I_{OUT}=50mA$	-	40	150	mΩ
Input Regulation	Reg·line	1	$I_{OUT}=50mA$ $15 < V_{IN} < 35V$	-	-	300	mV
Load Regulation	Reg·load	1	$V_{IN}=15V$ $50 < I_{OUT} < 200mA$	-	-	60	mV

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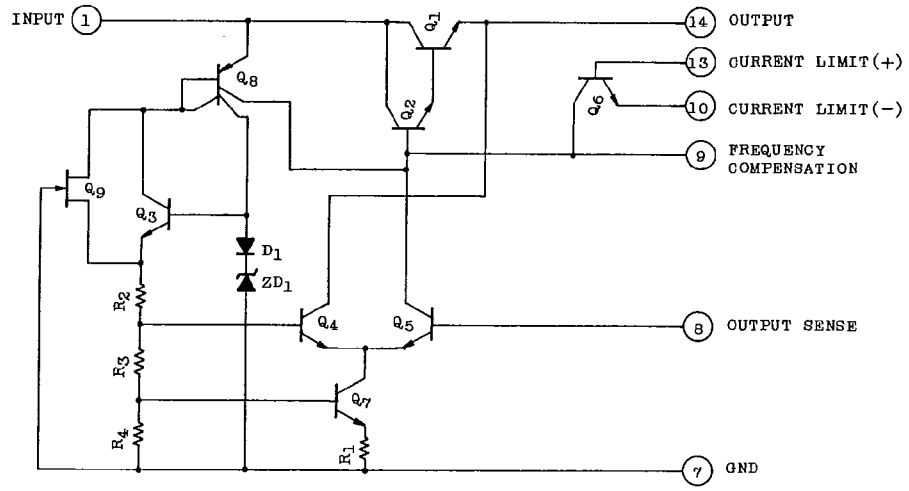
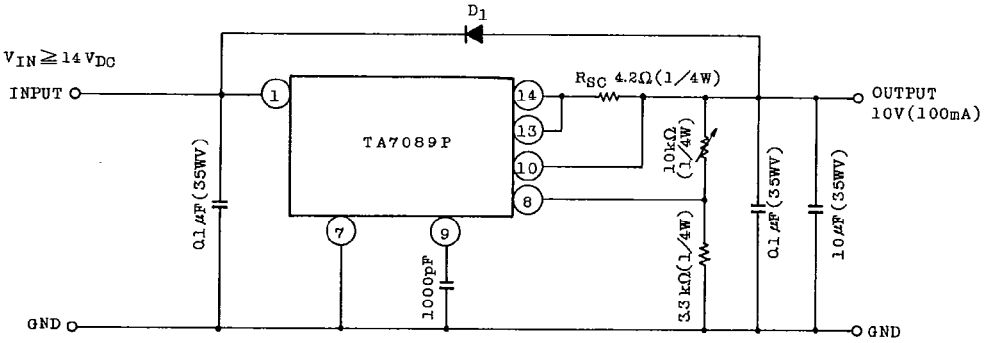
EQUIVALENT CIRCUIT



STANDARD APPLICATION CIRCUIT (10V, −100mA)



Note : IC Protecting Diode

When the surge voltage is applied to the IC output or when V_{IN}^{+} becomes more than $V_{OUT}^{+}(C_{IN}\ V_{OUT})$ at times of power ON or OFF.
It is required to cannot high speed diodes between input and output terminals.

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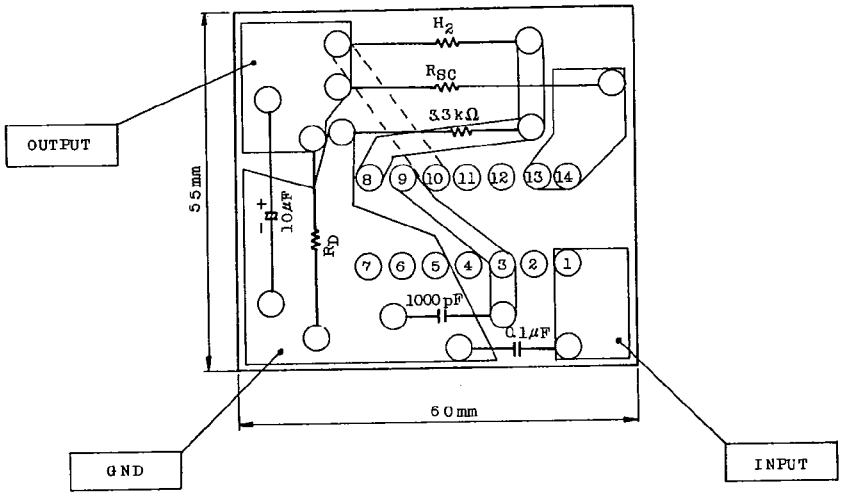
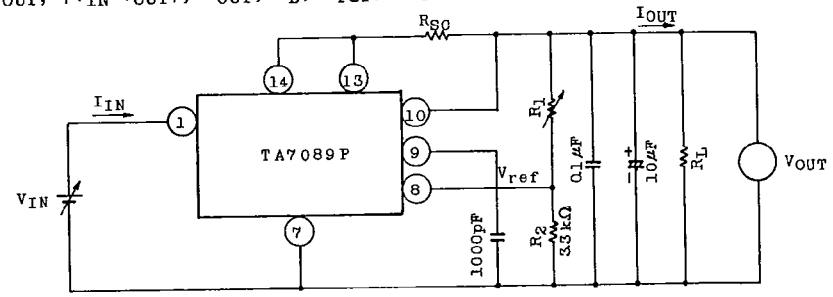
STANDARD PRINT BOARD

PATTERN



TEST CIRCUIT

1. V_{IN}, V_{OUT}, $|V_{IN}-V_{OUT}|$, I_{OUT}, I_B, V_{ref}, Reg·line, Reg·load, TC_{VO}

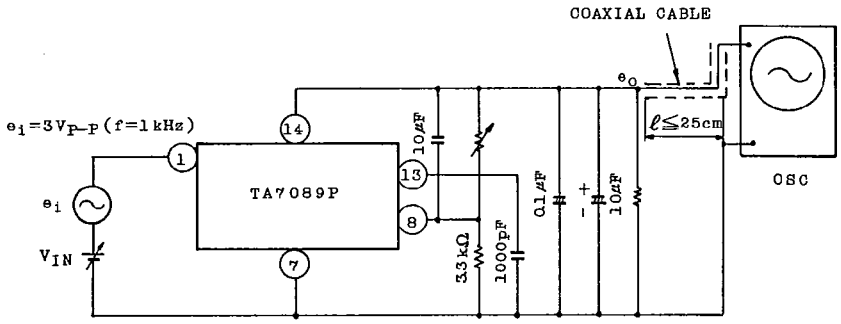


$$V_{OUT} = \frac{R_1+R_2}{R_2} \times V_{ref}$$

$$I_B = I_{IN}-I_{OUT}$$

$$TC_{VO} = \frac{V_{OUT}(75°C)-V_{OUT}(-30°C)}{V_{OUT}(25°C) \times 105} \times 100 \ (\%/°C)$$

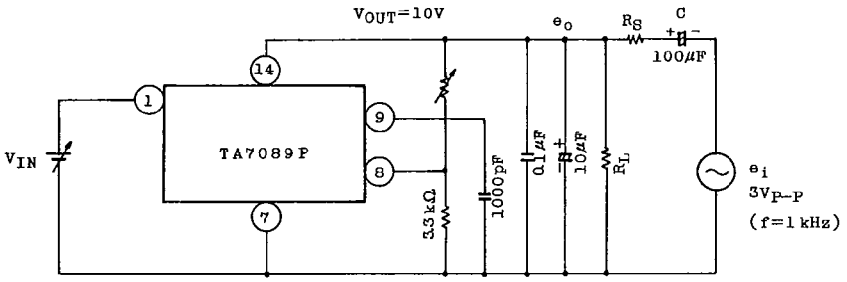
2. RR



Ripple Rejection

$$RR = 20 \log 10 \left(\frac{e_i}{e_o}\right) \quad (dB)$$

3. Z_o



Z_o Calculation Method

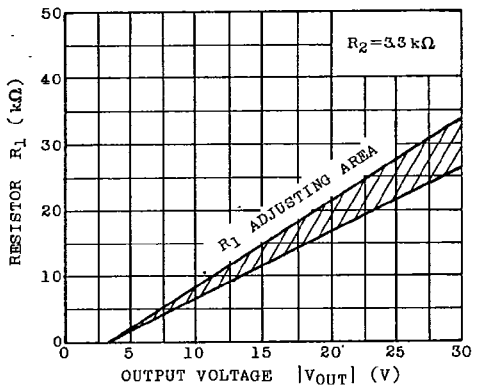
$$e_o = \frac{e_i}{R_S + Z_o} \cdot Z_o$$

$$R_S \gg Z_o$$

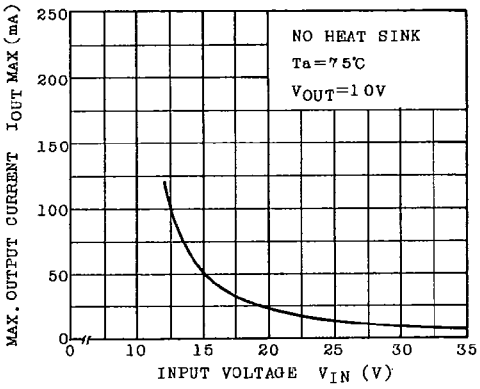
$$e_o = \frac{e_i}{R_S} \cdot Z_o$$

Therefore, $Z_o = \frac{e_o}{e_i} \cdot R_S \ (\Omega)$

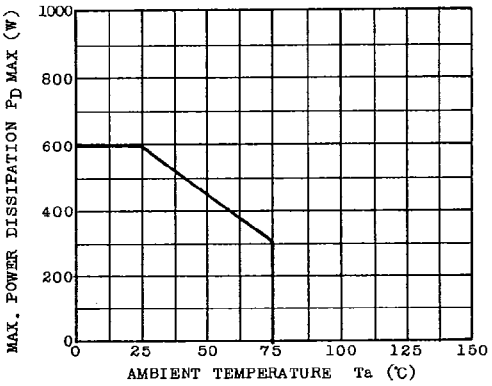
DECISION CHART OF RESISTOR R_1



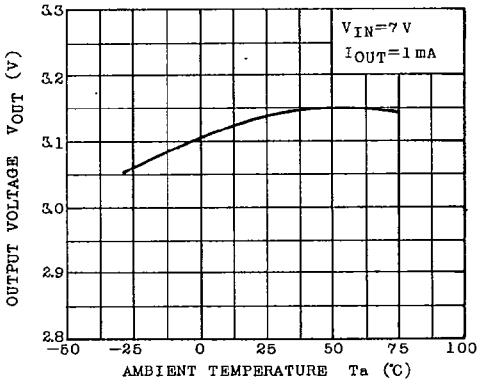
I_{OUT} MAX – V_{IN}



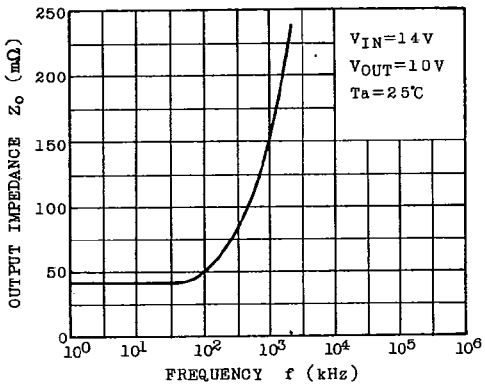
P_D MAX – Ta



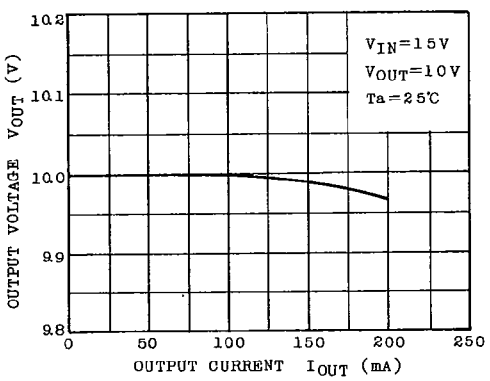
V_{OUT} – Ta



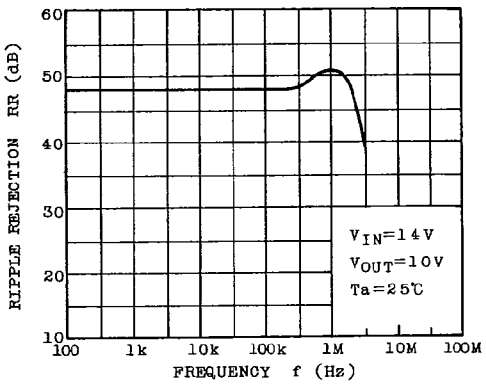
Z_O – f



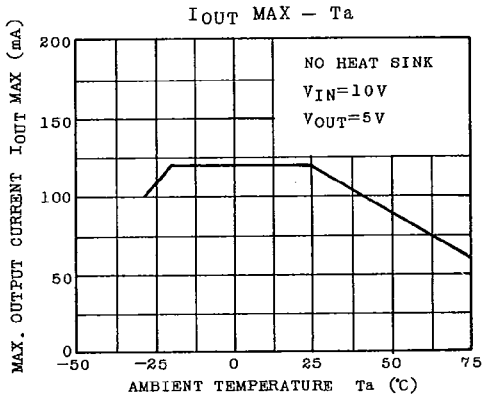
V_{OUT} – I_{OUT}



RR – f



I_{OUT} MAX – Ta



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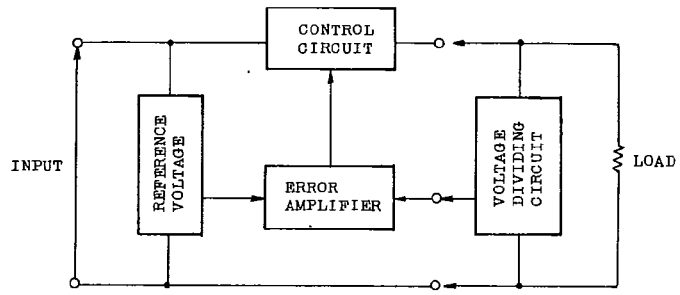
BLOCK DIAGRAM

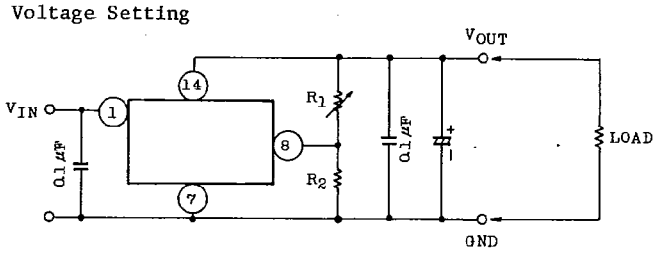


METHOD OF USE AND GENERAL PRECAUTIONS

1. Input Voltage Range

   The TA7089P can be used at 7 ~ 35V.

2. Output Voltage Setting



Output voltage is set by resistor R1 (See resistor-output voltage characteristic diagram.)

If $V_{OUT} = \frac{V_{ref}\ (R_1+R_2)}{R_2}$

Where, V_{ref}=3V

R_2=3.3kΩ

Output voltage is

$$\begin{cases} V_{OUT}=0.9\times10^{-3}\times R_1+3\,(V) \\ V_{IN}>V_{OUT}+2 \end{cases}$$

Output voltage setting range is 3.3 ~ 33V.

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3. Power Dissipation

Internal power dissipation P_D in IC at normal operation is

$$P_D = V_{IN} \times I_B + (V_{IN} - V_{OUT}) \times I_{OUT}$$

Where, I_B : Bias Current, V_{IN} : Input Voltage, V_{OUT} : Output Voltage, I_{OUT} : Output Current

Power dissipation at output shorted condition.

$$P_D = (I_{SC} + I_B) V_{IN}$$

Max. Power dissipation P_D MAX. must be as follows :

$$P_D \text{ MAX.} < \frac{T_j \text{ MAX} - Ta}{R_{th}}$$

Where, T_j MAX. ; Junction Temperature

Ta ; Ambient Temperature

R_{th} ; Thermal Resistance

T_j MAX. and R_{th} of the TA7089P are ;

T_j MAX. = 125°C

R_{th}=165°C/W (Free Air)

4. Rang of Output Current

Rang of output current is 0 ~ 200mA.

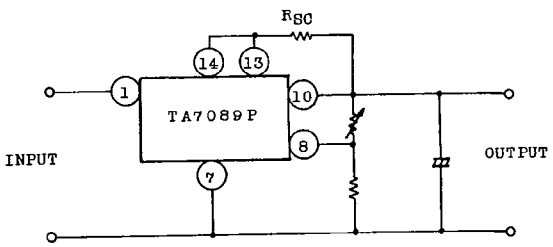
When output current is above 200mA, use external transistors.

(See Application circuits.)

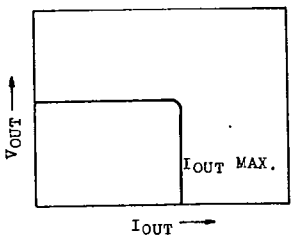
5. Control of Output Current

The TA7089P has a build-in output current limitting transistor and is therefore capable of constant current and fold back current limitting.

The constant current is limited as shown in the following diagrams.



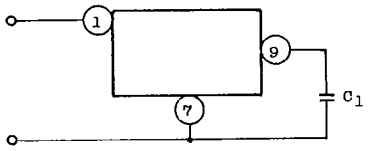
OVER CURRENT PROTECTIVE CHARACTERISTICS



Output current is limited at a point where voltage in RSC drops to voltage between the transistor base and emitter V_{BE} (about 0.65V at T_j=25°C)

$$R_{SC} = \frac{V_{BE}}{I_{OUT\ MAX.}} \qquad \text{Where,} \quad V_{BE} \fallingdotseq V_{BE}(T_j=25°C) - 2 \times 10\text{-}3\ (T_j\text{-}25)$$

6. Phase Compensating Capacitor



Select a capacitor having capacity 0.1μF-1000pF according to the external wiring conditions. Normally, use a capacitor at 1000pF.

7. Output Capacitors

Output capacitors of 10μF and 0.1μF shall be mounted parallelly.

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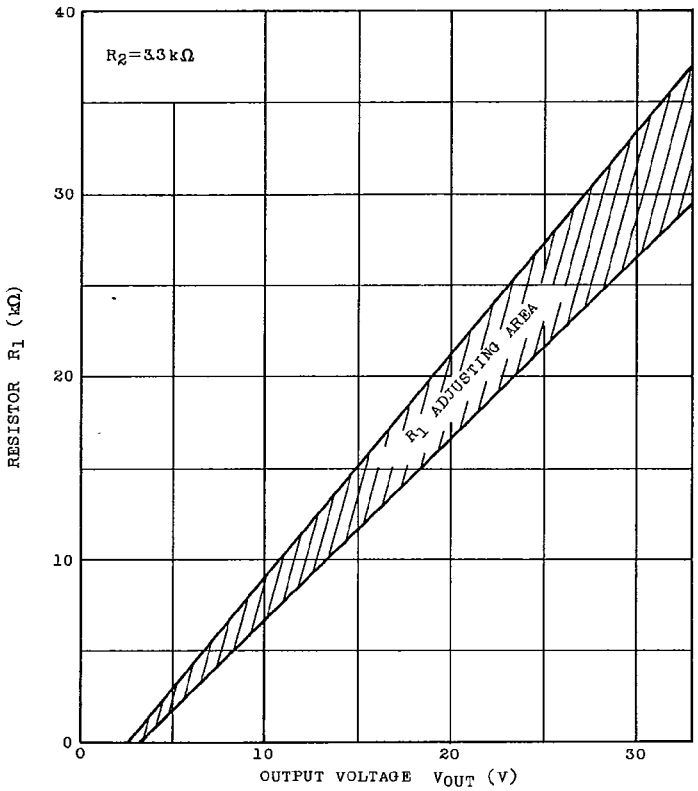
DECISION CHART OF RESISTOR R_1



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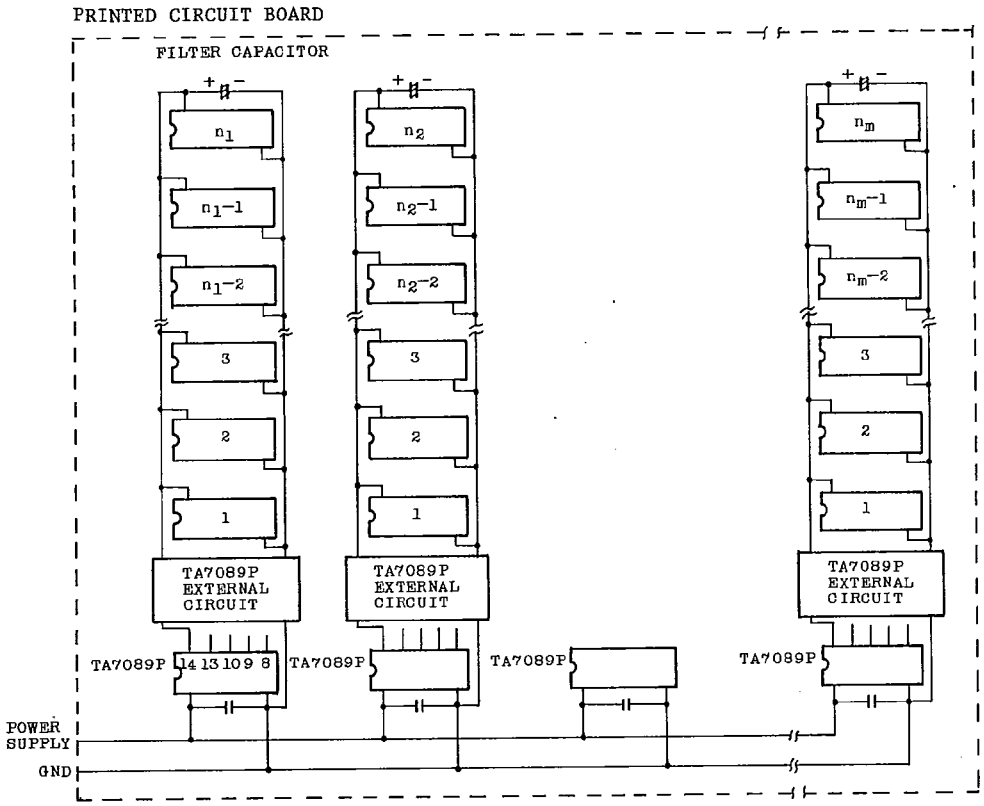
BASIC EXAMPLE OF 10μF MOUNTING OF TA7089P ON PRINTED CIRCUIT BOARD
(LOCAL REGULATOR APPLICATION)



ADVANTAGES

- Mutual effect between raws can be ignored.
- Adjustment is simple as malfunction due to noise is reduced.
- Pattern design is simple as the pin arrangement is 14 pins for output, 7 pins for GND and 1 pin for input.
- THL. IC, TTL. IC and other supply voltages can be incorporated into a same printed circuit board.

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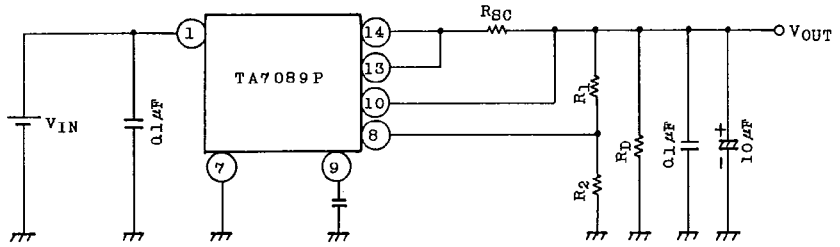
APPLICATION (1)

1. Circuit Diagram



2. Decision of Circuit Constant

Circuit specification

. Output Voltage V_{OUT}=6V

. Max. Output Current I_{OUT} MAX.=50mA

. Output Limitting Current I_{SC}=70mA

Decision of voltage dividing resistors R_1 and R_2

A resistor of 3.3kΩ is used as R_2 by considering current balance of a differential amplifier.

R_1 is obtained from the following expression or the resistor R_1 set-up table.

$$V_{OUT} = \frac{R_1+R_2}{R_2} \times V_{ref}$$

V_{ref} is in the range of 2.7~3.3V from the specification.

When R_1 is obtained through calculation according to the above, it is

$2.7k\Omega \leqq R_1 \leqq 4.4k\Omega$

Further, 3~4kΩ is obtained from the R_1 set up table.

Therefore, Resistor R_1 would be 3kΩ (fixed) + 1kΩ (variable resistor).

Decision of R_{SC}.

Current limitting resistor RSC value is obtained from the following expression :

$V_{BE} = R_{SC} \times I_{SC}$

V_{BE} : Base to emitter voltage of an internal current limitting transistor.

A value at $T=T_j$ is applied.

Assuming that a value of V_{BE} (at T_j=125°C) is 0.45V, R_{SC} is 6.4Ω when I_{SC}=70mA is substituted.

Decision of Min. Input Voltage

Min. input voltage V_{IN} MIN. which is required to operate this circuit is

$$V_{IN}\ \text{MIN.}=V_{OUT}+|V_{IN}-V_{OUT}|+V_R$$

V_R : Voltage between R_{SC}

Where, V_{OUT}=6V

$|V_{IN}-V_{OUT}|$=2V (from the Electrical characteristic table)

V_R=0.65V

Therfore, V_{IN} MIN.=8.65V

Decision of R_D

R_D is dummy resistor used to flow current constantly in order to operate the circuit stability.

Required current is approximately 3mA.

$$R_D = \frac{V_{OUT}}{3mA} \fallingdotseq 1.8k\Omega$$

Calculation of P_D

At the normal condition, max. power dissipation of IC is obtained from the following expression :

$$P_D=V_{IN}\times I_B+(V_{IN}-V_{OUT}) \times I_{OUT}$$

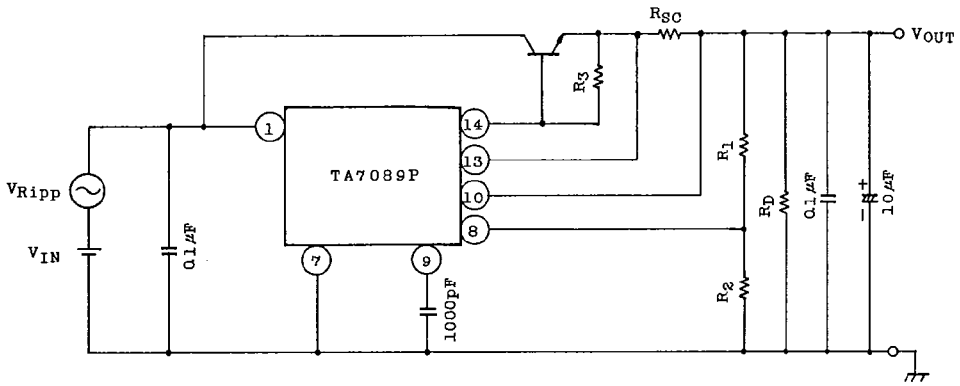
Power dissipation at load shorted condition is obtained from the following expression :

$$P_D=V_{IN}\times I_B+(V_{IN}-V_R) \times I_{SC}$$

Designing should be made carefully by calculating power dissipation at time of load shorted, input voltage and transformers so that P_D MAX. is not exceeded.

APPLICATION (2) CURRENT BOOST CIRCUIT EXAMPLE

1. CIRCUIT



2. Decision of Circuit Constants

Circuit Specification

- Output Voltage V_{OUT} 5V
- Max. Output Current I_{OUT} MAX. 1A
- Current Limitting Protection Circuit

. Decision of Voltage Dividing Resistors R_1 and R_2

A resistor of 3.3k is used as R_2 by considering current balance of a differential amplifier.

R_1 is obtained from the following expression :

$$V_{OUT} = \frac{R_1+R_2}{R_2} \times V_{ref}$$

When the resistor R_1 setting table (2) is used,

R_1 = 1.5kΩ~3kΩ

Therefore, R_1 would be 1.5kΩ (fixed) + 2kΩ (variable).

. Decision of R_{SC}

$$V_{BE} = R_{SC} \times I_{SC}$$

Assuming that

I_{SC}=1.2A

V_{BE}=0.65V

$$R_{SC} = \frac{V_{BE}}{I_{SC}} = \frac{0.45V\ (T_j=125°C)}{1.2} = 0.4\ (\Omega)$$

Rated capacity is

$0.65V \times 1.2A = 0.78$ (W)

$R_{SC}=0.4\Omega$ (1W)

. Decision of Min. Input Voltage

Obtaind Min. input voltage of the circuit.

$V_{IN\ MIN} = V_{OUT} + |V_{IN} - V_{OUT}| + V_{BE} + V_R$

V_R : Voltage between R_{SC}

when, $V_{OUT}, |V_{IN} - V_{OUT}|, V_{BE}, V_R$

expression, $V_{IN\ MIN} = 5.0 + 2.0 + 0.7 + 0.6$

$= 8.3$ (V)

Further, as the catalog standard is 7V or above,

$V_{IN\ MIN} = 8.3$ (V)

. Decision of R_3

Resistor R_3 is to be inserted for stabilizing the circuit and several mA would be sufficient.

When the circuit is designed by assuming that current is 5mA.

$$R_3 = \frac{V_{BE}}{5mA} = \frac{0.7V}{5mA} \fallingdotseq 150\ (\Omega)$$

. Decision of R_D

Resistor R_D is used to apply dummy current and functions to stabilize the circuit together with R_3.

1 ~ 10mA is generally accepted. The design is made here at 5mA.

$$R_D = \frac{V_{OUT}}{I_D} = \frac{5V}{5mA} = 1\ (k\Omega)$$

Summary

R_2	3.3kΩ
R_1	1.5kΩ (fixed) + 2kΩ (variable)
R_{SC}	0.4Ω (1W)
R_3	150Ω
R_D	1kΩ
V_{IN} MIN.	8.3V

3. Parastic Oscillation Prevention

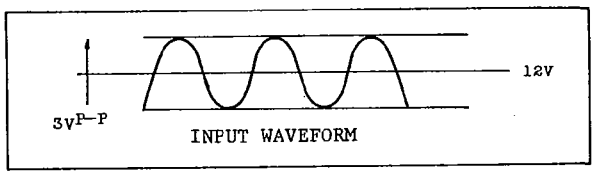
To prevent a parastic oscillation, insert a capacitor of about 0.1μF into the input and output sides. It would be effective when the capacitor is insert as close as to IC terminals.

4. Example of Output Voltage Ripple Value Calculation

Assuming that input ripple voltage is 3 V_{p-p} AC,

$$V_{IN} = 10V_{DC} + 3V_{p-p}\ AC$$

However, actual mean value of full load input voltage when voltage fluctuation at the transformer primary side is considered is 12V DC.



Obtain output ripple voltage.

As Reg. in is min. 40(dB) from the standard data table,

(Output ripple voltage) = 30mV_{p-p} AC.

5. Selection of Power Transistor

Full Load Input Voltage	12V (AVG)
Output Voltage	5V
Output Current	1A

When P_D MAX. is obtained from the above data,

$$P_D\ MAX = (12-5) \times 1$$
$$= 7\ (W)$$

However, when power dissipation resulted from output short is calculated.

$$P_D\ MAX = 12 \times 1.2 = 14.4\ (W)$$

2SD867 (or equivalent) is selected this time from TOSHIBA SEMICONDUCTOR HAND BOOK.

6. Design of Heat Sink

1) Design of power transistor radiation

From the 2SD 867 data table (TOSHIBA SEMICONDUCTOR HAND BOOK)

$$R_{th(j-c)} = \frac{150-25}{100} = 1.25°C/W$$

Therefore, $R_{th(j-a)}=1.25+1.0+R_{th(f)}$

(It is assumed that $R_{th(s)}+R_{th(c)}=1.0°C/W$)

P_D MAX = 14.4W
Tj MAX = 150°C
Ta=60°C (Including temperature rise in device)

From the above data,

$$R_{th(j-a)} = \frac{Tj\ MAX - Ta}{P_D\ MAX} = \frac{150-60}{14.4} = 6.2°C/W$$

Accordingly, thermal resistance required for a heat sink is,

$$R_{th(f)} = R_{th(j-a)} - R_{th(j-c)} - R_{th(s)} - R_{th(c)}$$
$$= 6.2 - 1.25 - 1.0$$
$$= 3.95°C/W$$

When an Aℓ heat sink is used, size required can be seen as follows from TOSHIBA SEMICONDUCTOR HAND BOOK :

100mm × 170mm × 2mm

Further, in actual designing it is a general practice to derate Tj MAX taking reliability into consideration.

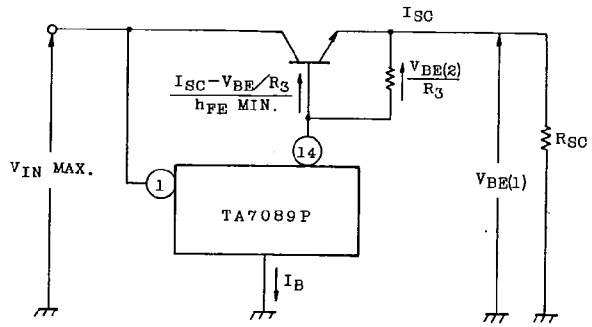
2) Design of IC Heat Sinking

Max. power consumed in IC is obtained from the following expression :

$$P_D\ MAX = (V_{IN}\ MAX - V_{BE(1)}) \times \left(\frac{I_{SC} - V_{BE(2)}/R_3}{h_{FE(MIN)}} + \frac{V_{BE(2)}}{R_3} + I_B\ MAX\right)$$

Assuming that

$V_{BE(1)}$: V_{BE} of current limitting internal transistor = 0.65V
$V_{BE(2)}$: V_{BE} of power transistor = 0.65V
h_{FE} MIN : Min. value of h_{FE} of power transistor (at $I_C=I_{SC}$) ≒ 40
I_B MAX : Max. value of bias current of TA7089P = 6mA
P_D MAX is above 504mW.



7. Application

Specification

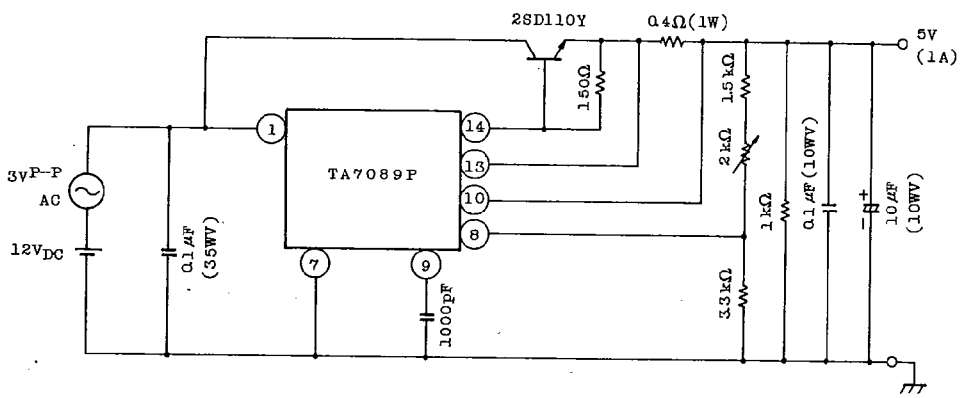
V_{IN} $12V_{DC} + 3V^{P-P}_{AC}$

V_{OUT} $5V_{DC} + 30mV^{P-P}_{AC}$

I_L MAX 1.2A

Current limitting protection circuit

Example 1. Current Boost Circuit



2SD876 Heat Sink ($R_{th(f)}$ = 3.95°C/W)

100 × 170 × 2mm Al

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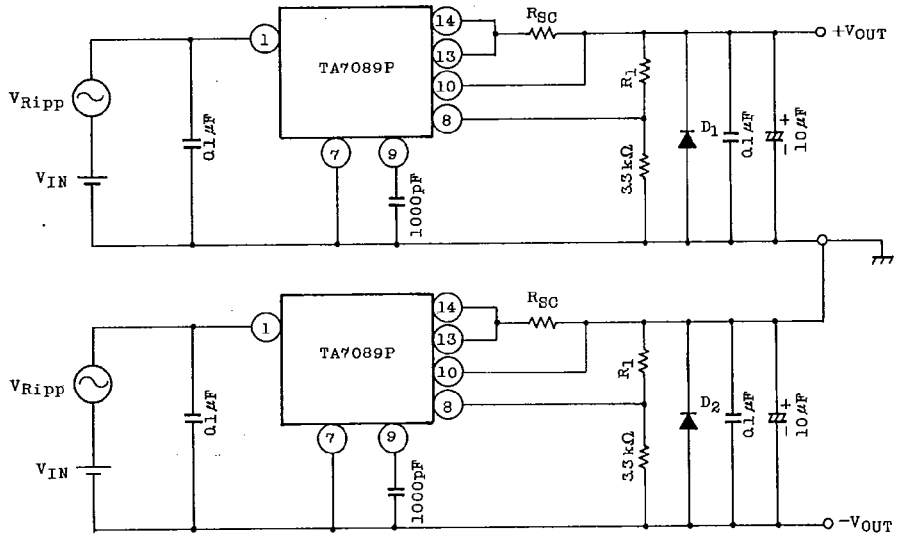
Example 2. Positive and Negative Power Supplied



Use diodes having less forward voltage drop for D_1 and D_2.