Ordering number: EN 4554A

Thick Film Hybrid IC

SANYO

No. 4554A

STK6875

Bidirectional DC Brush-type Motor Driver (I_O max = 5A)

Overview

The STK6875 is a bridge-type power pack, bidirectional DC brush-type motor driver IC that incorporates Sanyo's unique IMST (insulated metal substrate technology) for superior thermal radiation characteristics. In comparison with the STK6860H series, it employs power MOSFETs in an H-bridge configuration to realize low power dissipation and high current output.

Applications

- PPC drum and scanner motor drivers
- LBP drum motor drivers
- Printer head carriage motor drivers
- General DC motor applications

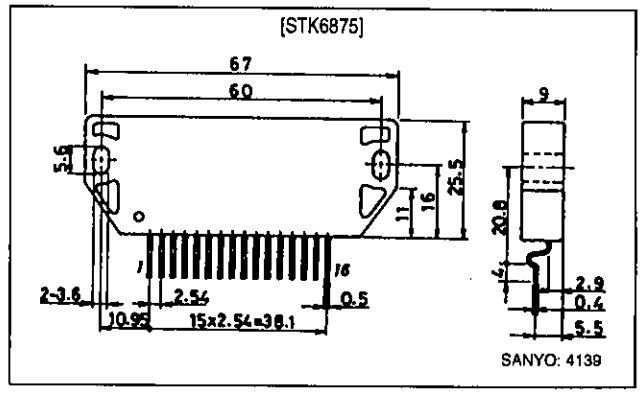
Features

- Employs MOSFETs for rush current margin
- TTL-level signal inputs
- 3-pin PWM control
- Brake function
- Wide operating supply voltage ($V_{CC}1$ = 12 to 42V)
- Few external components (only 2 external bootstrap capacitors required for operation)

Package Dimensions

unit: mm

4139



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	$V_{CC}1$ max	No signal	50	V
Maximum supply voltage 2	$V_{CC}2$ max	No signal	7	V
Maximum peak rush current	Io peak	100ms cycle, ≤1% duty, $V_{CC}2$ = 5.0V	12	A
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

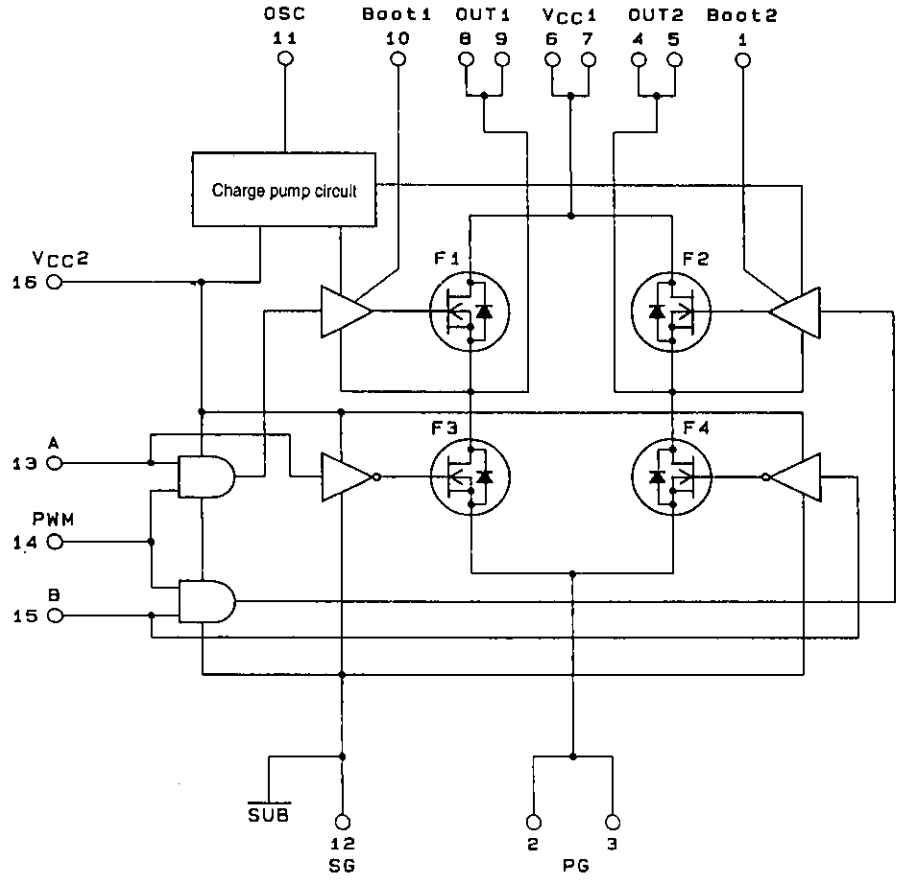
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$	Input signal present	12 to 42	V
Supply voltage 2	$V_{CC}2$	Input signal present	5 ±5%	V
Motor output current	I_{OH} max	DC	5	A
PWM frequency	fp		1 to 30	kHz
FET withstand voltage	V_{DSS}		60	V

Operating Characteristics at Ta = 25°C, $V_{CC}1$ = 24V, $V_{CC}2$ = 5.0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	I_{CCO}	R_L = 4.5Ω	30	40	50	mA
Output saturation voltage	Vst	R_L = 4.5Ω	–	0.85	1.20	V
Input ON voltage	V_{IH}		2.0	–	–	V
Input OFF voltage	V_{IL}		0	–	0.8	V
Input ON current 1	$I_{IH}1$	V_I = 2.7V (pin 14)	–	–	20	μA
Input ON current 2	$I_{IH}2$	V_I = 2.7V (pin 13 or 15)	–	–	0.7	mA
Input OFF current 1	$I_{IL}1$	V_I = 0.4V (pin 14)	–	–	–0.4	mA
Input OFF current 2	$I_{IL}2$	V_I = 0.4V (pin 13 or 15)	–	–	–0.2	mA
Diode forward bias voltage	Vdf	Idf = 5A, V_{GS} = 0V	–	1.30	1.60	V
Sensing voltage	Vsense		–	–	0.5	V

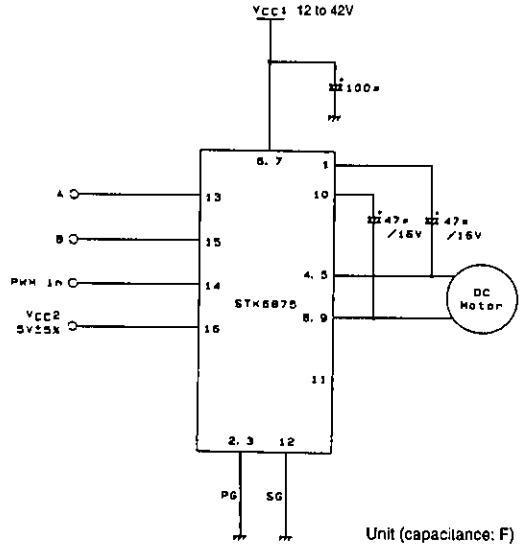
Note. All tests are measured using a regulated power supply.

Equivalent Circuit



"Boot" is an abbreviation for "bootstrap."
OSC (pin 11) is left open for normal operation.

Sample Application Circuit



Unit (capacitance: F)

Mode	Phase Inputs	
	A	B
Forward	H	L
Reverse	L	H
Standby 1 (prohibited)	H	H
Standby 2	L	L

Notes.
H = 5V, L = 0V
Input specifications: TTL-levels, Maximum PWM input frequency = 30kHz, PWM input should be tied HIGH if 2-pin control is used.
OSC (pin 11) is left open for normal operation and is used as a monitor point.

Heatsink Design

Heatsink Thermal Resistance

The heatsink size is determined by the motor output current (I_{OH}), the motor electrical characteristics and chopping frequency, and the conduction frequency.

The heatsink thermal resistance (θc-a) is given by the following equation.

$$\theta c\text{-}a = \frac{Tc\ max - Ta}{Pd}\ [°C/W]$$

where Tc max is the hybrid IC substrate temperature [°C], Ta is the ambient temperature within the set [°C], and Pd is the hybrid IC internal average power dissipation [W].

For a 2mm thick aluminum heatsink, the required surface area can be determined from Figure 2. However, as the ambient temperature within the set can vary greatly due to air flow conditions, the heatsink size should be chosen such that the temperature of the IC rear surface (aluminum side) mounting does not exceed Tc = 105°C.

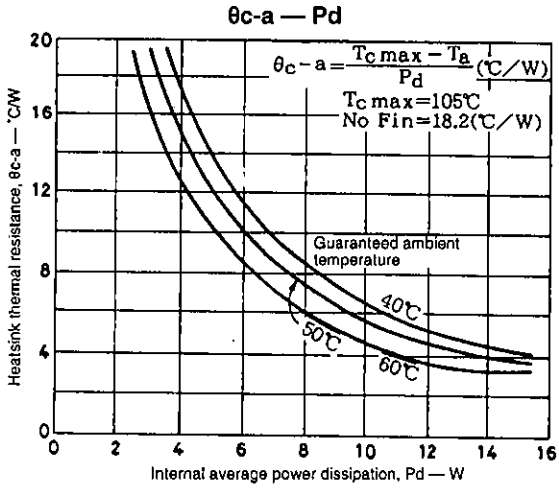


Figure 1. θc-a — Pd

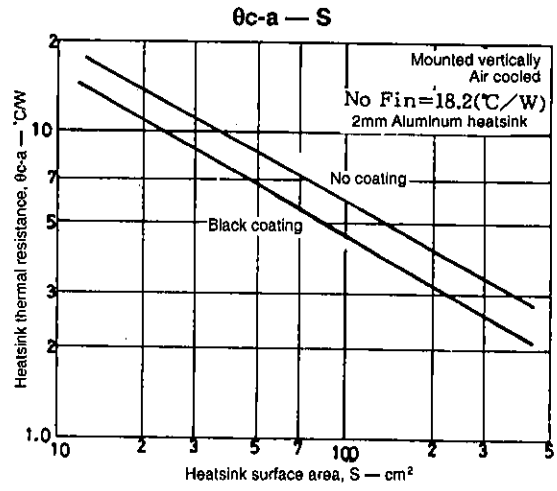


Figure 2. θc-a — S

Internal Average Power Dissipation

Within the hybrid IC, the large power dissipation elements are the H-bridge configuration upper PWM FETs, the lower FETs comprising the forward/reverse loop, and the flywheel FET body diodes. Therefore, the internal average power dissipation (Pd) can be given by the following equation.

Pd = upper FET loss + lower FET loss + body diode loss

$$= Vst \times I_M \times fp \times t_{ON} + Vst \times I_M + Vdf \times I_M \times fp \times t_{OFF}$$

where Vst is the FET saturation voltage [V], I_M is the motor output current [A], Vdf is the FET body diode forward bias voltage [V], and fp is the chopping frequency [Hz].

Figures 5 and 6, respectively show the Io-Vst and Io-Vdf characteristics.

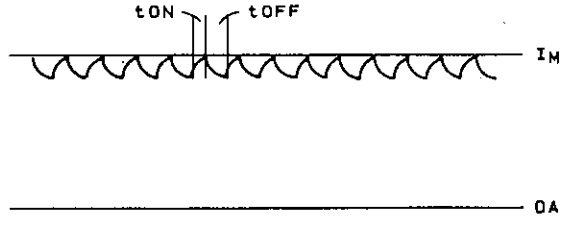


Figure 3. I_M model waveform

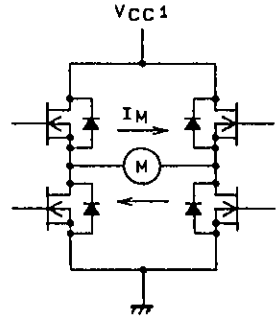


Figure 4. Model circuit diagram

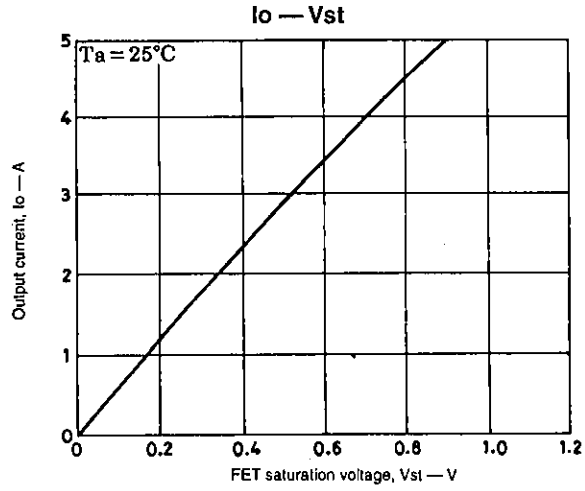


Figure 5. Io — Vst

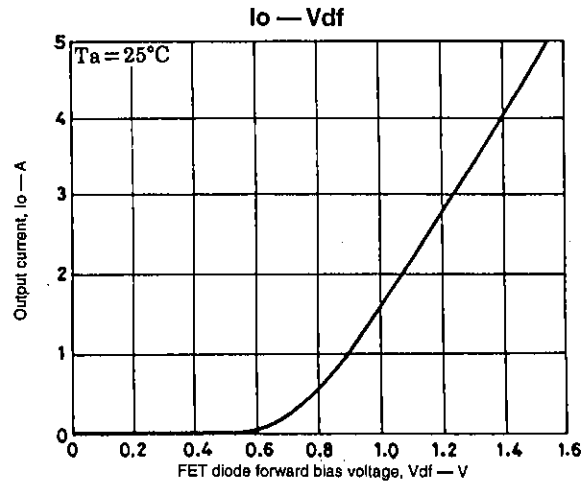


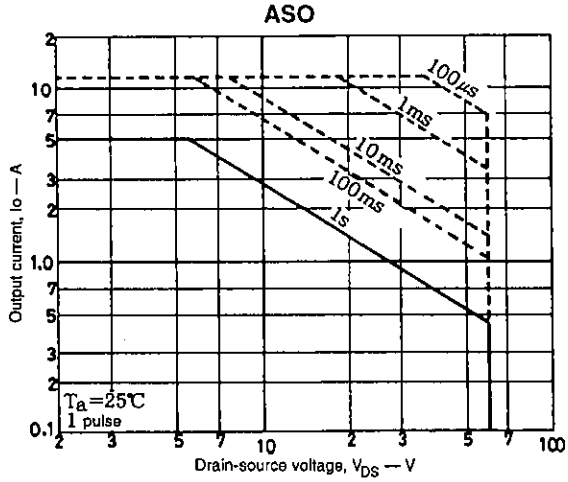
Figure 6. Io — Vdf

Junction Temperature

The junction temperature for each element (F1 to F4) is given by the power dissipation per element (Pds [W]) and the junction thermal resistance (θj-c [°C/W]).

$Tj = Tc + \theta j\text{-}c \times Pds$ [°C]

where Pds is the power dissipation per element. The power element thermal resistance for F1 to F4 is θj-c = 7°C/W under the conditions shown in the ASO diagram.



Usage Notes

Driver Start-up Method

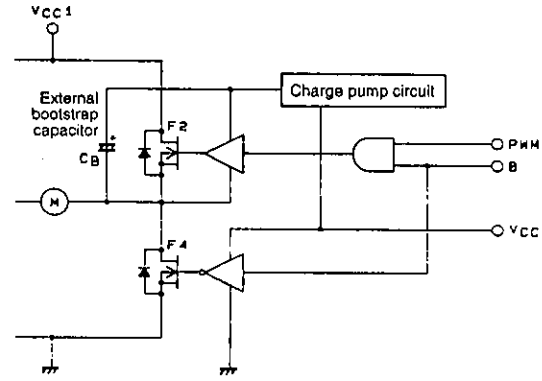


Figure 7. Upper and lower MOSFET drive circuit

When the driver circuit starts, the external control signals are in standby mode (A = LOW and B = LOW; A = B = HIGH is a prohibited mode). After the supply voltages ($V_{CC}1$, $V_{CC}2$) are applied to the driver circuit, the external control input signals then control the circuit drive mode.

Phase A = HIGH (pin 13) and B = HIGH (pin 15) input signal mode (prohibited mode)

When A = HIGH and B = HIGH input signal mode (standby mode 1), the following abnormal circuit operation can occur. Accordingly, the use of this mode of operation should be avoided.

- When in standby mode 1, the external bootstrap capacitor (47μF/16V) charge voltage Vch drops to an insufficient level. As a result, when the driver circuit switches to the start-up condition, the high side FET (F1 and F2) drive voltage (V_{GS}) is too low.
- If phases A and B both go HIGH after a start-up condition, the motor rotational energy causes the high side FETs to form a current loop (braking current). The high side FET drive voltage (V_{GS}) drops, and the insufficient drive can lead to device breakdown. In this mode, if the

charge voltage (Vch) for both bootstrap capacitors (47μF/16V) is monitored and maintained at Vch ≥ 4.0V, phases A and B both being HIGH should not cause any problems. Therefore, precaution should be taken to maintain the bootstrap capacitor charge voltage if using standby mode 1 to stop the motor (Phase A is monitored between pin 10 and pins 8 and 9. Phase B is monitored between pin 1 and pins 4 and 5.).

PG (pins 2 and 3) and SG (pin 12) functions

The circuit pattern for the power ground, PG, and the signal ground, SG, should be designed to form a single earth point. Also, a current detection resistor can be connected to PG, as shown in Figure 8. The voltage drop (V_{RE}) across the resistor (R_E) is given by the following equation.

$$V_{RE} = (I_{OH} \times R_E) \leq 0.5V$$

where I_{OH} is the motor output current [A], R_E is the current detection resistance [Ω], and V_{RE} is the voltage drop across R_E. The value for R_E should be chosen taking into consideration that the value for V_{RE} must not exceed the specification for the sensing voltage Vsense.

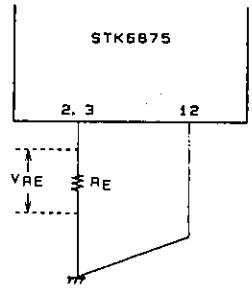


Figure 8. PG and SG common ground point

Braking Operation

There are 3 brake modes, as explained below.

In mode (a), phase A and B inputs both go LOW (motor is short circuited because F3 and F4 only are ON).

In mode (b), PWM input goes LOW (motor flywheel current regeneration).

In mode (c), both phase A and B inputs go LOW after PWM has gone LOW (combination of modes (a) and (b)).

- In brake mode (a), the lower MOSFETs are used for speed damping, or braking (Fast Motor Stop). The motor is effectively short circuited and, therefore, the flywheel current rises rapidly and the lower FETs can become overloaded. Figure 10 shows the overload flywheel current flowing in the F3 and F4 loop shown in Figure 9. Precaution should be taken if using this mode to ensure that the overload flywheel current flowing in the lower FETs does not exceed the maximum rating of the hybrid IC.

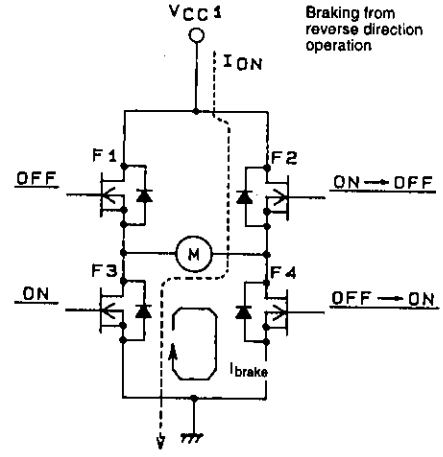


Figure 9. Brake mode (a) current flow

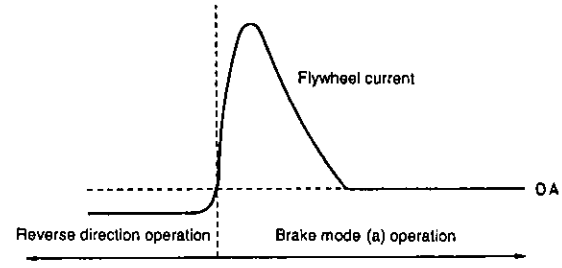


Figure 10. Motor flywheel current

- In brake mode (b), the motor rotational current just prior to the application of the control signals dissipates through the lower MOSFET, as shown in Figure 11, to stop the motor (Free Running Motor Stop). There is thus no overload condition, but braking takes longer.

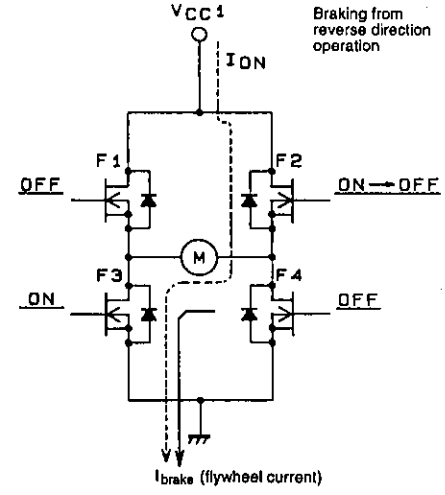


Figure 11. Brake mode (b) current flow

- In brake mode (c), PWM input goes LOW to dissipate some degree of motor rotational energy. Then, phase A and B inputs go LOW for full braking. Because brake mode (b) is first used to dissipate some rotational energy, the current that flows in the lower MOSFET during brake mode (a) operation should not exceed the maximum rating of the device.

However, after the PWM input goes LOW, the degree of dead time required before mode (a) operation should be chosen such that the flywheel current does not exceed the maximum rating (Figure 12). The brake time required for the motor to stop is shorter than that in brake mode (b). Also, brake mode is simply released by taking either the PWM input or a phase input HIGH.

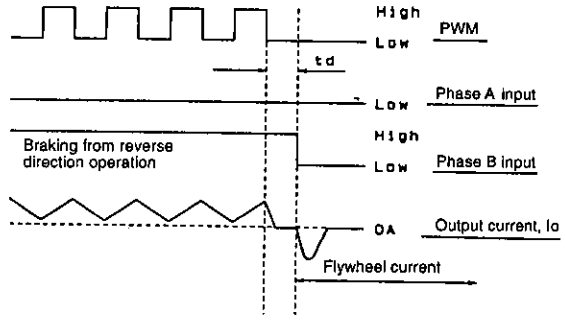


Figure 12. Brake mode (c) input signal timing chart

Sanyo recommends brake mode (c) operation to provide good brake time with safe flywheel current levels.

Upper and Lower MOSFET Short-circuit Current

When using brake mode (a) or (c), and when releasing brake mode, it is possible that the upper and lower MOSFETs can be simultaneously ON. Accordingly, each MOSFET driver circuit has a built-in delay of >1μs input signal dead time (td1 and td2) to prevent large short-circuit current flowing through the upper and lower MOSFETs.

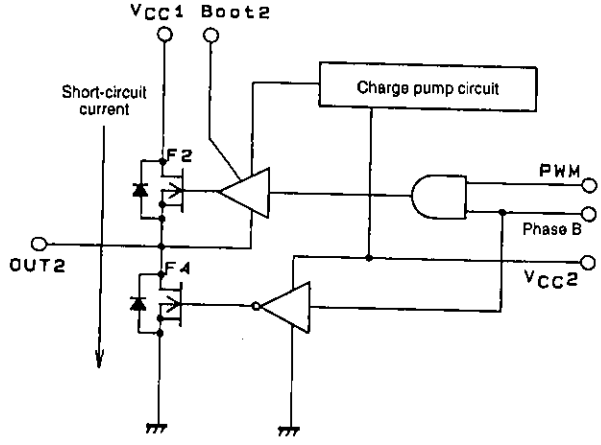
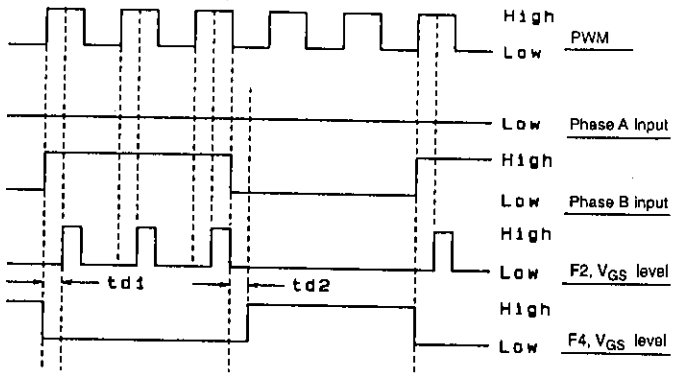


Figure 13. Upper and lower MOSFET equivalent circuit



td1 = upper MOSFET drive circuit dead time
td2 = lower MOSFET drive circuit dead time
td1, td2 ≥ 1μs

Figure 14. Upper and lower MOSFET V_{GS} voltage timing chart