



No. 4799A

**LC7538JM**  
**Electronic Volume Control System  
 for Car Audio**

**Overview**

The LC7538JM is a fully equipped electronic volume IC which permits significant reductions in externally connected components while providing ample volume, balance, loudness, fader, bass and treble control functions.

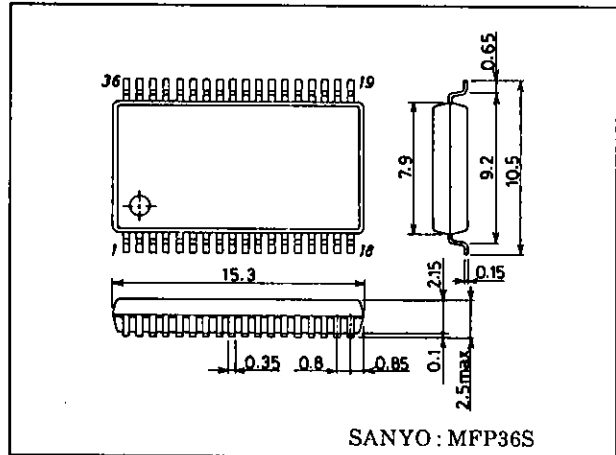
**Features**

- **Volume** : 81 positions ranging from 0 dB to -79 dB (in 1 dB increments) plus -∞. Separate left and right control provides excellent balance function.
- **Loudness** : Loudness operation provided by externally attached CR to activate tap at the -20 dB position of the volume ladder resistor.
- **Fader** : Fader function traversing 16 positions with rear or front attenuated output only (these 16 positions consist of 2 dB step intervals ranging from 0 dB to -20 dB, 5 dB step intervals ranging from -20 dB to -45 dB, plus the end settings of -60 dB and -∞).
- **Bass and Treble**: Using externally attached C (capacitor), the LC7538JM provides bass-treble mutual 15-position control and formats a NF-form tone control circuit (LUX form).
- On-chip op amplifier for caching applications reduces external components.
- Reduced switching noise with silicon gate CMOS processor.
- All controls performed using serial data input (C<sup>2</sup>B).

**Package Dimensions**

unit : mm

**3204**



**Specifications**

**Absolute Maximum Ratings at Ta = 25°C, V<sub>SS</sub> = 0 V**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	V <sub>DD</sub>	11	V
Maximum input voltage	V <sub>IN</sub> max1	CL, DI, CE	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>IN</sub> max2	LTIN, RTIN, L5dBIN, R5dBIN, L1dBIN, R1dBIN, LFIN, RFIN	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	210	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-50 to +125	°C

**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**  
 TOKYO OFFICE: Tokyo Bldg., 1-10, 1-Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

**LC7538JM**

**Allowable Operation Conditions at Ta = 25°C, VSS = 0 V**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	VDD	*1	7.0		10.0	V
Input high level voltage	V <sub>IH</sub>	CL, DI, CE	4.0		V <sub>DD</sub>	V
Input low level voltage	V <sub>IL</sub>	CL, DI, CE	V <sub>SS</sub>		1.0	V
Input amplitude voltage	V <sub>IN</sub>	LTIN, RTIN, L5dBIN, R5dBIN, L1dBIN, R1dBIN, LFIN, RFIN	V <sub>SS</sub>		V <sub>DD</sub>	Vp-p
Input pulse width	t <sub>pw</sub>	CL	1			μs
Setup time	t <sub>SETUP</sub>	CL, DI, CE	1			μs
Hold time	t <sub>HOLD</sub>	CL, DI, CE	1			μs
Operating Frequency	f <sub>opg</sub>	CL			500	kHz

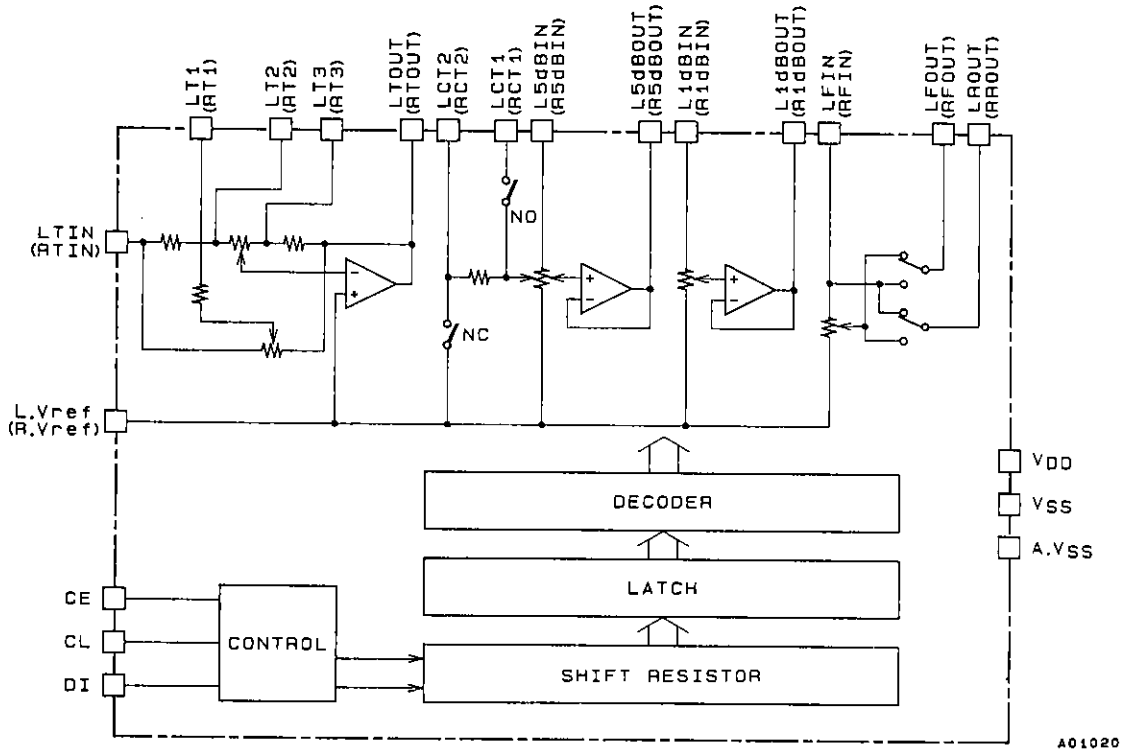
Note: 1. A capacitor rated at 2000 pF or less should be installed between all power supply pins and V<sub>SS</sub>.

**Electrical Characteristics at Ta = 25°C, VDD = 9 V, VSS = 0 V**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD (1)	V <sub>IN</sub> = 1 Vrms, f = 1 kHz, total overall flat		0.04		%
	THD (2)	V <sub>IN</sub> = 1 Vrms, f = 20 kHz, total overall flat		0.06		%
Crosstalk	CT	V <sub>IN</sub> = 1 Vrms, f = 1 kHz, total overall flat, R <sub>g</sub> = 1 kΩ	60	87		dB
Maximum Output Reduction	V <sub>o min</sub>	V <sub>IN</sub> = 1 Vrms, f = 1 kHz, main volume →∞, fader volume →∞, C = 1000 μF between Vref and V <sub>SS</sub> for L/R		82		dB
All Resistance Value	R <sub>VOL</sub> (1)	5 dB step	15	25	35	kΩ
	R <sub>VOL</sub> (2)	1 dB step	12	20	28	kΩ
	R <sub>FADER</sub>		12	20	28	kΩ
	R <sub>BASS</sub>		48	80	112	kΩ
	R <sub>TREBLE</sub>		30	50	70	kΩ
Input high level current	I <sub>IH</sub>	V <sub>I</sub> = 8 V (CL, CE, DI pins)			10	μA
Input low level current	I <sub>IL</sub>	V <sub>I</sub> = 0 V (CL, CE, DI pins)	-10			μA
Output noise voltage	V <sub>N</sub>	All overall flat (IHF-A), R <sub>g</sub> = 1 kΩ		7.5	15	μV
Current dissipation	I <sub>DD</sub>	V <sub>DD</sub> -V <sub>SS</sub> = 10 V		15	21	mA
Analog switch on resistance	R <sub>ON</sub>	CT1	1.8	3.0	4.2	kΩ
		Between CT2 and Vref	0.6	1.0	1.4	kΩ
		Fader S1 to S4	1.8	3.0	4.2	kΩ
		→∞	0.6	1.0	1.4	kΩ
		All other cases	6.0	10.0	14.0	kΩ

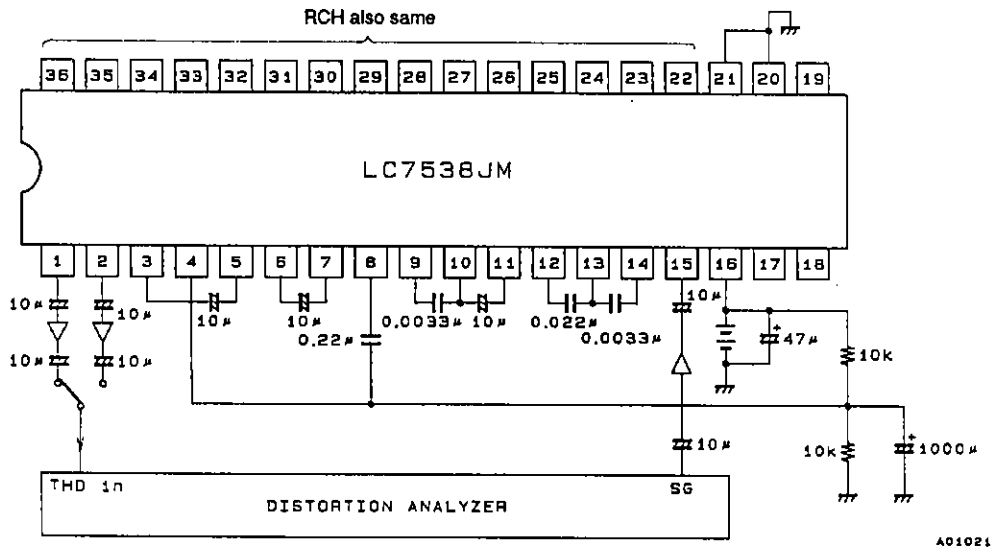
# LC7538JM

## Equivalent Circuit Block Diagram



## Test Circuit

### a) Total Harmonic Distortion



Unit (resistance: Ω, capacitance: F)



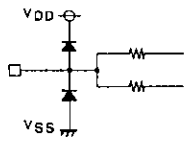
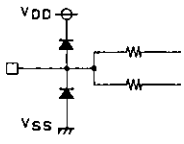
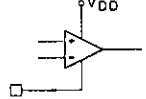
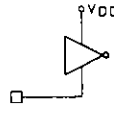
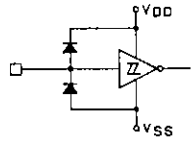
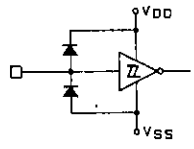
Pin Descriptions

Pin name	Pin No.	Description	Remarks
LROUT	1	<ul style="list-style-type: none"> <li>These pins function as output pins for the fader. Output reduction for rear and front is performed separately for each. Attenuation capacity is unified for both left and right. Step positioning is designed using an open circuit so that reception is performed using high impedance.</li> </ul>	<p style="text-align: right;">A02181</p>
LFOUT	2		
RROUT	36		
RFOUT	35		
LFIN	3	<ul style="list-style-type: none"> <li>When utilizing the fader function, these pins function as input pins.</li> <li>Low impedance driven.</li> </ul>	<p style="text-align: right;">A02182</p>
RFIN	34		
LVREF	4	<ul style="list-style-type: none"> <li>These pins are common pins for fader volume, tone and main volume. The pattern impedance connected here should be lowered as much as possible.</li> <li>LVref and RVref are not connected to VSS.</li> <li>Connections for LVref and RVref to VSS should be established externally to match all specifications. Notably, attention should be paid to capacity since capacitors are subject to residual resistance during volume output reduction when installed between LVref (RVref) and VSS as is the case with single power sources.</li> <li>Normally, high voltage applied from VDD.</li> </ul>	<p style="text-align: right;">A02183</p>
RVREF	33		
L1dBOUT	5	<ul style="list-style-type: none"> <li>These pins are output pins for the 1 dB step attenuator located in the section main volume.</li> </ul>	<p style="text-align: right;">A02184</p>
R1dBOUT	32		
L1dBIN	6	<ul style="list-style-type: none"> <li>These pins are input pins for the 1 dB step attenuator located in the section main volume.</li> <li>Low impedance driven.</li> </ul>	<p style="text-align: right;">A02182</p>
R1dBIN	31		
L5dBOUT	7	<ul style="list-style-type: none"> <li>These pins are output pins for the 5 dB step attenuator located in the section main volume.</li> </ul>	<p style="text-align: right;">A02184</p>
R5dBOUT	30		
LCT1	9	<ul style="list-style-type: none"> <li>These pins are for loudness control. Connect a high-band compensation capacitor between CT1 to 5dB IN and a low-band compensation capacitor between CT2 to Vref.</li> </ul>	
LCT2	8		
RCT1	28		
RCT2	29		
L5dBIN	10	<ul style="list-style-type: none"> <li>These pins are input pins for the 5 dB step attenuator located in the section main volume.</li> <li>Low impedance driven.</li> </ul>	<p style="text-align: right;">A02182</p>
R5dBIN	27		
LTOUT	11	<ul style="list-style-type: none"> <li>These pins are output pins for tone control.</li> </ul>	<p style="text-align: right;">A02185</p>
RTOUT	26		

Continued on next page.

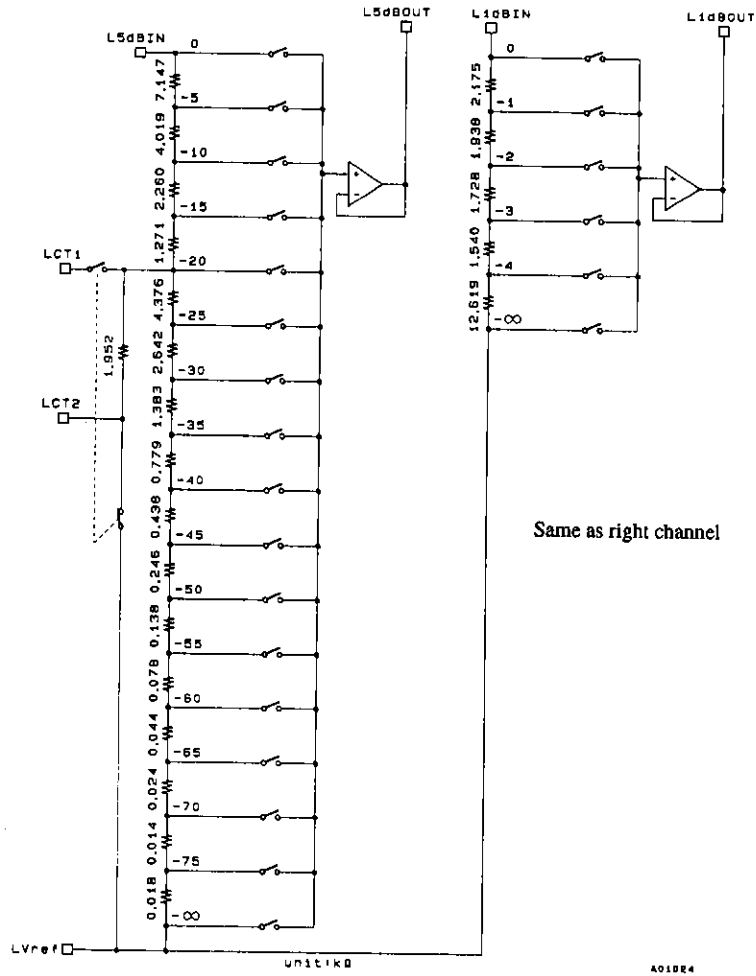
# LC7538JM

Continued from preceding page.

Pin name	Pin No.	Description	Remarks
LT3	12	<ul style="list-style-type: none"> <li>• These pins are for connecting bass and treble compensation for the tone circuit.</li> <li>• Connect a high-band compensation capacitor between T1 and T2.</li> <li>• Connect a low-band compensation capacitor between T2 and T3.</li> </ul>	 <p style="text-align: right;">A02106</p>
LT2	13		
LT1	14		
RT3	25		
RT2	24		
RT1	23		
LTIN	15	<ul style="list-style-type: none"> <li>• These pins are tone control input pins.</li> <li>• Low impedance driven.</li> </ul>	 <p style="text-align: right;">A02106</p>
RTIN	22		
VDD	16	<ul style="list-style-type: none"> <li>• Supply voltage pin.</li> </ul>	
A. VSS	21	<ul style="list-style-type: none"> <li>• Ground pin for on-chip op amp.</li> </ul>	 <p style="text-align: right;">A02107</p>
VSS	20	<ul style="list-style-type: none"> <li>• Ground pin for internal logic.</li> </ul>	 <p style="text-align: right;">A02108</p>
CE	17	<ul style="list-style-type: none"> <li>• This is the chip enable pin. According to the timing of the switch from high to low, data is written to an internal latch and all analog switches operate.</li> <li>• Data transfer with high-level switches to enable.</li> </ul>	 <p style="text-align: right;">A02109</p>
DI	18	<ul style="list-style-type: none"> <li>• These are input pins for the clock and serial data for control.</li> </ul>	 <p style="text-align: right;">A02109</p>
CL	19		

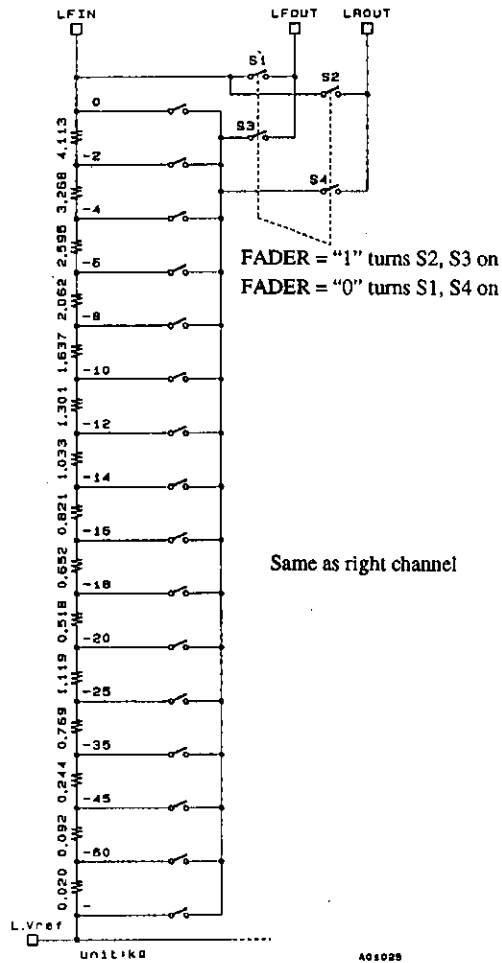
Equivalent Circuit for Main Volume Section

Unit (resistance:  $\Omega$ )



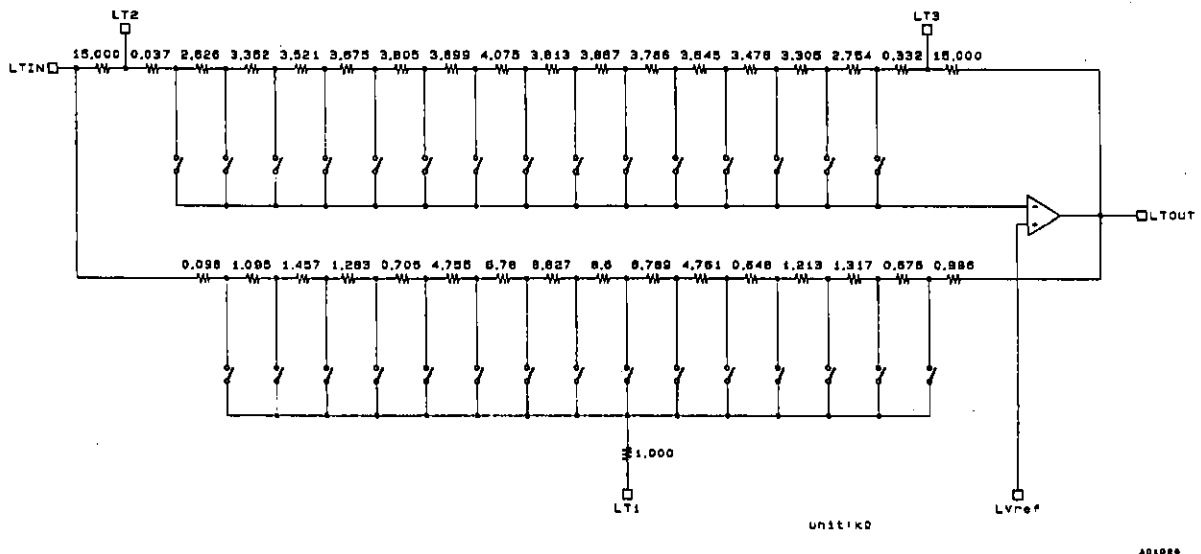
Equivalent Circuit for Fader Volume Section

Unit (resistance:  $\Omega$ )



When data of  $-\infty$  is transferred to main volume control 1 dB step, S1 and S2 open and S3, S4 are turned on simultaneously.

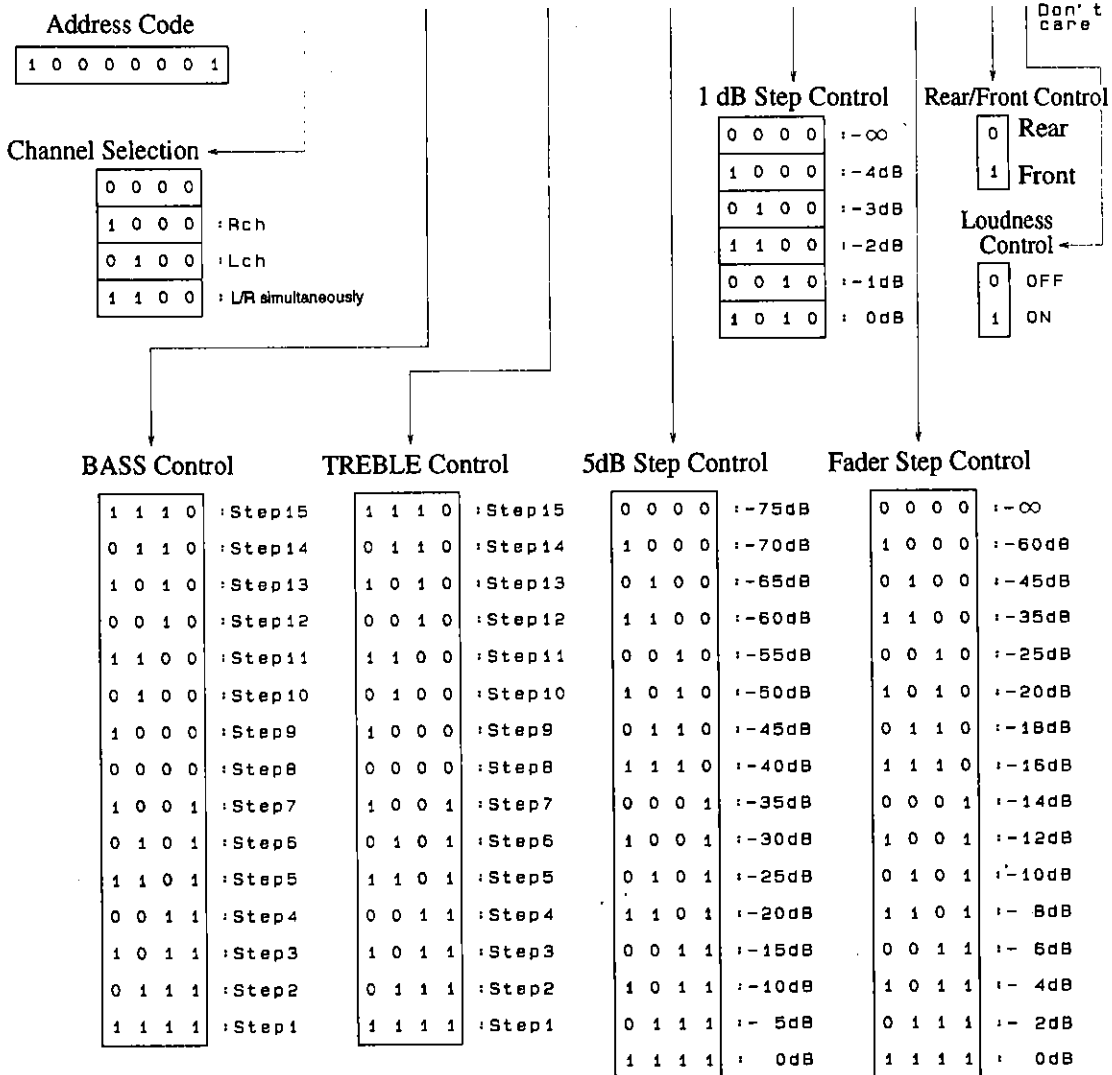
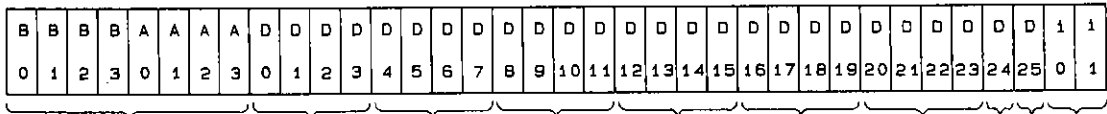
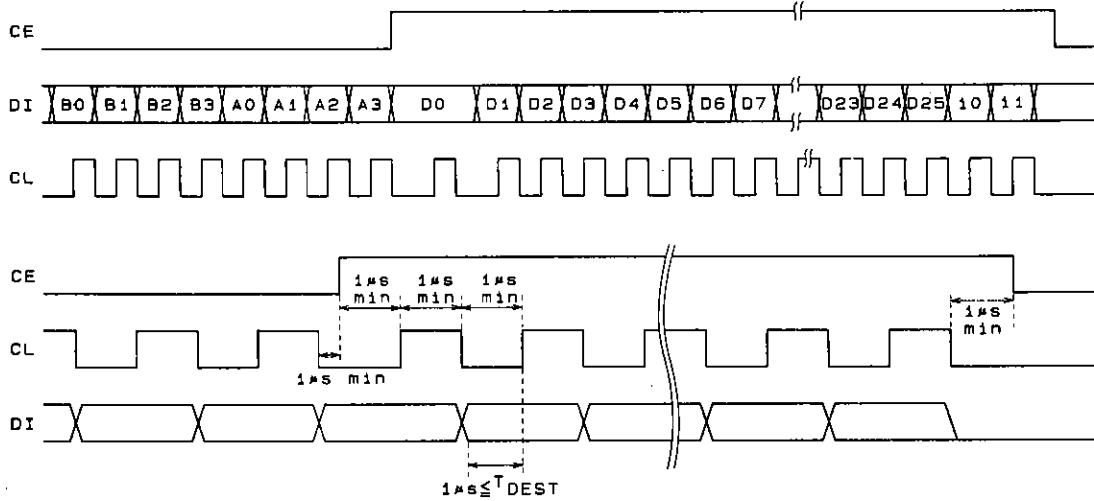
Equivalent Circuit for Tone Section





**Control System Timing and Data Format**

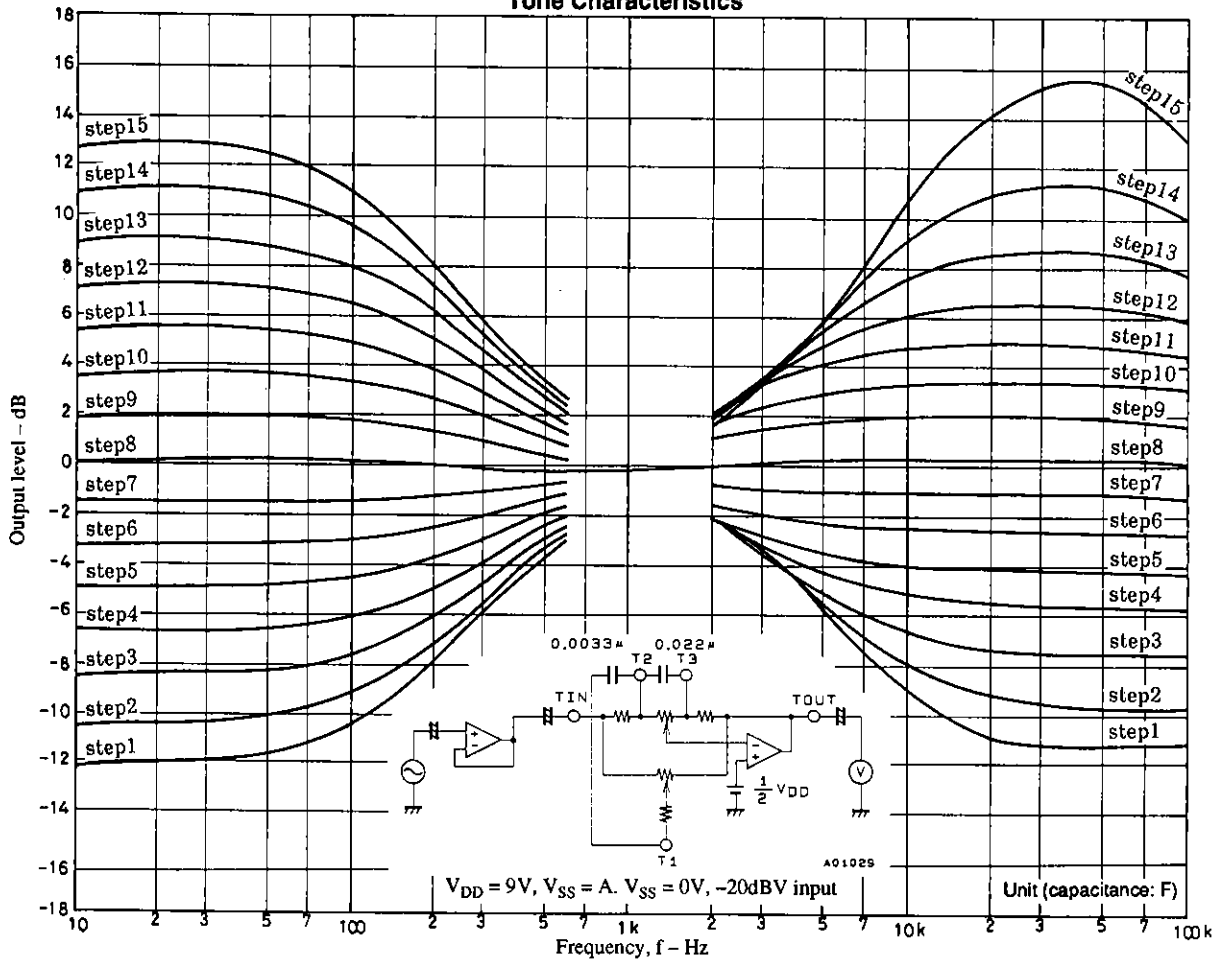
Controlling of LC7538JM involves the input of regulating serial data to CE, CL and DI pins. Data format consists of 36 bits composed of an 8-bit address and 28-bit data.



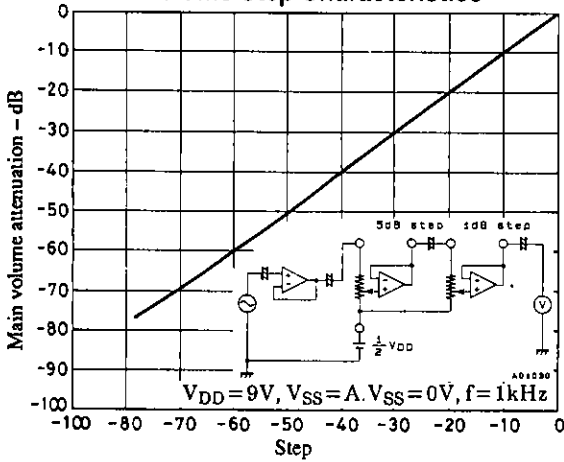
A01027



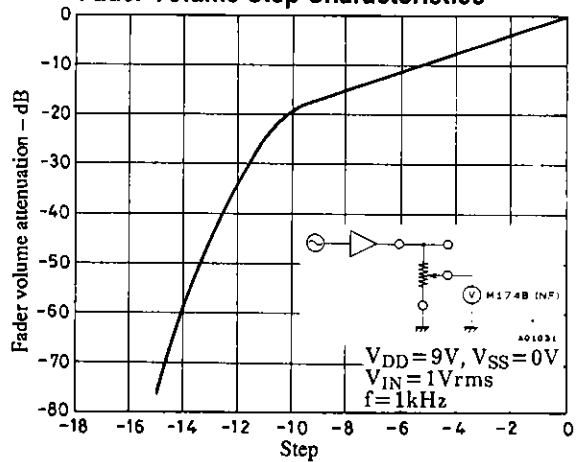
Tone Characteristics



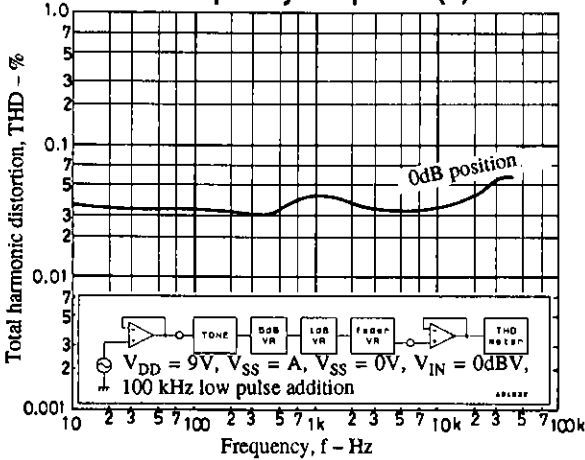
Main Volume Step Characteristics



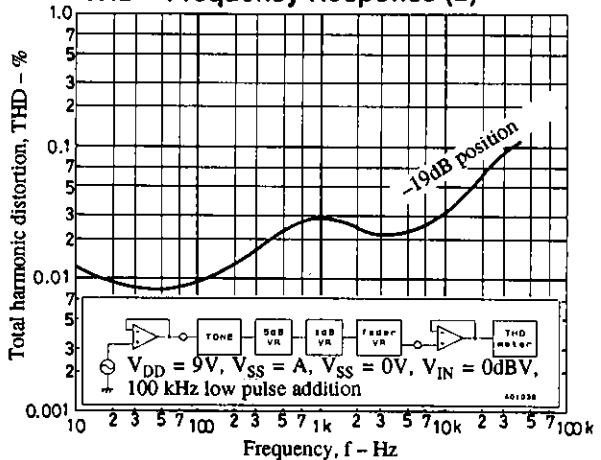
Fader Volume Step Characteristics



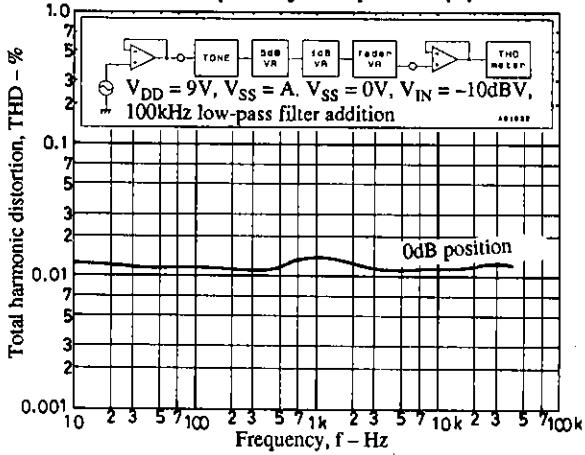
THD - Frequency Response (1)



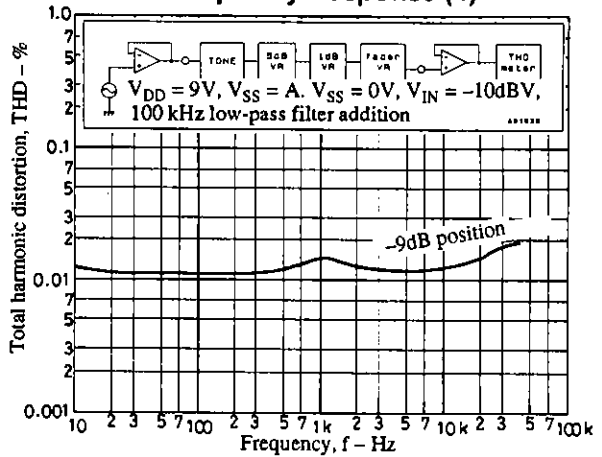
THD - Frequency Response (2)



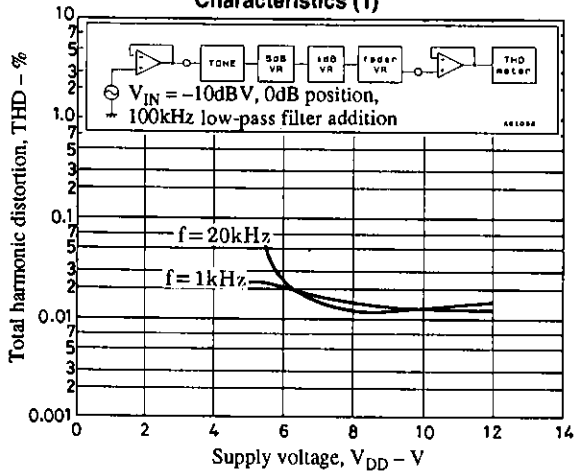
THD – Frequency Response (3)



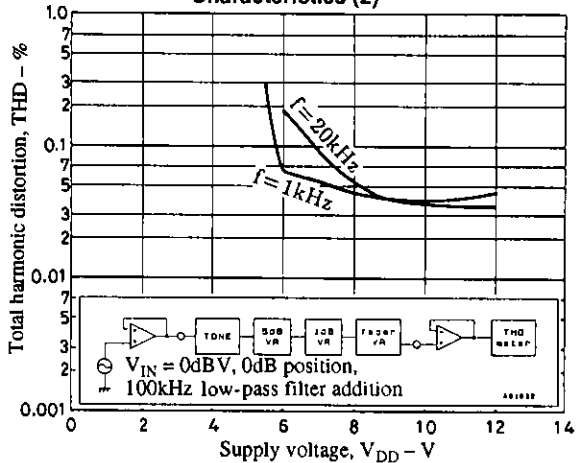
THD – Frequency Response (4)



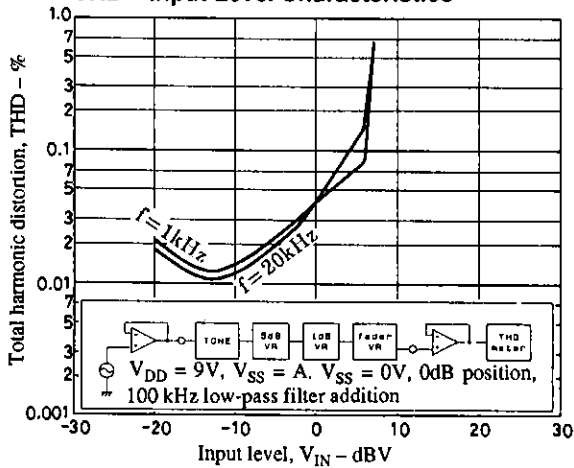
THD – Power Supply Voltage Characteristics (1)



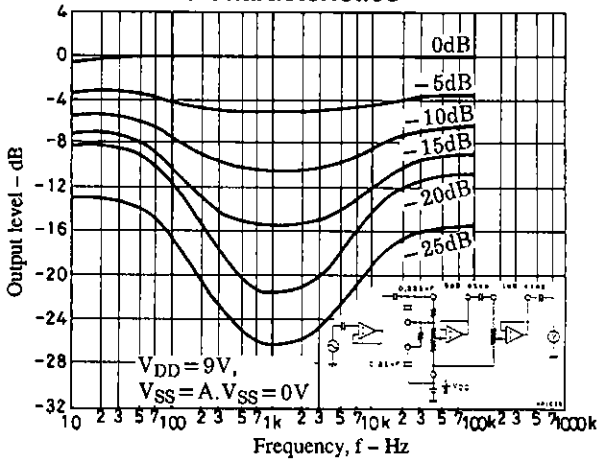
THD – Power Supply Voltage Characteristics (2)



THD – Input Level Characteristics



Loudness Characteristics



**Loudness External Constant Calculation Sample**

First, refer to page 7 where the 5 dB step internal equivalent circuit for the LC7538JM is shown. Using this information, an external constant for loudness can be added to establish a simplified circuit for computation as shown in Figure 1. Computations gaining a 5 dB boost with  $f = 100$  Hz using this configuration are shown in the following. ( $f = 100$  Hz and 5 dB boost)

Within figure 1, when R and C are defined as:

$$R1 = R2 = 10 \text{ k}\Omega$$

$$R3 = 1 \text{ k}\Omega$$

$C1 = Z1, C2 = Z2$ , then the following equation can be established:

$$V_{OUT} = \frac{\frac{R2(R3 + Z2)}{R2 + R3 + Z2}}{\frac{R1 \cdot Z1}{R1 + Z1} + \frac{R2(R3 + Z2)}{R2 + R3 + Z2}} = -20\text{dB}$$

(at = 1kHz)

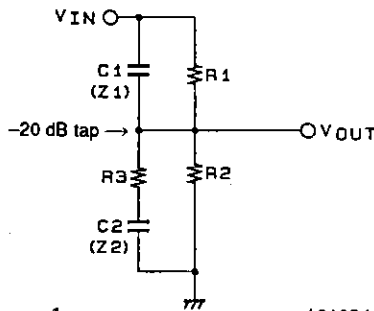
$$V_{OUT} = \frac{\frac{R2(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}}{\frac{R1 \cdot 10 \cdot Z1}{R1 + 10 \cdot Z1} + \frac{R2(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}} = -15\text{dB}$$

(at = 100Hz)

thereby resulting in,

$$Z1 \approx 178.3 \text{ k}\Omega \text{ and } Z2 = 176 \Omega.$$

Under such conditions where  $f = 1$  kHz, specifications may be satisfied if C (capacitor) having these impedances is supplied externally. The end result is that  $C1 = 893$  pF and  $C2 = 0.9$   $\mu$ F.



- R1, R2 and R3 : LC7538JM on-chip resistors
- C1 : External high-band compensation capacitor
- C2 : External low-band compensation capacitor

Figure 1

A01034

**Notes for Above Applications**

- When the power supply is turned on, the internal analog switch becomes inexact. Until data is set, counter measures such as those required for muting are performed externally.
- In order to prevent crossover into the analog system of high-frequency digital signals transferred to the CL, DI and CE pins, transfer along these signal lines should occur along shielded lines, or the signal lines should be protected by using the grounding pattern or the circuit.
- For volume steps with large attenuation levels (over -20 dB), when the loudness circuit is off the high frequency region (above about 4 kHz) will be attenuated by about 3 dB relative to the low frequency region (about 400 Hz) due to the influence of the resistance of the loudness circuit analog switch. Therefore we recommend using tone control compensation together with the volume step described above.
- When sending data immediately after power on, send data as follows:
  - When sending independent left and right data, send data at least four times.

$\overline{\text{Lch data}} \overline{\text{Rch data}} \overline{\text{Lch data}} \overline{\text{Rch data}} \dots$

- Alternatively, when sending data that drives the left and right channels at the same time, send the data at least twice.

$\overline{\text{L/R data}} \overline{\text{L/R data}} \dots$

•••••