SANYO No.2590

LA7096

Monolithic Linear IC

VTR Audio Signal Recording/Playback Processor

Functions

- Tape head select switches
- Power supply switch for OSC bias circuit
- Equalizer amp, line amp, ALC

Features

- The LA7096 is an IC that provides various functions (including two tape head select switches and a power supply switch for the OSC bias circuit) required for VTR audio signal recording/playback. The LA7096 is fabricated on a single chip and requires a minimum number of peripheral parts.

Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	$V_{CC}max$		15	V
Allowable Power Dissipation	Pdmax	(Ta=65°C)	600	mW
Operating Temperature	Topg		-10 to +65	°C
Storage Temperature	Tstg		-55 to +125	°C
Pin 1 Input Voltage	V_{1IN}		130(±65)	Vp-p
Pin 1 Input Current	I_{1IN}		±1.5	mA

Recommended Operating Conditions at Ta=25°C

			unit
Recommended Operating Voltage	V_{CC}	12.0	V
Operating Voltage Range	Vopr	11.5 to 12.5	V

Electrical Characteristics at Ta=25°C, V_{CC}=12V, f=1kHz, 0 dBv:1.0Vrms

			min	typ	max	unit
Current Dissipation (EE)	I_{CCE}	Quiescent	14.0	18.0	23.0	mA
(PB)	I_{CCP}	"	13.5	17.5	22.5	mA
(REC)	I_{CCR}	"	11.5	15.5	20.5	mA
Overall Gain at PB Mode	VG_{PB}	EQ IN to LINE OUT, V_O=-5dBv	67.0	68.5	70.0	dB
[Equalizer Amp]						
Open-Loop Voltage Gain	VG_{OE}	V_O=-5dBv	60.0	65.0		dB
Equivalent Input Noise Voltage	V_{NIE}	Rg=2.2kohms, DIN audio filter		1.0	1.8	uVrms
Input Resistance	Z_{INE}			140		kohm

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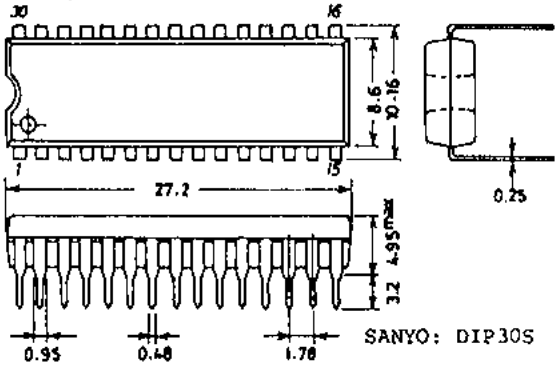
Case Outline 3061-D30SNIC
(unit:mm)



SANYO: DIP30S

Specifications and information herein are subject to change without notice.

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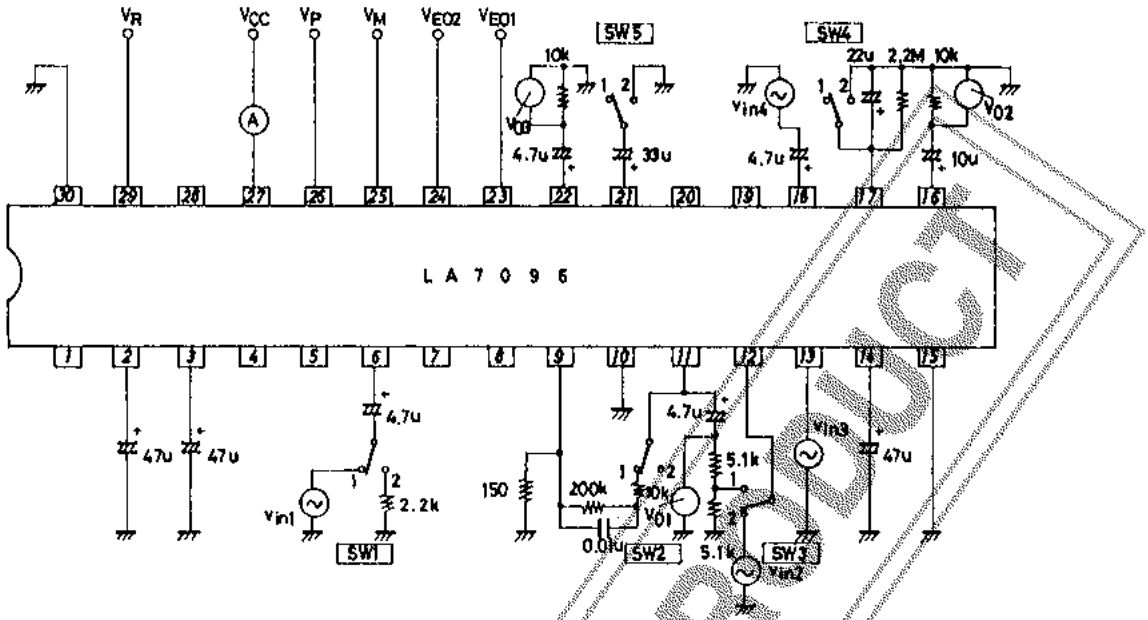
			min	typ	max	unit
[Line Amp]						
Voltage Gain (PB Input)	VG_{LP}	V_O=-5dBv	32.5	34.0	35.5	dB
(EE,REC Input)	VG_{LR}	"	32.5	34.0	35.5	dB
Total Harmonic Distortion	THD_L	"		0.15	0.4	%
Output Noise Voltage	V_{NOL}	PB mute ON, DIN audio filter		-71.0	-65.0	dBv
Input Resistance (PB Input)	Z_{IN1}			35.0		kohm
(EE,REC Input)	Z_{IN2}			35.0		kohm
Maximum Output Voltage	V_{OML}	THD=3%	2.7	3.2		Vrms
Output Voltage at ALC Mode	V_{OA}	Vin=-30dBv	-3.0	-1.5	0	dBv
ALC Effect	ALC	Vin=-30 to -10dBv		1.0	3.0	dB
Total Harmonic Distortion at ALC Mode	THD_A	Vin=-30dBv		0.2	0.6	%
[Recording Amp]						
Voltage Gain (Open Loop)	VG_{OR}	V_O=-5dBv	35.0	40.0		dB
(Closed Loop)	VG_{CR}	"	11.5	12.5	13.5	dB
Total Harmonic Distortion	THD_R	"		0.2	0.6	%
Input Resistance	Z_{INR}			35.0		kohm
Maximum Output Voltage	V_{OMR}	THD=3%	2.5	3.0		Vrms
[Muting Circuit]						
ON-State Voltage	V_{MON}	Pin25 DC	3.0		10	V
OFF-State Voltage	V_{MOF}	"	0		1.0	V
Muting Attenuation (PB)	M_P		85.0	90.0		dB
(REC)	M_R		75.0	80.0		dB
[PB/EE Select Circuit]						
PB Mode Hold Voltage	V_{PP}	Pin26 DC	3.8		10	V
EE Mode Hold Voltage	V_{PE}	"	0		1.0	V
[REC/EE Select Circuit]						
REC Mode Hold Voltage	V_{RR}	Pin29 DC	4.0		10	V
EE Mode Hold Voltage	V_{RE}	"	0		1.0	V
[Equalizer Select Circuit]						
Switch ON-State Voltage	V_{EON}	Pins23,24 DC	3.0		10	V
Switch OFF-State Voltage	V_{EOF}	"	0		0.8	V
[Head Select Switch]						
Pin 1 ON-State Resistance	R_{ON1}	I_1=±1mA		10	20	ohm
Pin 5 ON-State Resistance	R_{ON5}	I_5=±1mA		5	10	ohm
Pin 1 Leakage Current	I_{L1}	V_1=±50V			±10	uA
Pin 5 Leakage Current	I_{L5}	V_5=±0.1V			±2	uA

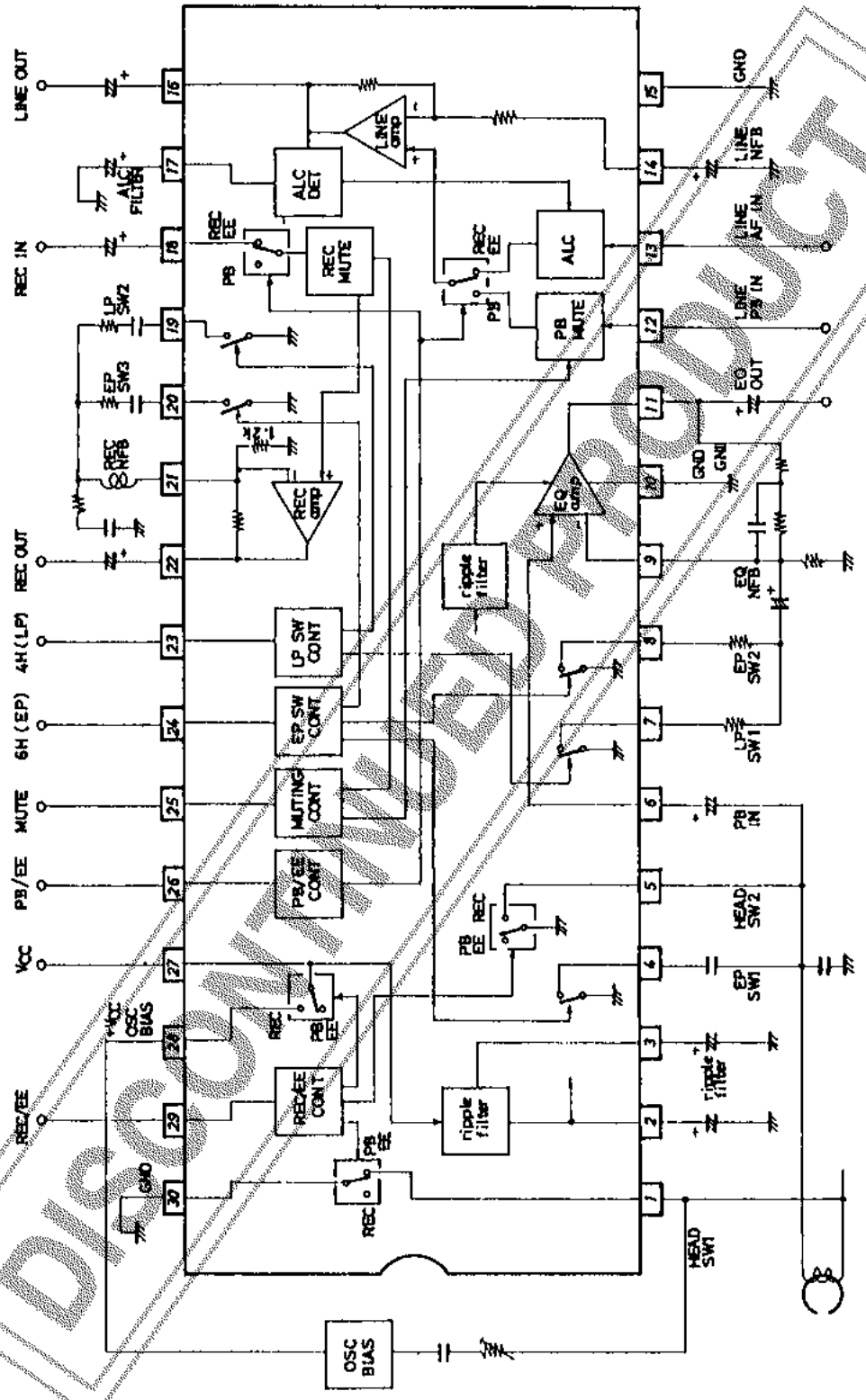
Test Circuit



Switch Operating Table

Item (Symbol)	SW1	SW2	SW3	SW4	SW5	VM	VP	VR	Input	Test
ICCE	2	1	1	2	1	GND	GND	GND	—	A
ICCP	2	1	1	2	1	GND	VCC	GND	—	A
ICCR	2	1	1	2	1	GND	GND	VCC	—	A
VGPB	1	1	1	2	1	GND	VCC	GND	VIN1	Vo2
VGOE	1	2	2	2	1	GND	VCC	GND	VIN1	Vo1
VNIL	2	1	2	2	1	GND	VCC	GND	—	Vo1
VGLP, THDL, VOML	2	1	2	2	1	GND	VCC	GND	VIN2	Vo2
VGLR	2	1	1	2	1	GND	GND	GND	VIN3	Vo2
VNOL	2	1	2	2	1	VCC	VCC	GND	—	Vo2
VOA, ALC, THDA	2	1	2	1	1	GND	GND	GND	VIN3	Vo2
VGOR	2	1	2	2	2	GND	GND	GND	VIN4	Vo3
VGCR, THDR, VOMR	2	1	2	2	1	GND	GND	GND	VIN4	Vo3
MP	1	1	1	2	1	VCC	VCC	GND	VIN1	Vo2
MR	2	1	1	2	1	VCC	GND	GND	VIN4	Vo3

Block Diagram



Sample Application Circuit