

LA7282, 7282M

VCR Audio Signal Recording / Playback Processor

Overview

The LA7282 and 7282M are small package ICs containing all functions necessary to record and playback VCR audio signal.

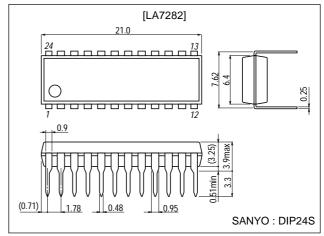
Features

- Small package leaves large space for other components.
- Delete of In and Output electrolysis capacitor.
- Low capacitor $(0.1\mu F)$ for the line amplifier inputs (PB IN and AUDIO IN)
- Non-Adjustment of PB Gain by less gain scatter.

Package Dimensions

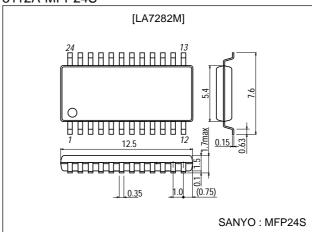
unit:mm

3067A-DIP24S



unit:mm

3112A-MFP24S



- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
- SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges,or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maxumum supply voltage	V _{CC} max		14	V
Pin 1 input voltage	V _{IN1}	Ta=65°C, f=80kHz (sin), I _{LK} =10μA	90 (±45)	Vp-p
Pin 1 input current	I _{IN1}		±1.5	mA
Allowable power dissipation	Pd max	Ta≤65°C, when mounted on the recommended PCB	400	mW
Operating temperature	Topr		-10 to +65	°C
Storage temperature	Tstg		-55 to +125	ů

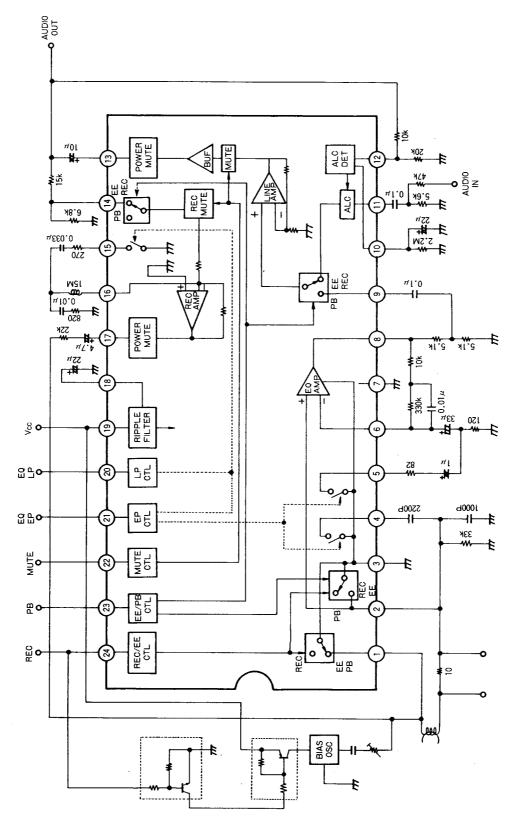
Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	Vcc		12.0	V
Operating voltage range	V _{CC} op		11.25 to 12.75	V

Operating Characteristics at Ta = 25°C, $V_{CC}=12V$, f=1kHz, 0dBv=:1.0Vrms

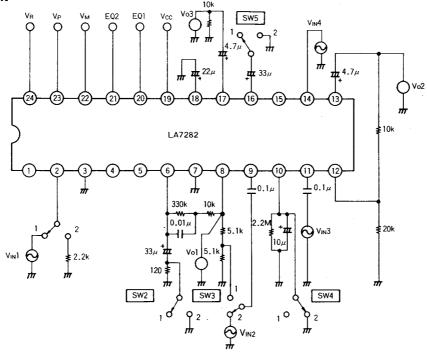
Parameter	Symbol	Conditions		Ratings		Unit	
i arameter	Symbol	Conditions	min	typ	max	Offic	
Current drain (FE)	ICCE	Quiescent	8.0	12.0	17.0	mA	
Current drain (PB)	ICCP	Quiescent	9.0	13.0	18.0	mA	
Current drain (REC)	ICCR	Quiescent	7.0	10.0	14.0	mA	
Overall gain at PB mode	VG _{PB}	EQ IN-LINE OUT, V _O =-5dBv	59.0	59.5	60.0	dB	
[Equalizing amplifier]							
Open loop voltage gain	VG _{OE}	V _O =-5dBv	66.0	71.0		dB	
Equivalent input noise voltage	V _{NIE}	Rg=2.2kΩ, DIN audio filter		1.2	1.8	μVrms	
Input impedance	Z _{INE}			130		kΩ	
[Line amplifier]							
Voltage gain (PB IN)	VG _{LP}	V _O =-5dBv	21.0	21.5	22.0	dB	
Voltage gain (EE, REC IN)	VG _{LR}	V _O =-5dBv	21.0	21.5	22.0	dB	
Total harmonic distortion	THDL	V _O =-5dBv		0.3	0.5	%	
Output noise voltage	V _{NOL}	DIN audio filter		-70.0	-64.0	dBv	
Input impedance (PB IN)	Z _{IN1}			120		kΩ	
Input impedance (EE, REC IN)	Z _{IN2}			120		kΩ	
Maximum output voltage	V _{OML}	THD=3%	1.5	2.1		Vrms	
Output voltage at ALC	VOA	V _{IN} =-28dBv	-9.0	-8.0	-7.0	dBv	
ALC Effect	ALC	V _{IN} =-28 to -8dBv		1.5	3.0	dB	
Total harmonic distortion at ALC	THDA	V _{IN} =-28dBv		0.25	0.6	%	
[Recording amplifier]	•		•				
Voltage gain (open loop)	VGOR	V _O =-5dBv	47.0	52.0		dB	
Voltage gain (closed loop)	VGCR	V _O =-5dBv	12.5	13.0	13.5	dB	
Total harmonic distortion	THDR	V _O =-5dBv		0.1	0.3	%	
Input impedance	Z _{INR}			50		kΩ	
Maximum output voltage	Z _{OMR}	THD=3%	1.5	2.0		Vrms	
[Muting circuit]	'		•				
On voltage	V _{MON}	Pin 22, DC	3.8		6.0	V	
Off voltage	V _{MOFF}	Pin 22, DC	0		1.0	V	
Mute attenuation level (PB, EE)	M _P , M _E		80.0	90.0		dB	
Mute attenuation level (REC)	MR		65.0	70.0		dB	
[PB/EE selector circuit]	'		•				
PB mode hold voltage	V _{PP}	Pin 23, DC	0		1.0	V	
EE mode hold voltage	VPE	Pin 23, DC	3.3		6.0	V	
[REC/EE selector circuit]							
REC mode hold voltage	V _{RR}	Pin 24, DC	3.3		V _{CC}	V	
EE mode hold voltage	V _{RE}	Pin 24, DC	0		1.0	V	
[Equalizer selector circuit]	,						
Switch on voltage	VEON	Pin 20, 21, DC	3.5		6.0	V	
Switch off voltage	VEOFF	Pin 20, 21, DC	0		0.8	V	
[Head selector switch]	, 20.1		· · · · · · · · · · · · · · · · · · ·				
Pin 1 on resistance	R _{ON1}	I1=±1mA		15	30	Ω	
Pin 2 on resistance	R _{ON2}	I2=±1mA		5	10	Ω	
Pin 1 input voltage	V _{IN1}	Ta=65°C, f=80kHz (sin), ILK=10μA			±45	V	

Block Diagram



Unit (resistance : Ω , capacitance : F)

Test Circuit

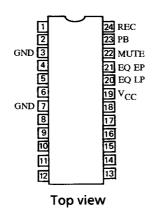


Unit (resistance : Ω , capacitance : F)

<Switch Setting Table>

Parameter (Symbol)	SW1	SW2	SW3	SW4	SW5	v _M	V _P	٧ _R	Input	Measurement
ICCE	2	1	1	2	1	GND	5V	GND	-	A
ICCP	2	1	1	2	1	GND	GND	GND	_	A
ICCR	2	1	1	2	1	GND	5V	5V	_	A
VG _{PB}	1	1	1	2	1	GND	GND	GND	V _{IN} 1	V _O 2
VG _{OE}	1	2	2	2	1	GND	GND	GND	V _{IN} 1	V _O 1
V _{NIE}	2	1	2	2	1	GND	GND	GND	-	V _O 1
VG _{LP} , THD _L , V _{OML}	2	1	2	2	1	GND	GND	GND	V _{IN} 2	V _O 2
VG _{LR}	2	1	1	2	1	GND	5V	GND	V _{IN} 3	V _O 2
V _{NOL}	2	1	2	2	1	GND	5V	GND	_	V _O 2
V _{OA} , ALC, THD _A	2	1	2	1	1	GND	5V	GND	V _{IN} 3	V _O 2
VGOR	2	1	2	2	2	GND	5V	GND	V _{IN} 4	V _O 3
VG _{CR} , THDR, V _{OMR}	2	1	2	2	1	GND	5V	GND	V _{IN} 4	V _O 3
MP	1	1	1	2	1	5V	GND	GND	V _{IN} 1	V _O 2
M _R	2	1	1	2	1	5V	5V	GND	V _{IN} 4	V _O 3
ME	2	1	2	2	1	5V	5V	GND	V _{IN} 2	V _O 2

Pin Assignment



LA7282, 7282M

Pin Functions Unit (resistance : Ω)

amount of the PB EQ AMP. On resistance: 15Q, typ. (playback EP mode) On resistance: 15Q, typ. (playback EP mode) Input impedance: 12ALD, typ. (playback EP mode) Input of negative feedback of the EQ AMP to establish desired equalizing characteristics. 7 GND 7 GND 8 EQ AMP Output 9 LINE AMP PB Input Be signal to the EQ AMP. The input impedance of pin 9 is high (120kg) and requires a small coupling capacitor of 0.1µF. 10 ALC FILTER 10 ALC FILTER 11 LINE AMP Audio Input 12 ALC Detect input 13 LINE AMP Output 14 REC AMP Input 15 ALC Detect input 16 ALC Detect input 17 ALC Detect input 18 ALC Detect input 19 ALC Detect input 19 ALC Detect input 10 ALC PILTER 10 Output impedance: 50Q, typ. 11 Input recording signal from LINE AMP. 11 Input recording signal from LINE AMP. 12 Input recording signal from LINE AMP. 13 Input recording signal from LINE AMP. 14 REC AMP Input 15 Input recording signal from LINE AMP. 16 Input recording signal from LINE AMP. 17 Input recording signal from LINE AMP. 18 Input current is set by the divider consisting of R1 and R2. 18 Input current is set by the divider consisting of R1 and R2. 19 Input recording signal from LINE AMP. 19 Input current is set by the divider consisting of R1 and R2. 19 Input current is set by the divider consisting of R1 and R2. 19 Input current is set by the divider consisting of R1 and R2. 19 Input current is set by the divider consisting of R1 and R2. 19 Input current is set by the divider consisting of R1 and R2. 19 Input current is set by the divider consisting of R1 and R2. 19 Input current is set by the divider consisting of R1 and R2. 19 Input current is set by the divider consisting of R1 and R2. 19 Input current is set by the divider consisting of R1 and R2. 19 Input	u.	ictions	Unit (resistance : \$2)	/ -
On resistance: 100, type. 2	Pin No.	Function	Terminal Circuit	Description
2	1			On resistance : 10Ω , type.
Sets the tight resource frequency. On resistance: 1504 typ. Input impedance: 120kL, typ. (playback EP mode) Input of the PB EO AMP. On resistance: 120kL, typ. (playback EP mode) Input of the PB EO AMP. On resistance: 120kL, typ. (playback EP mode) Input of regative freedback of the EQ AMP to establish desired equalizing otheracteristics. For amail coupling capacitor of 0.1µE. Input EE, REC signal. Input EE,	2	and	130 k	Input playback signal to the head. Input impedance : $130k\Omega$, typ. EE, REC : on ; PB : off
On resistance: 126kL typ. (playback EP mode) 1 EP Switch 2 1 Input Impedance: 126kL typ. (playback EP mode) 1 Input BE DA AMP. 1 GND 1 Common return for all circuits except for EQ AMP and head switch 1. 2 GND 3 EQ AMP Output 1 Input PB signal to the EQ AMP. The input impedance of pin 9 is high (120kL) and requires a small coupling capacitor of 0.1µE. 10 ALC FILTER 10 ALC FILTER 11 LINE AMP Audio Input 12 ALC Detect Input 12 ALC Detect Input 13 LINE AMP Output 14 REC AMP Input 15 Input EE, REC signal. The input impedance of pin 11 is high (120kΩ) and requires a small coupling capacitor of 0.1µE. 14 REC AMP Input 15 Input EE, REC signal. The input impedance of pin 11 is high (120kΩ) and requires a small coupling capacitor of 0.1µE. 16 Input EE, REC signal. The input impedance of pin 11 is high (120kΩ) and requires a small coupling capacitor of 0.1µE. 17 Accepts the output signal of LINE amplifier. The ALC level is determined by the voltage divide consisting of R₁ and R₂. 18 Input recording signal from LINE AMP. Input current is set by the divider consisting of R₁ and R₂. 2 Rec AMP Input 14 REC AMP Input 15 Input recording signal from LINE AMP. Input current is set by the divider consisting of R₁ and R₂. 2 Rec AMP Input 14 REC AMP Input 15 Input recording signal from LINE AMP. Input current is set by the divider consisting of R₁ and R₂. 2 Rec AMP Input 16 Input recording signal from LINE AMP. Input current is set by the divider consisting of R₁ and R₂. 2 Rec AMP Input 1 Input recording signal from LINE AMP. Input current is set by the divider consisting of R₁ and R₂. 2 Rec AMP Input are one to lower and as inverting amplifier. Input current is set by the divider consisting of R₁ and R₂.	3	GND		An exclusive GND for pin 1 head switch 1, EQ AMP and playback EP switch.
amount of the PB EQ AMP. On resistance: 15Ω, typ. [Input impedance: 15Ω, typ. [Input	4	EP Switch 1	120k \$	On resistance : 15Ω typ.
Input of negative feedback of the EQ AMP to establish desired equalizing characteristics. Page 1	5	EP Switch 2	12k \$	On resistance : 15Ω , typ.
Select value of R ₁ and R ₂ so that the reference input is at the shoulder of the ALC. ALC PILTER Input EE, REC signal. Rec AMP input Select value of R ₁ and R ₂ so that the reference input is at the shoulder of the ALC. The amplifier gain should be set for 21.5dB. The input impedance of pin 9 is high (120kΩ) and requires a small coupling capacitor enables detection. The RC time constant sets attack recovery time. Input EE, REC signal. Rec amplifier gain should be set for 21.5dB. The input impedance of pin 11 is high (120kΩ) and requires a small coupling capacitor of 0.1μF. ALC Detect Input Rec AMP input Accepts the output signal of LINE amplifier. The ALC level is determined by the voltage divide consisting of R ₁ and R ₂ . Input recording signal from LINE AMP. Input current is set by the divider consisting of R1 and R2. Pin 4 requires no coupling capacitor since REC AMplication is to operate at zero level and as inverting amplifier. Rec AMP in the reference input is at the shoulder of the ALC. Input current is set by the divider consisting of R1 and R2. Pin 4 requires no coupling capacitor since REC AMplication Rec AMP in the reference input is at the shoulder of the ALC. Pin 4 requires no coupling capacitor since REC AMplication Rec AMP in the reference input is at the shoulder of the ALC. Pin 4 requires no coupling capacitor since REC AMplication Rec AMP in the reference input is at the shoulder of the ALC. Pin 4 requires no coupling capacitor since REC AMplication Rec AMP in the reference input is at the shoulder of the ALC. Pin 4 requires no coupling capacitor since REC AMplication Rec AMP in the reference input is at the shoulder of the ALC. Pin 4 requires no coupling capacitor since REC AMplication Rec AMP in the reference input is at the shoulder of the ALC. Pin 4 requires no coupling capacitor since REC AMplication Rec AMP in the reference input is at the shoulder of the ALC. Pin 4 requires no coupling capacitor since REC AMplica	6	EQ AMP NFB		
Input PB signal to the EQ AMP. The input impedance of pin 9 is high (120kΩ) and requires a small coupling capacitor of 0.1µF. Connecting this pin to GND through a capacitor enables detection. The RC tim constant sets attack recovery time. Input EE, REC signal. The amplifier gain should be set for 21.5dB. The input impedance of pin 11 is high (120kΩ) and requires a small coupling capacitor of 0.1µF. ALC Detect Input ALC Detect Input RI ALC Detect Input RI ALC Detect Input RI ACCEPTS the output signal of LINE amplifier. The ALC level is determined by the voltage divide consisting of R1 and R2. Input recording signal from LINE AMP. Input current is set by the divider consisting of R1 and R2. Pin 14 requires no coupling capacitor since REC AMP is to operate at zero level and as inverting amplifier.	7	GND		Common return for all circuits except for EQ AMP and head switch 1.
Input EE, REC signal. Input EE, REC signal. Input EE, REC signal. The amplifier gain should be set for 21.5dB. The input impedance of pin 11 is high (120kΩ) and requires a small coupling capacitor of 0.1μF. ALC Detect Input ALC Detect Input REC AMP Input REC AMP Input Input recording signal from LINE AMP. Input recording signal from LINE AMP. Input tourrent is set by the divider consisting of R1 and R2. Input tourrent is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2. Input current is set by the divider consisting of R1 and R2.	8	EQ AMP Output	8	
constant sets attack recovery time. Input EE, REC signal. RI REC at spinal Select value of R₁ and R₂ so that the reference input is at the shoulder of the ALC. The amplifier gain should be set for 21.5dB. The input impedance of pin 11 is high (120kΩ) and requires a small coupling capacitor of 0.1μF. ALC Detect Input Accepts the output signal of LINE amplifier. The ALC level is determined by the voltage divide consisting of R₁ and R₂. Output impedance : 50Ω, typ. Input current is set by the divider consisting of R1 and R₂. Pin 14 requires no coupling capacitor since REC AM is to operate at zero level and as inverting amplifier. Pin 14 requires no coupling capacitor since REC AM is to operate at zero level and as inverting amplifier. Pin 14 requires no coupling capacitor since REC AM is to operate at zero level and as inverting amplifier.	9		(9) 120k (9)	
Input R1	10	ALC FILTER	(10)	Connecting this pin to GND through a capacitor enables detection. The RC time constant sets attack recovery time.
Accepts the output signal of LINE amplifier. The ALC level is determined by the voltage divide consisting of R ₁ and R ₂ . 13 LINE AMP Output Output impedance : 50Ω, typ. Input current is set by the divider consisting of R1 and R2. Pin 14 requires no coupling capacitor since REC AM is to operate at zero level and as inverting amplifier.	11		- -	Select value of R_1 and R_2 so that the reference input is at the shoulder of the ALC. The amplifier gain should be set for 21.5dB. The input impedance of pin 11 is high (120k Ω) and requires a small coupling
14 REC AMP Input Input recording signal from LINE AMP. Input current is set by the divider consisting of R1 an R2. Pin 14 requires no coupling capacitor since REC AM is to operate at zero level and as inverting amplifier	12	ALC Detect Input	120k ≸	Accepts the output signal of LINE amplifier. The ALC level is determined by the voltage divider
Input current is set by the divider consisting of R1 an R2. Pin 14 requires no coupling capacitor since REC AM is to operate at zero level and as inverting amplifier	13	LINE AMP Output	(3	Output impedance : 50Ω , typ.
	14	REC AMP Input	(14) w p 1 12k ≸	Input current is set by the divider consisting of R1 and

Continued on next page.

LA7282, 7282M

Continued from preceding page.

Unit (resistance : Ω)

Pin No.	Function	Terminal Circuit	Description					
15	LP Switch	(5) 60k	Sets the high peaking point to the frequency suitable for LP. On resistance : 15Ω typ. Input impedance : $60k\Omega$ typ.					
16	REC AMP NFB	RNF RE 1.5k	Connecting an L, C, R network to this pin causes a peaking frequency to rise.					
17	REC AMP Output	17	Output impedance : 40Ω typ.					
18	Ripple Filter	Each AMP Vcc 19	Connecting a electrolytic capacitor across this pin and GND smoothes ripples.					
19	Supply Voltage (V _{CC})		V _{CC} =15V max V _{CC} =11.25 - 12.75V typ.					
20	LP Control	20 10k	Applying 3.5V DC or more (6.0V max) to this pin turns on LP switch (pin 15). The switch turns off at 0.8V or below.					
21	EP Control	2) 10k	Applying 3.5V DC or more (6.0V max.) to this pin turns on EP switch (pin 4, 5) and LP switch (pin 15). The switches turn off at 0.8V or below.					
22	MUTE Control		Applying 3.8V DC or more (6.0V max.) to this pin turns on mute circuit. The mute is desabled at 1.0V or below. [Control mode]					
			Mode MUTE [L] MUTE [H]					
		22 10k	LINE AMP REC AMP LINE AMP REC AMP					
		100k	PB Mode					
		<u> </u>	REC Mode O O O ×					
			[O: Pass signal, ×: Block signal]					
23	PB Control	23 10k	Applying 3.3V DC or more (6.0V max.) to this pin enters EE mode and 1.0V or below PB mode.					
24	REC Control	24 10k	Applying 3.0V DC or more (up to VCC) to this pin enters REC mode and 1.0V or below EE mode.					

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of October, 2000. Specifications and information herein are subject to change without notice.