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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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# HA17324A Series

## Quad Operational Amplifier

ADE-204-031B (Z)

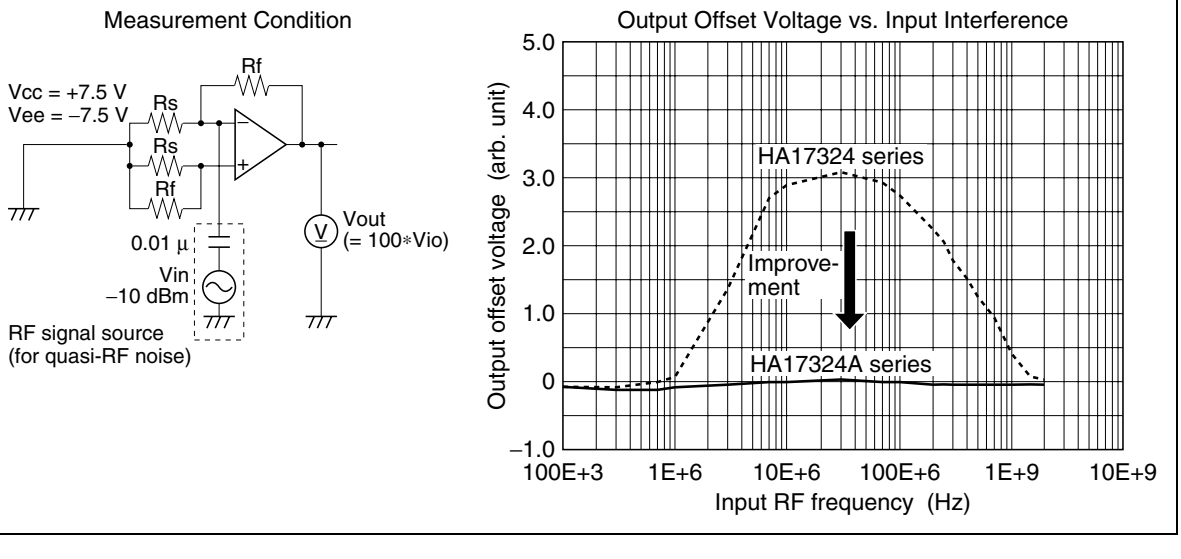
Rev.2
May 2001

## Description

HA17324A series are quad operational amplifier that provide high gain and internal phase compensation, with single power supply. They can be widely used to control equipments.

## Features

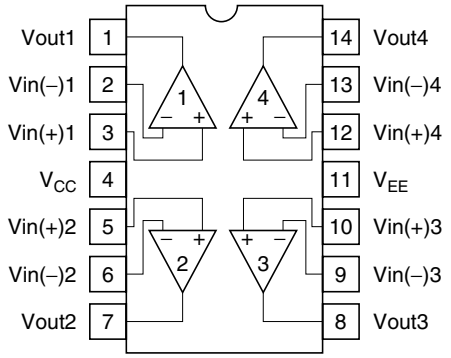
- Wide range of supply voltage, and single power supply used
- Internal phase compensation
- Wide range of common mode voltage, and possible to operate with an input about 0 V
- Low electro-magnetic susceptibility level



## Ordering Information

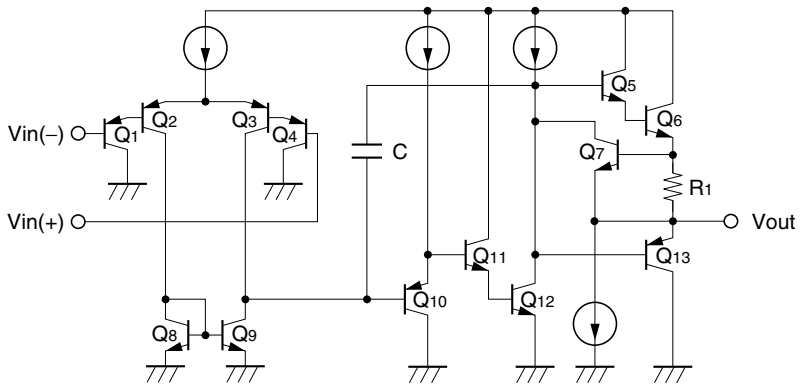
| Type No. | Application | Package |
|---|---|---|
| HA17324A | Commercial use | DP-14 |
| HA17324AF | | FP-14DA |
| HA17324ARP | | FP-14DN |

## Pin Arrangement




(Top view)

## Circuit Schematic (1/4)

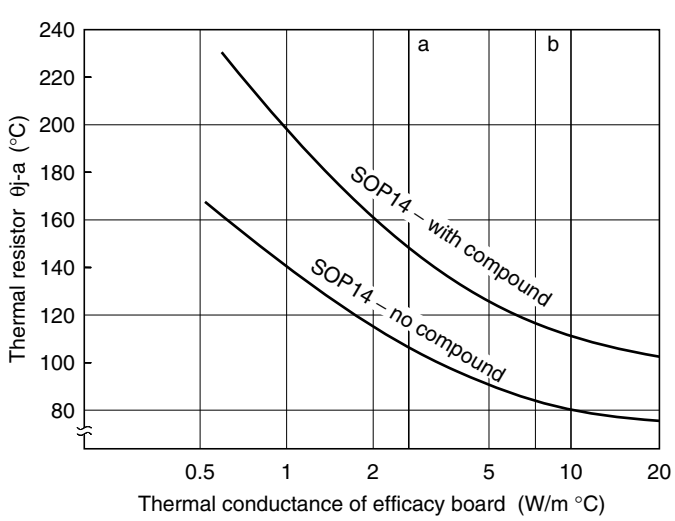


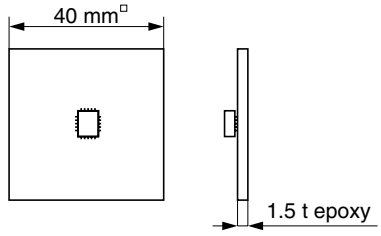
## Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 32 | V |
| Sink current | Isink | 50 | mA |
| Power dissipation | $P_T$ | 625 *1,2 | mW |
| Common mode input voltage | $V_{CM}$ | –0.3 to $V_{CC}$ | V |
| Differential input voltage | Vin (diff) | $\pm V_{CC}$ | V |
| Operating temperature | Topr | –40 to +85 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |

Notes: 1. For the DILP package.
This is the allowable values up to Ta = 50°C. Derate by 8.3 mW/°C.
2. For the SOP package.
Tjmax = θj-a · $P_C$max + Ta (θj-a; Thermal resistor between junction and ambient at set board use).
The wiring density and the material of the set board must be chosen for thermal conductance of efficacy board.
And $P_C$max cannot be over the value of $P_T$.




a. Class epoxy board of 10% wiring density
b. Class epoxy board of 30% wiring density

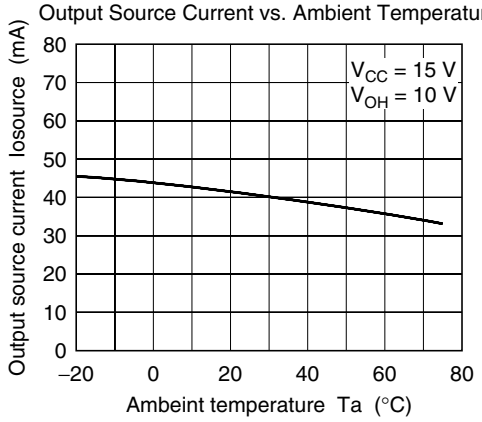
## Electrical Characteristics

($V_{CC}$ = +15 V, Ta = 25°C)

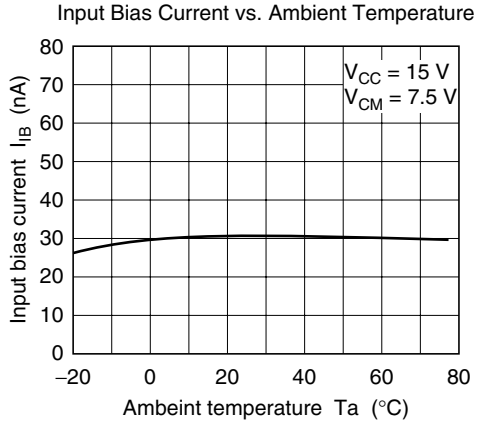
| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input offset voltage | $V_{IO}$ | — | 2 | 7 | mV | $V_{CM}$ = 7.5 V, $R_S$ = 50 Ω, Rf = 50 kΩ |
| Input offset current | $I_{IO}$ | — | 5 | 50 | nA | $V_{CM}$ = 7.5 V, $I_{IO}$ = \| $I_{I(-)} - I_{I(+)}$ \| |
| Input bias current | $I_{IB}$ | — | 30 | 500 | nA | $V_{CM}$ = 7.5 V |
| Power source rejection ratio | PSRR | — | 93 | — | dB | f = 100 Hz, $R_S$ = 1 kΩ, Rj = 100 kΩ |
| Voltage gain | $A_{VD}$ | 75 | 90 | — | dB | $R_S$ = 1 kΩ, Rf = 100 kΩ, $R_L$ = ∞ |
| Common mode rejection ratio | CMR | — | 80 | — | dB | $R_S$ = 50 Ω, Rf = 5 kΩ |
| Common mode input voltage range | $V_{CM}$ | –0.3 | — | 13.5 | V | $R_S$ = 1 kΩ, Rf = 100 kΩ, f = 100 Hz |
| Maximum output voltage | Vop-p | — | 13.6 | — | V | f = 100 Hz, $R_S$ = 1 kΩ, Rf = 100 kΩ, $R_L$ = 20 kΩ |
| Output source current | Iosource | 20 | 40 | — | mA | $V_{IN}^+$ = 1 V, $V_{IN}^-$ = 0 V, $V_{OH}$ = 10 V |
| Output sink current | Iosink | 10 | 20 | — | mA | $V_{IN}$ = 0 V, $V_{IN}$ = 1 V, $V_{OL}$ = 2.5 V |
| Supply current | $I_{CC}$ | — | 0.8 | 2 | mA | $V_{IN}$ = GND, $R_L$ = ∞ |
| Slew rate | SR | — | 0.19 | — | V/µs | f = 1.5 kHz, $V_{CM}$ = 7.5 V, $R_L$ = ∞ |
| Channel separation | CS | — | 120 | — | dB | f = 1 kHz |
| Output sink current | Iosink | 15 | 50 | — | µA | $V_{IN}^+$ = 0 V, $V_{IN}^-$ = 1 V, $V_{OL}$ = 200 mV |
| | Iosink | 3 | 9 | — | mA | $V_{IN}^+$ = 0 V, $V_{IN}^-$ = 1 V, $V_{OL}$ = 1 V |
| Output voltage | $V_{OH}$ | 13.2 | 13.6 | — | V | $I_{OH}$ = –1 mA |
| | $V_{OH}$ | 12.0 | 13.3 | — | V | $I_{OH}$ = –10 mA |
| Output voltage | $V_{OL}$ | — | 0.8 | 1.0 | V | $I_{OL}$ = 1 mA |
| | $V_{OL}$ | — | 1.1 | 1.8 | V | $I_{OL}$ = 10 mA |

## Characteristic Curves

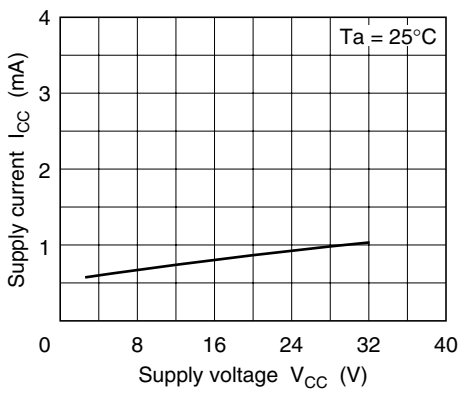
Output Source Current vs. Ambient Temperature



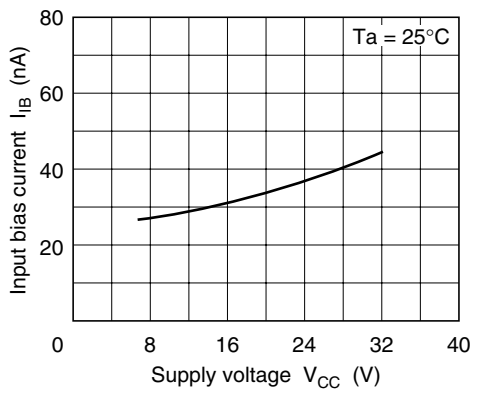

Input Bias Current vs. Ambient Temperature



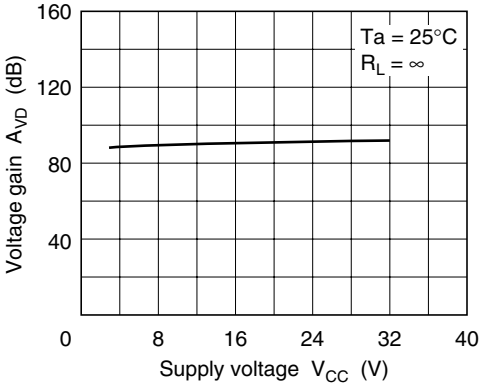

Supply Current vs. Supply Voltage



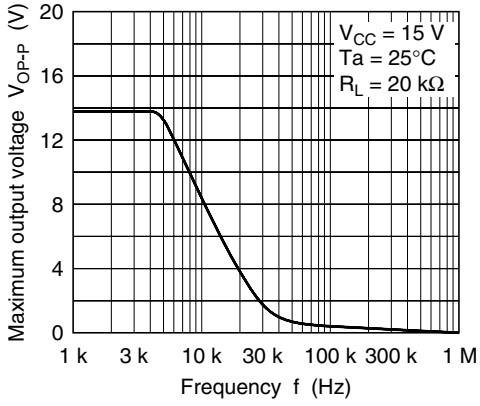

Input Bias Current vs. Supply Voltage



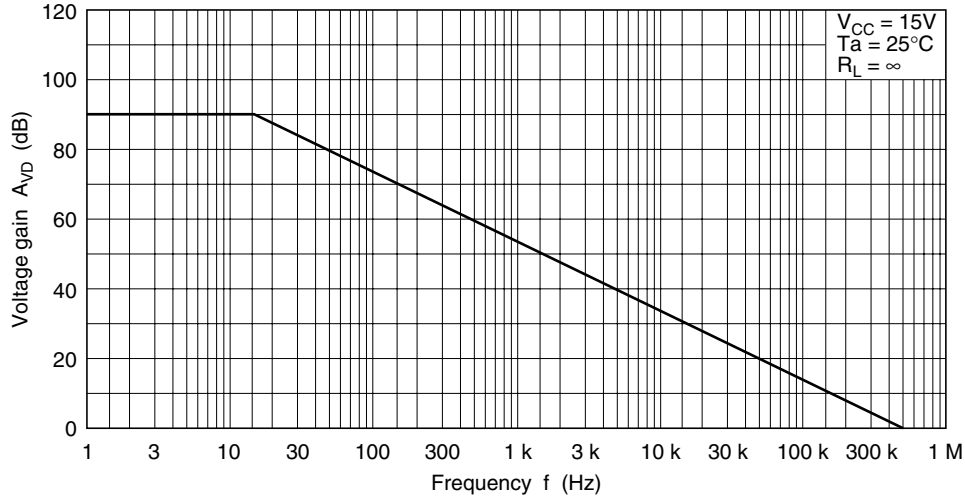

Voltage Gain vs. Supply Voltage



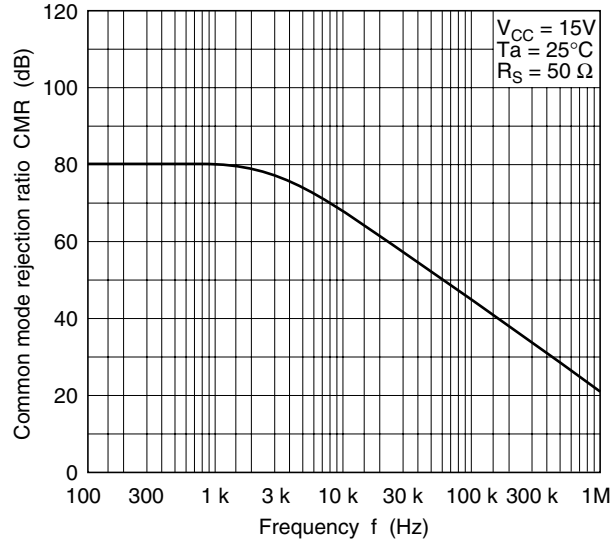

Maxlmum Output Voltage vs. Frequency



Voltage Gain vs. Frequency




Common Mode Rejection Ratio vs. Frequency



## Solder Mounting Method

1. Small and light surface-mount packages require spicial attentions on solder mounting.
   On solder mounting, pre-heating before soldering is needed.
   The following figure show an example of infrared rays refow.
2. The difference of thermal expansion coefficeient between mounted substrates and IC leads may cause a failure like solder peeling or soler wet, and electrical characteristics may change by thermal stress. Therefore, mounting should be done after sufficient confirmation for especially in case of ceramic substrates.

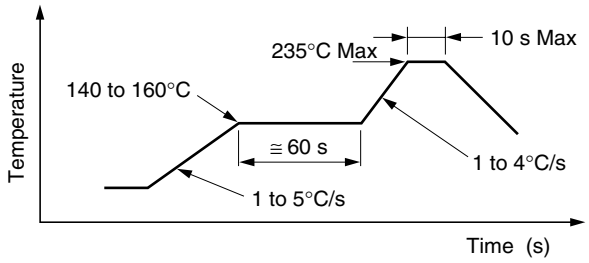
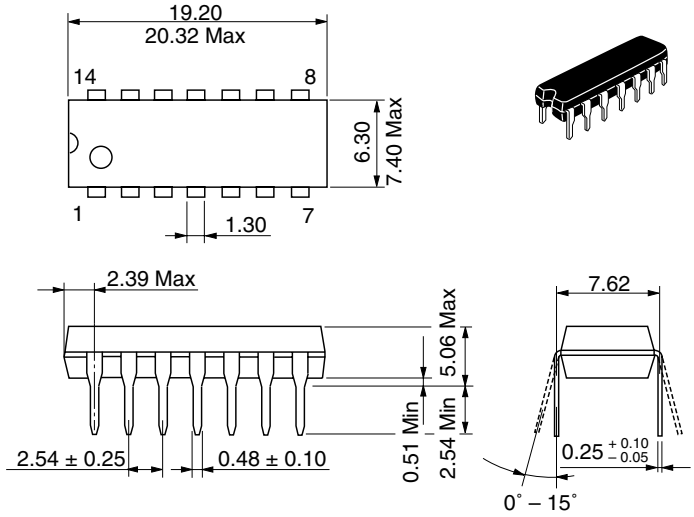



**Figure 1 An Example of Infrared Rays Reflow Conditions**

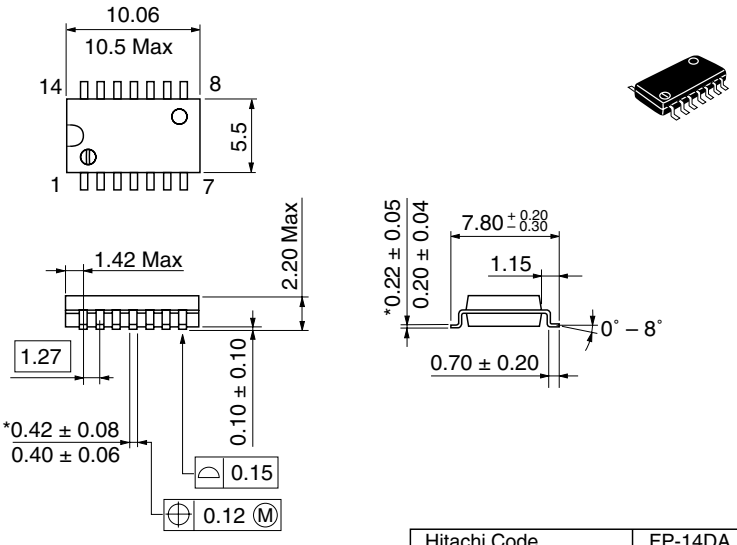
## Package Dimensions

Unit: mm




| | |
|---|---|
| Hitachi Code | DP-14 |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Mass (reference value) | 0.97 g |

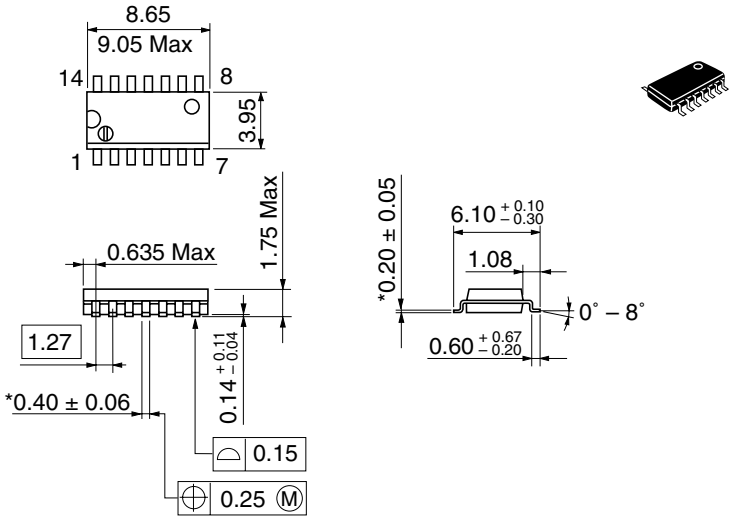
Unit: mm




| | |
|---|---|
| Hitachi Code | FP-14DA |
| JEDEC | — |
| EIAJ | Conforms |
| Mass (reference value) | 0.23 g |

*Dimension including the plating thickness
Base material dimension

Unit: mm




| | |
|---|---|
| Hitachi Code | FP-14DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Mass (reference value) | 0.13 g |

*Pd plating

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HITACHI

**Hitachi, Ltd.**
Semiconductor & Integrated Circuits
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : http://semiconductor.hitachi.com/
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**For further information write to:**

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : http://www.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
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URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
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