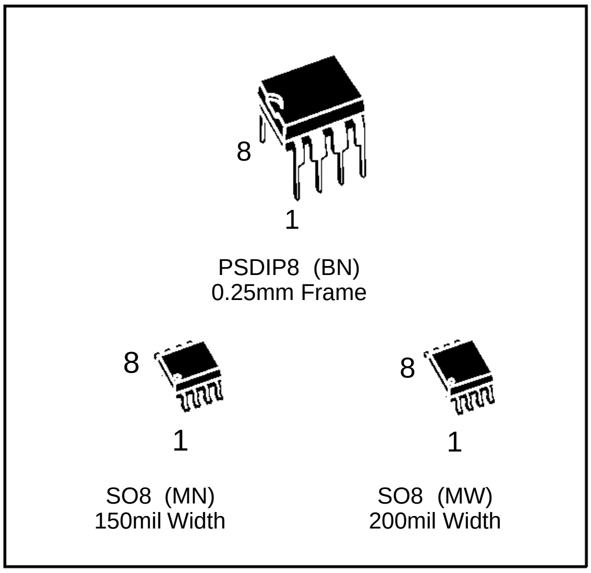
64K/32K SERIAL I^{2}C BUS EEPROM

PRELIMINARY DATA

- COMPATIBLE with I^{2}C EXTENDED ADDRESSING
- TWO WIRE I^{2}C SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  – 4.5V to 5.5V for M24C64 and M24C32
  – 2.5V to 5.5V for M24C64-W and M24C32-W
  – 1.8V to 5.5V for M24C64-R and M24C32-R
- HARDWARE WRITE CONTROL
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD and LATCH-UP PERFORMANCES



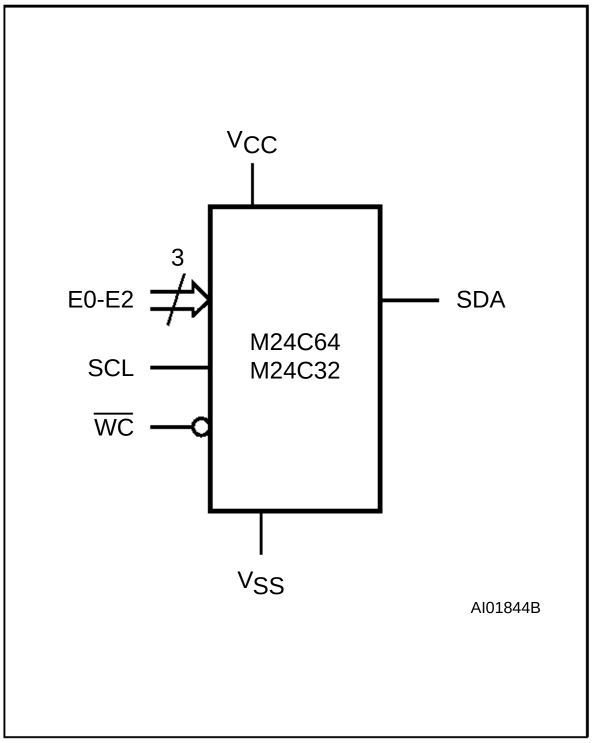
DESCRIPTION

The M24C64 and the M24C32 are 64K bit and a 32K bit electrically erasable programmable memories (EEPROM), organized as 8,192 x 8 and as 4,096 x 8 bits respectively. The ”-W” versions operate with a power supply value as low as 2.5V and the ”-R” versions operate down to 1.8V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is preliminary information a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 2A. DIP Pin Connections

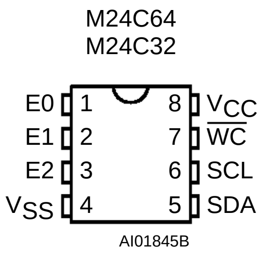


Figure 2B. SO Pin Connections

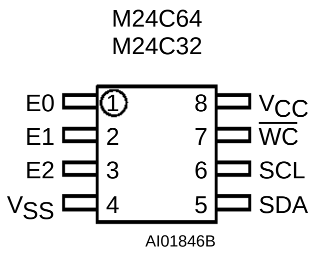


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (SO8) 40 sec (PSDIP8) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.6 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)	4000	V
	Electrostatic Discharge Voltage (Machine model) (3)	500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The Memory carries a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The Memory behaves as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), then 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$R\overline{W}$ bit	Data Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	1	START, Device Select, $R\overline{W}$ = '0', Address,
	'1'		reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	≥1	As CURRENT or RANDOM Mode
Byte Write	'0'	1	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	32	START, Device Select, $R\overline{W}$ = '0'

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition. In this way, up to 8 Memories may be connected to the same I^2C bus and selected individually.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

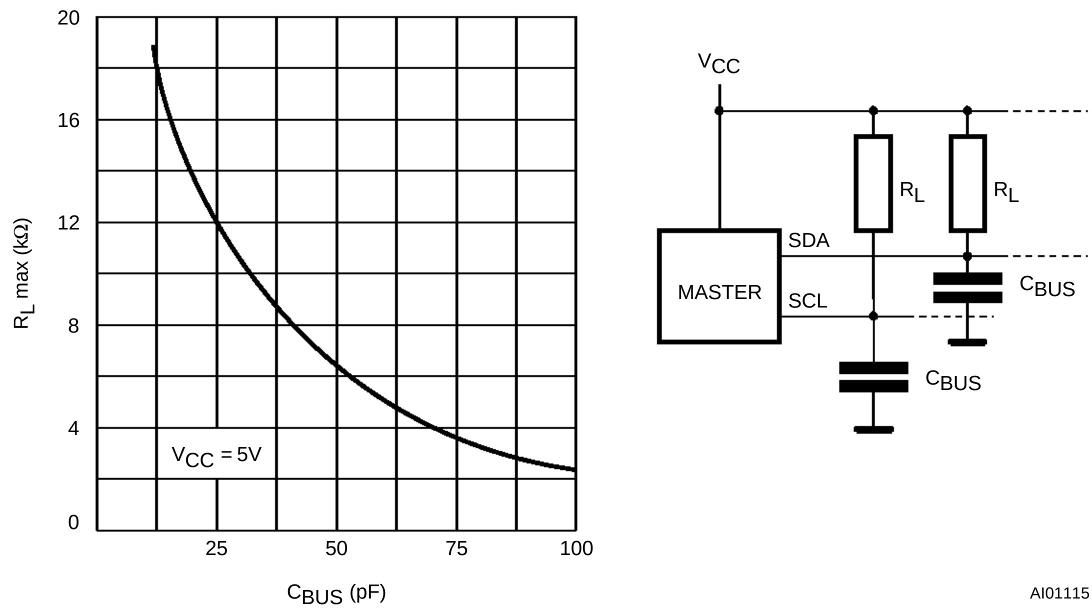
Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL compatible.

Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. When pin $\overline{WC}$ is unconnected, the $\overline{WC}$ input is internally read as V_{IL} (see Table 5).

When $\overline{WC}$ = '1', Device Select and Address bytes are acknowledged; Data bytes are not acknowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus, f_C = 400kHz



DEVICE OPERATION

I^2C Bus Background

The Memory supports the extended addressing I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The Memory is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the Memory continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the Memory and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the Memory samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave Memory , the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \le 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \ge 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (-W series)	V_{CC} = 2.5V, f_C = 400kHz (Rise/Fall time < 30ns)		1	mA
	Supply Current (-R series)	V_{CC} = 1.8V, f_C = 400kHz (Rise/Fall time < 30ns)		0.8	mA
I_{CC1}	Supply Current, Standby	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		10	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz, Note 1		100	µA
I_{CC2}	Supply Current, Standby (-W series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		2	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 400kHz, Note 1		50	µA
I_{CC3}	Supply Current, Standby (-R series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V		1	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V, f_C = 400kHz, Note 1		50	µA
V_{IL}	Input Low Voltage (SCL, SDA, E2, E1, E0)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA, E2, E1, E0)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (-W series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (-R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.2	V

Note: 1. Characterized only but not tested in production.

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

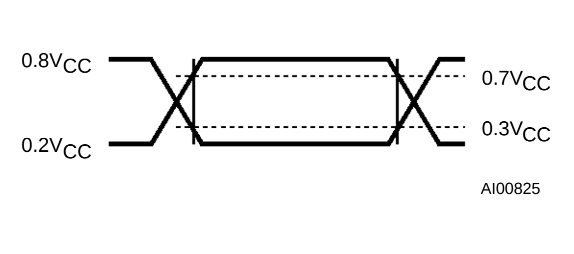
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV} (3)	t_{AA}	Clock Low to Next Data Out Valid	200	1000	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.
3. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. Bits b15 to b0 form the address of any byte of the memory. Bits b15 to b13 are don't care on the M24C64 series. Bits b15 to b12 are don't care on the M24C32 series.

Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

b15 to b13 are don't care on M24C64 series.
b15 to b12 are don't care on M24C32 series..

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Figure 5. AC Waveforms

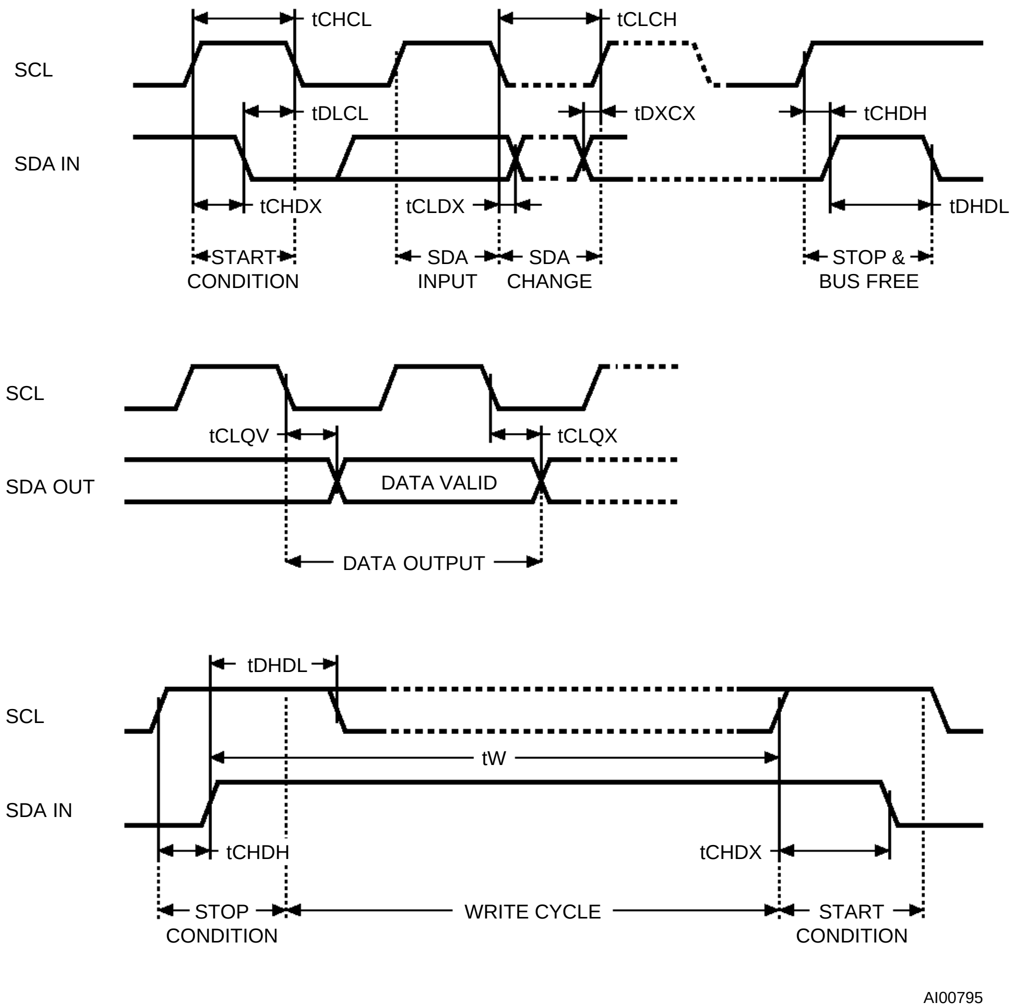
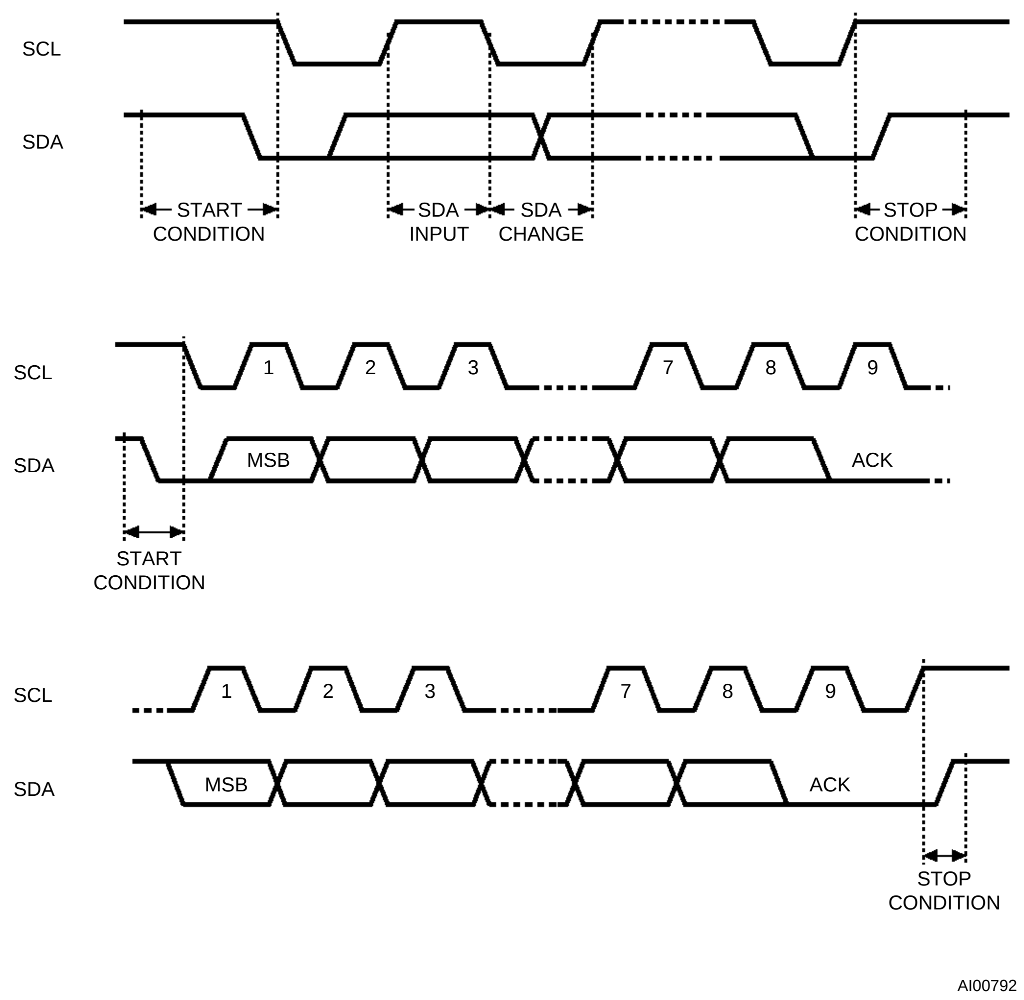


Figure 6. I²C Bus Protocol



Write Operations

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The Memory acknowledges this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the Memory location. Writing in the Memory may be inhibited if input pin $\overline{WC}$ is taken high.

Any write command with $\overline{WC}$ = '1' (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes, as shown in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the Memory. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 32 bytes to be written in a single write cycle, provided that they are all located in the same row of 32 bytes in the memory, that is the same Address bits (b12 to b5). The master sends one up to 32 bytes of data, which are each acknowledged by the Memory. After each byte is transfered, the internal byte address counter (5 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the Memory will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the Memory disables itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

– Initial condition: a Write is in progress (see Figure 7).
– Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
– Step 2: if the Memory is internally writing, no ACK will be returned. The Master goes back to Step1. If the Memory has terminated the internal writing, it will issue an ACK.
  The Memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 7. Write Cycle Polling using ACK

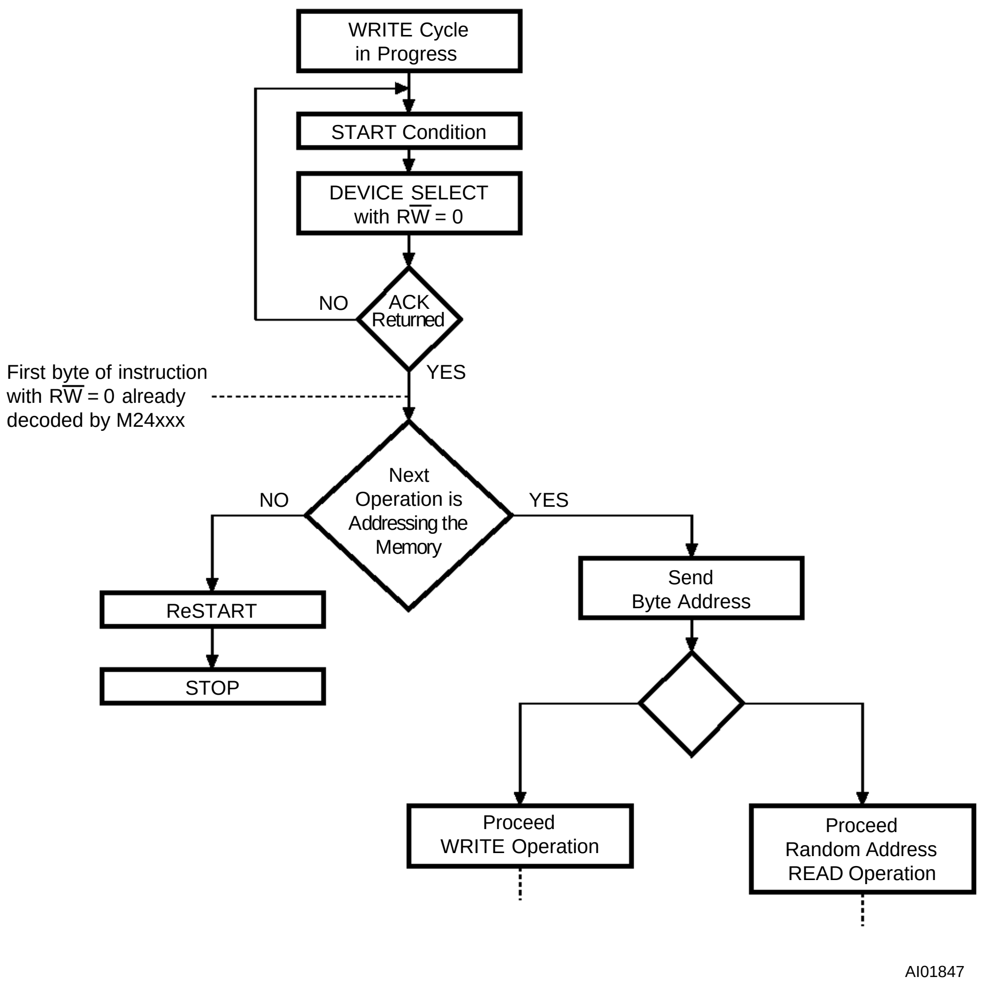
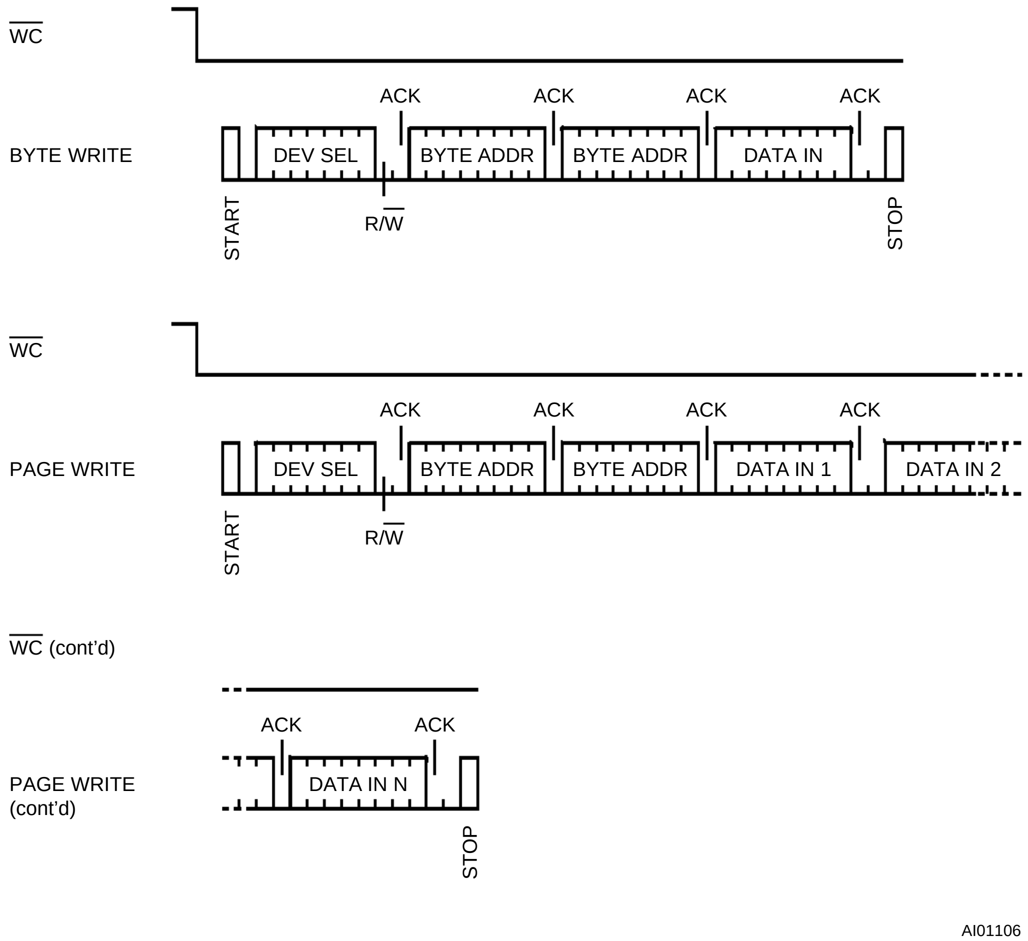


Figure 8. Write Modes Sequence with Write Control = 0



Read Operations

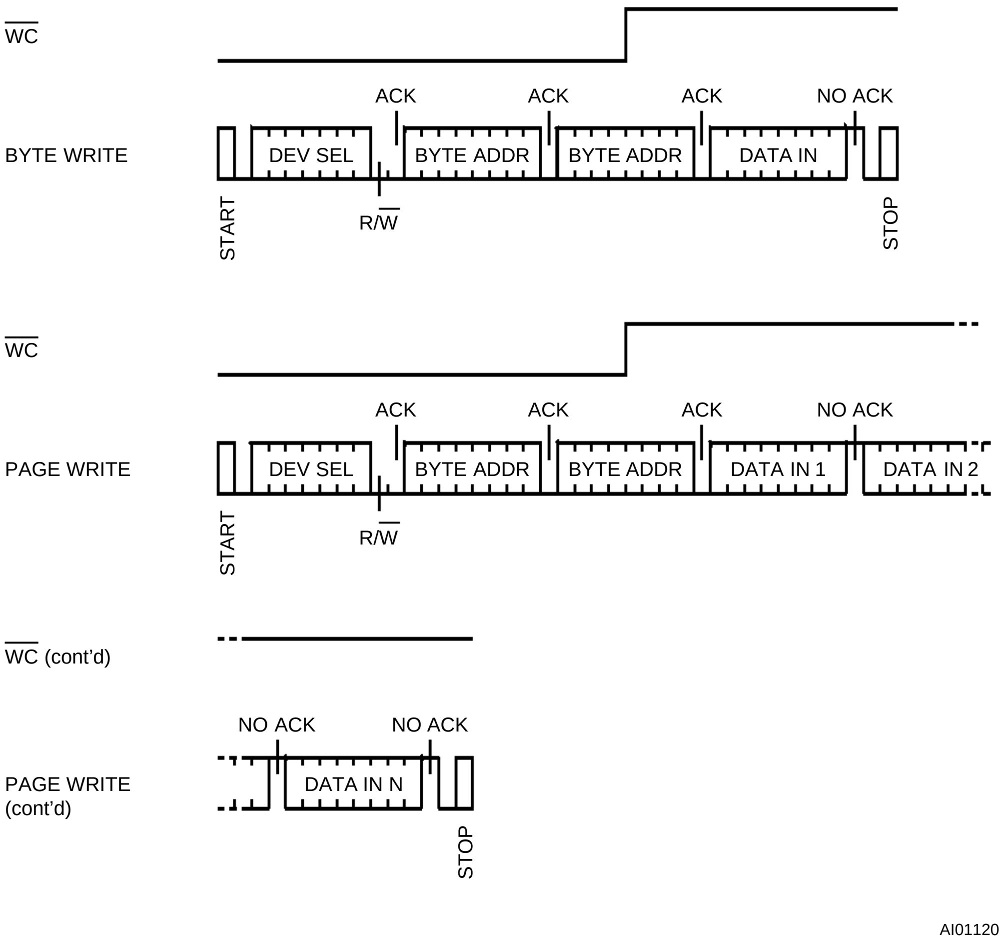
On delivery, the memory content is set at all ”1’s” (or FFh).

Current Address Read. The Memory has an internal address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the RW bit set to ’1’. The Memory acknowledges this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the RW bit set to ’1’. The Memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the Memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition.

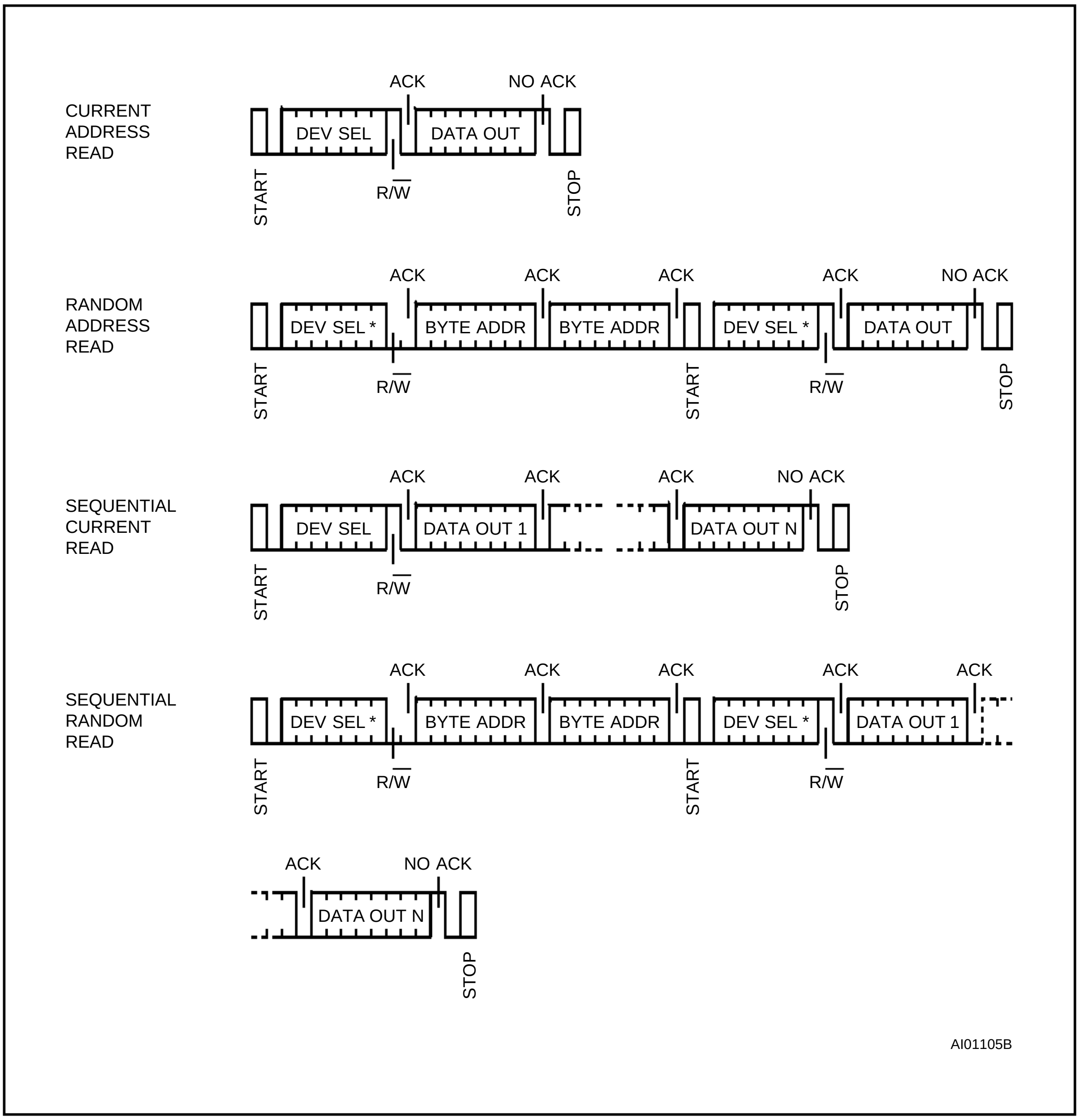
Figure 9. Write Modes Sequence with Write Control = 1



The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the Memory waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the Memory terminates the data transfer and switch to a standby state.

Figure 10. Read Mode Sequences



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME

Example: M24C64 – R MN 6 T

Density	Operating Voltage	Package	Temperature Range	Option
64 64K (8K x 8)	blank 4.5V to 5.5V	BN PSDIP8 0.25mm Frame	1 0 to 70 °C	T Tape & Reel Packing
32 32K (4K x 8)	W 2.5V to 5.5V	MN SO8 150mil Width	6 –40 to 85 °C	
	R 1.8V to 5.5V	MW SO8 200mil Width	3 (1) –40 to 125 °C	

Note: 1. Temperature Range on request only.

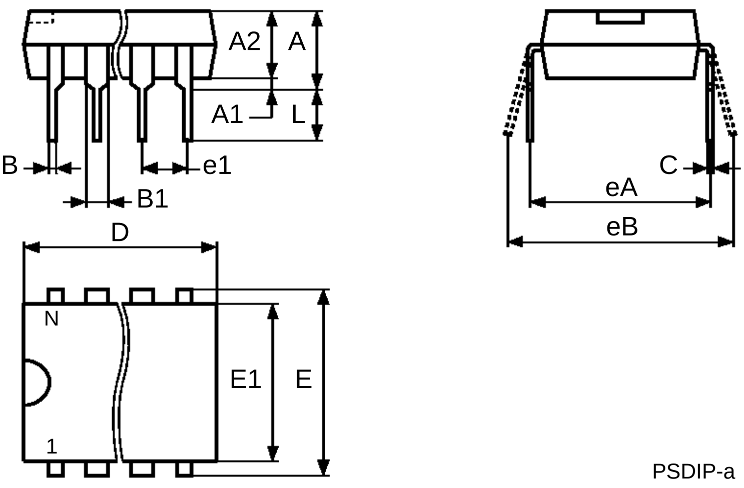
Devices are shipped from the factory with the memory content set at all ”1’s” (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8

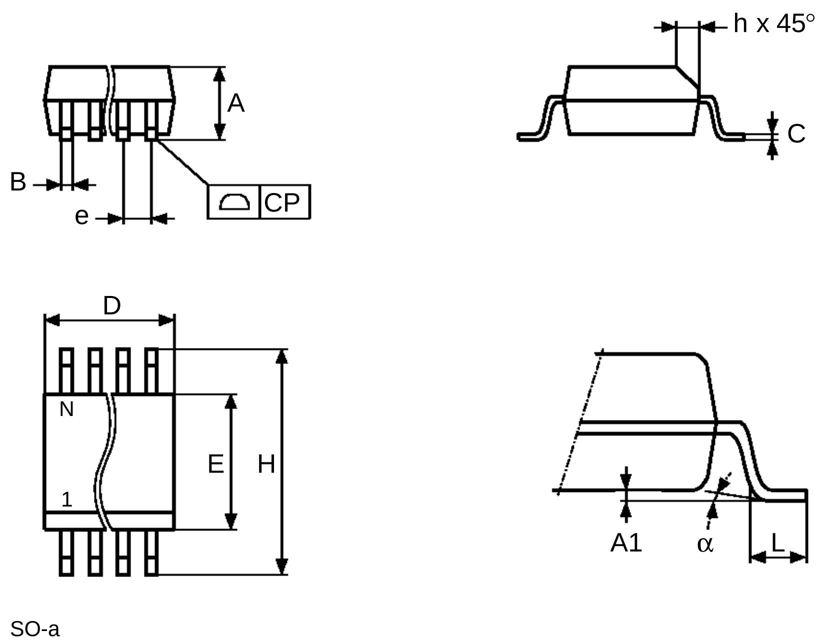


Drawing is not o scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8a



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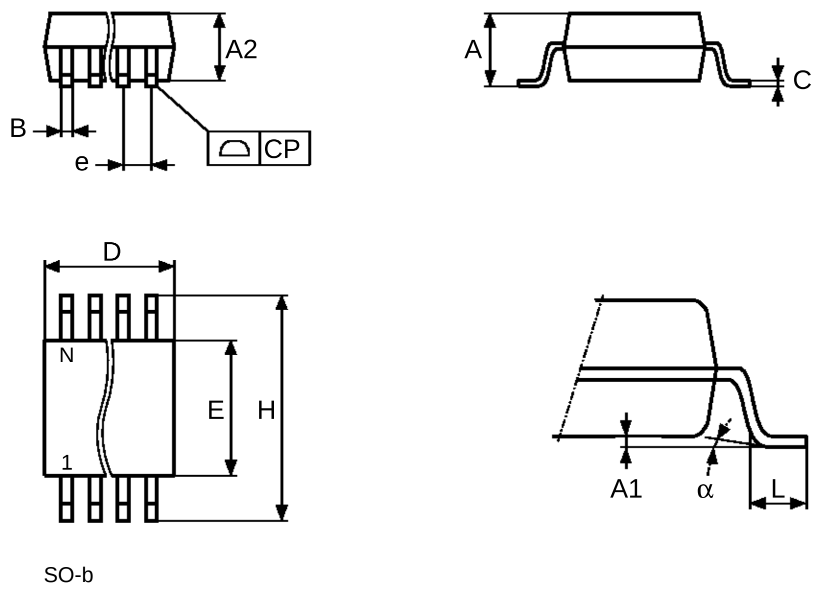
SO8 - 8 lead Plastic Small Outline, 200 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N	8			8		
CP			0.10			0.004

SO8b



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