Ordering number: EN 1571B

Monolithic Digital IC

SANYO No. 1571B

LB1649

Dual Bidirectional Motor Driver

The LB1649 is a dual bidirectional motor driver. Since each channel has a 2-input logic circuit and performs bidirectional driving and braking functions, it is capable of direct driving 2pcs. of motor of various types rated at 6 to 24V. The output voltage can be varied by using external zener diodes.
It is especially suited for dual motor drive (reel motor, loading motor, cassette motor in VTR) and for stepping motor drive.

Features

- With power transistors for motor drive contained, capable of withstanding dash current of 1A max.
- Performs braking function at the motor stop mode.
- Contains elements to absorb motor dash current.
- Input connectable direct to MOS LSI.
- Minimum number of external parts required.
- Wide operating voltage range.

Absolute Maximum Ratings at Ta=25°C

			unit
Maximum Supply Voltage	V_{CC}max	25	V
Input Voltage	V_{IN}	25	V
Output Current	I_O	±1	A
Allowable Power Dissipation	Pdmax	1.9	W
Operating Temperature	Topr	-25 to +75	°C
Storage Temperature	Tstg	-55 to +125	°C

Allowable Operating Conditions at Ta=25°C

			unit
Supply Voltage	V_{CC}	7 to 25	V

Electrical Characteristics at Ta=25°C, V_{CC}=12V, per channel

			min	typ	max	unit
Current Dissipation	I_{CC}	Braking mode, R_L=∞ per channel		7.0	10.0	mA
Output Leakage Current	I_{OL}	Braking mode, R_L=∞ per channel		40	120	μA
Input Threshold Voltage	V_{th}	R_L=∞	0.9	1.05	1.20	V
Output Voltage	V_O	R_L=60ohms, V_Z=7.4V	6.5	7.2	7.5	V

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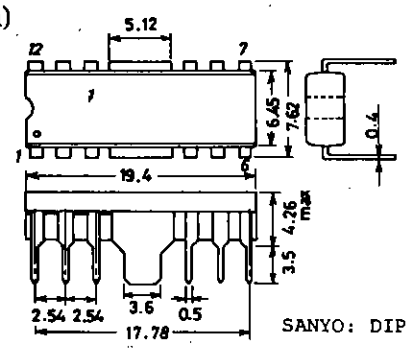
Package Dimensions 3022A
(unit: mm)



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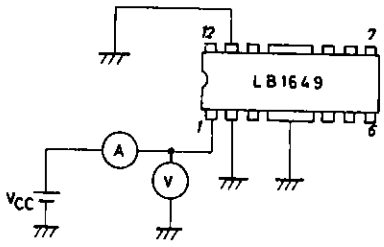
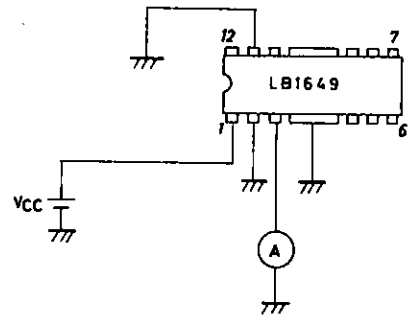
			min	typ	max	unit
Output Tr Saturation Voltage (Upper)	V_{sat1}	I_{OUT}=300mA		1.9	2.3	V
		I_{OUT}=500mA		2.0	2.4	V
Output Tr Saturation Voltage (Lower)	V_{sat2}	I_{OUT}=300mA		0.3	0.55	V
		I_{OUT}=500mA		0.5	0.7	V

Test Circuits (per channel)

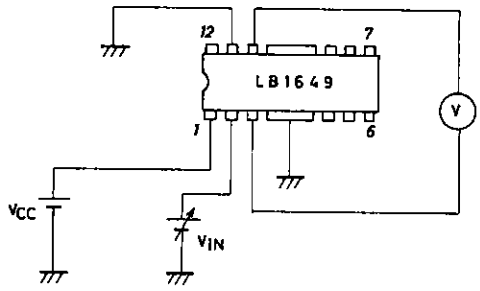
(1) I_{CC}



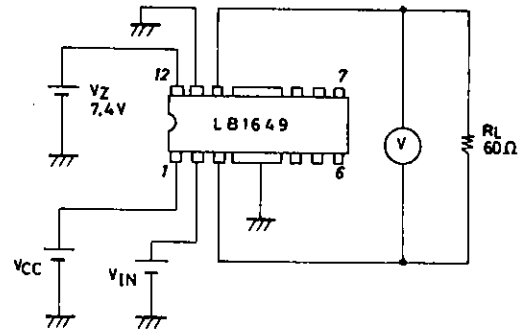
(2) I_{OL}



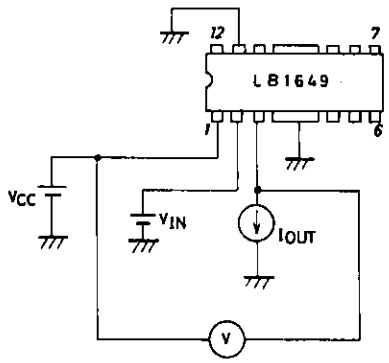
(3) V_{th}



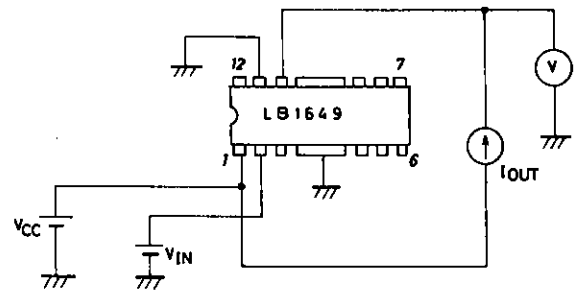
(4) V_O



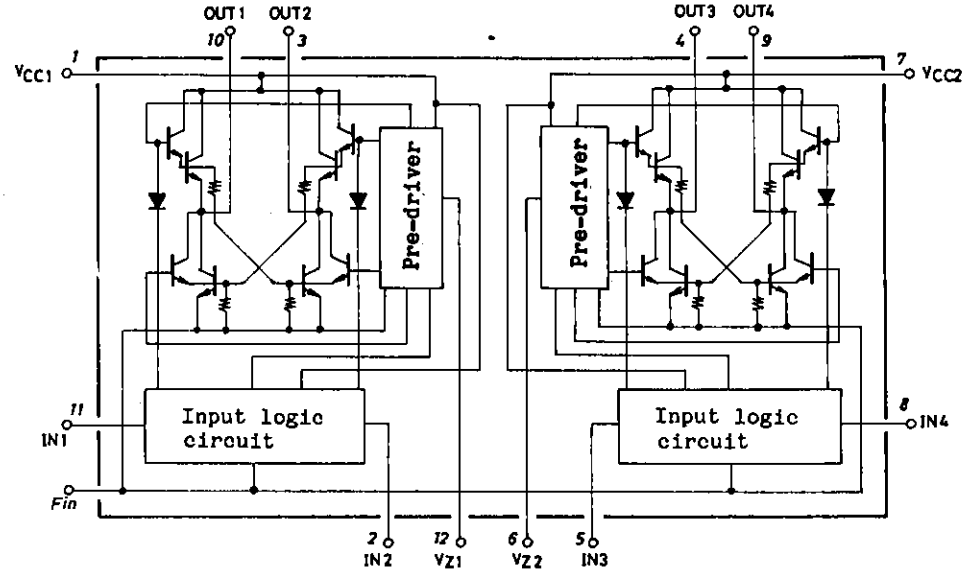
(5) V_{sat1}



(6) V_{sat2}



Equivalent Circuit Block Diagram



Truth Table of Logic Circuit

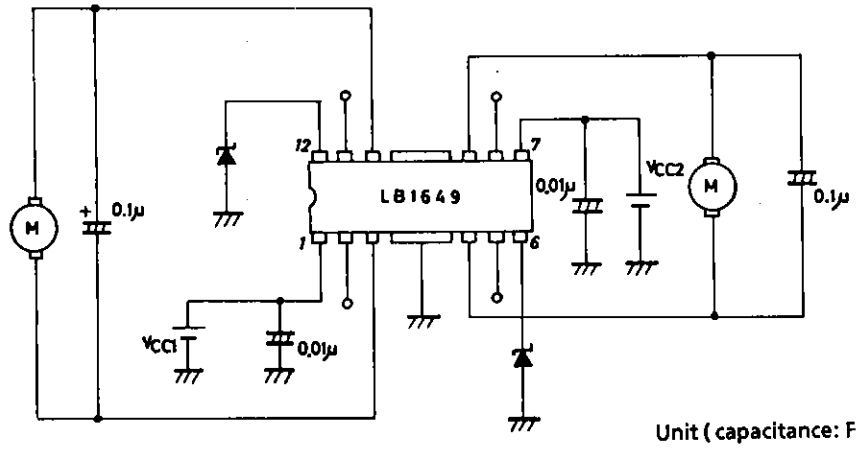
IN1	IN2	OUT1	OUT2	IN3	IN4	OUT3	OUT4
0	0	L	L	0	0	L	L
1	0	H	L	1	0	H	L
0	1	L	H	0	1	L	H
1	1	L	L	1	1	L	L

Note) A capacitor of 0.01μF or greater must be connected across $V_{CC}1,2$ and GND.

INPUT			OUT PUT				MODE	
IN1	IN2,3	IN4	OUT1	OUT2	OUT3	OUT4	M1	M2
0	0	0	L	L	L	L	Brake	Brake
1	0	0	H	L	L	L	Forward/Reverse	Brake
0	1	1	L	H	L	L	Reverse/Forward	Brake
1	1	0	L	L	H	L	Brake	Forward/Reverse
0	0	1	L	L	L	H	Brake	Reverse/Forward
1	1	1	L	L	L	L	Brake	Brake

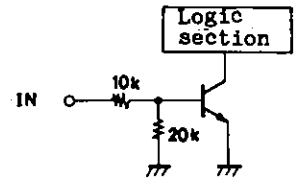
The remaining input states 1,0,1 and 0,1,0 are not inhibited.

Sample Application Circuit



Input Circuit

The input circuit is shown right.

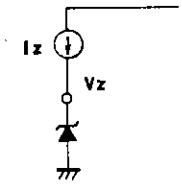


Unit (resistance: Ω)

V_Z pin

Zener voltage	V_Z pin Voltage value
≧5.6V	small
<5.6V	large*

*Susceptible to V_Z pin flow-out current change.



I_Z----V_Z flow-out current