

**SANYO**

No. 5466

**LC75394NE****Single-Chip Electronic Volume Control System****Overview**

The LC75394NE is an electronic volume control system providing control over volume, balance, 5-band equalizer, and input switching based on serial inputs.

**Functions**

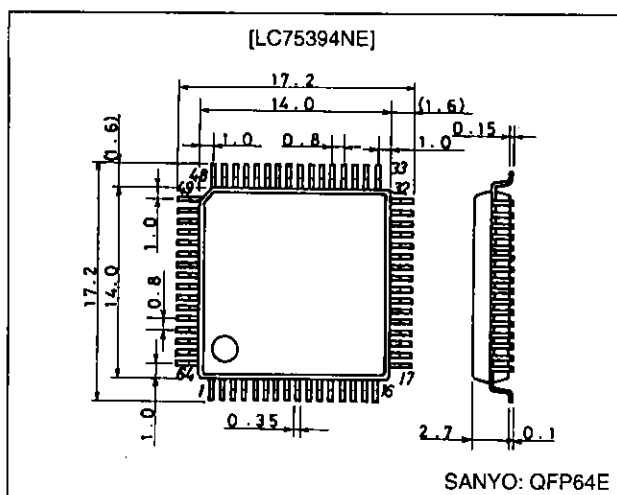
- **Volume control:**  
The chip provides 25 levels of volume attenuation: in 2-dB steps between 0 dB and -20 dB, 3-dB steps between -20 dB and -32 dB, 4-dB steps between -32 dB and -52 dB, 4.5-dB steps between -52 dB and -70 dB, and  $-\infty$ . Independent control over left and right channels provides balance control.
- **Equalizer:**  
The chip provides control in 2-dB steps over the range between +10 dB and -10 dB. Four of the five bands have peaking equalization; the remaining one, shelving equalization.
- **Selector:**  
The left and right channels each offer a choice of four inputs. An external constant determines the amplification for the input signal.

**Features**

- Built-in buffer amplifiers reduce the number of external parts necessary.
- Silicon gate CMOS reduces switching noise.
- Serial data input  
—Supports CCB\* format communication with the system controller.
- A built-in reference voltage circuit divides the supply voltage ( $V_{DD}$ ) in half.

**Package Dimensions**

unit: mm

**3159-QFP64E**

\*

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

**Specifications****Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$** 

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	$V_{DD}$	12	V
Maximum input voltage	$V_{IN\text{ max}}$	CL, DI, CE, L1 to L4, R1 to R4, LTIN, RTIN, LVRIN, RVRIN	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 85^\circ\text{C}$	310	mW
Operating temperature	$T_{opr}$		-30 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$

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## LC75394NE

### Allowable Operating Ranges at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}$	$V_{DD}$	6.0		11.0	V
Input high level voltage	$V_{IH}$	CL, DI, CE	4.0		$V_{DD}$	V
Input low level voltage	$V_{IL}$	CL, DI, CE	$V_{SS}$		1.0	V
Input voltage amplitude	$V_{IN}$	CL, DI, CE, L1 to L4, R1 to R4, LTIN, RTIN, LVRIN, RVRIN	$V_{SS}$		$V_{DD}$	V <sub>p-p</sub>
Input pulse width	$t_{pw}$	CL	1.0			$\mu\text{s}$
Setup time	$t_{SETUP}$	CL, DI, CE	1.0			$\mu\text{s}$
Hold time	$t_{HOLD}$	CL, DI, CE	1.0			$\mu\text{s}$
Operating frequency	$f_{opg}$	CL			500	kHz

### Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} = 10\text{ V}$ , $V_{SS} = 0\text{ V}$

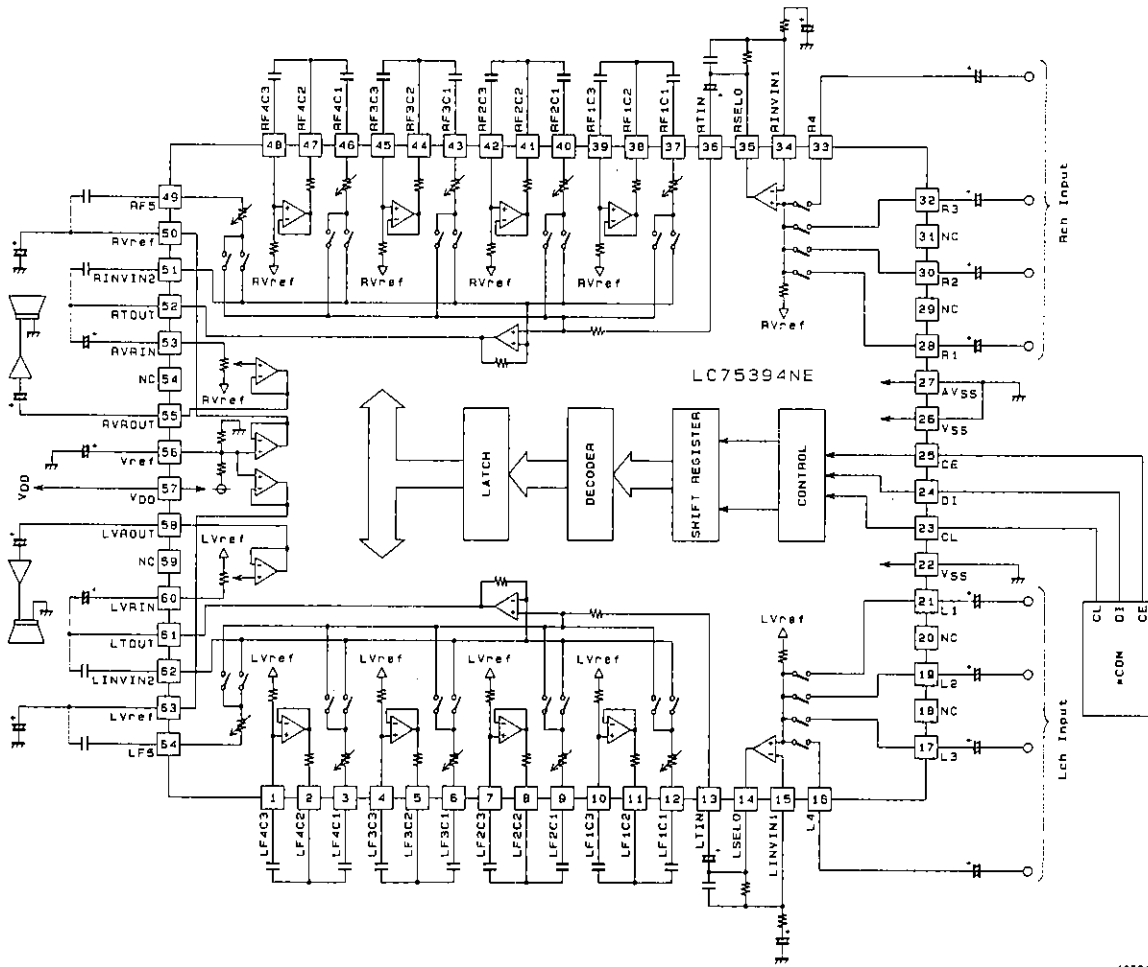
Parameter	Symbol	Conditions	min	typ	max	Unit
[Input block]						
Input resistance	$R_{in}$	L1 to L4, R1 to R4		1		M $\Omega$
Clipping level	$V_{cl}$	LSELO, RSELO: THD = 1.0%		2.65		V <sub>rms</sub>
Output load resistance	$R_L$	LSELO, RSELO	3			k $\Omega$
[Volume control block]						
Input resistance	$R_{in}$	LVRIN, RVRIN	60	100	140	k $\Omega$
[Equalizer control block]						
Control range	$G_{eq}$	Max, boost/cut	$\pm 8$	$\pm 10$	$\pm 12$	dB
Step resolution	$E_{step}$		1	2	3	dB
Internal feedback resistance	$R_{feed}$		17	28	39	k $\Omega$
[Overall characteristics]						
Total harmonic distortion	THD (1)	$V_{IN} = 1\text{ V}_{rms}$ , $f = 1\text{ kHz}$ , with all controls flat overall		0.0033		%
	THD (2)	$V_{IN} = 1\text{ V}_{rms}$ , $f = 20\text{ kHz}$ , with all controls flat overall		0.012		%
Crosstalk	CT	$V_{IN} = 1\text{ V}_{rms}$ , $f = 1\text{ kHz}$ , with all controls flat overall, $R_g = 1\text{ k}\Omega$		86		dB
Output at maximum attenuation	$V_O\text{ min}$	$V_{IN} = 1\text{ V}_{rms}$ , $f = 1\text{ kHz}$ , main volume $-\infty$		-90		dB
Output noise voltage	$V_N\text{ (1)}$	With all controls flat overall (IHF-A), $R_g = 1\text{ k}\Omega$		3.9		$\mu\text{V}$
	$V_N\text{ (2)}$	With all controls flat overall (DIN-AUDIO), $R_g = 1\text{ k}\Omega$		5.4		$\mu\text{V}$
Current drain	$I_{DD}$	$V_{DD} - V_{SS} = 11\text{ V}$		25	33	mA
Input high level current	$I_{IH}$	CL, DI, CE, $V_{IN} = 11\text{ V}$			10	$\mu\text{A}$
Input low level current	$I_{IL}$	CL, DI, CE, $V_{IN} = 0\text{ V}$	-10			$\mu\text{A}$

### Input Amplifier Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} - V_{SS} = 10\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Input offset voltage	$V_{IO}$		-10		+10	mV
Input offset current	$I_{IO}$	$V_{SS} \leq V_{IN} \leq V_{DD}$		$\pm 10$		nA
Open-loop voltage gain	$A_O$			80		dB
Width of 0 dB band	$f_T$			2.5		MHz
Allowable load resistance	$R_L$		3			k $\Omega$

# LC75394NE

## Equivalent Block Diagram and Sample Application Circuit

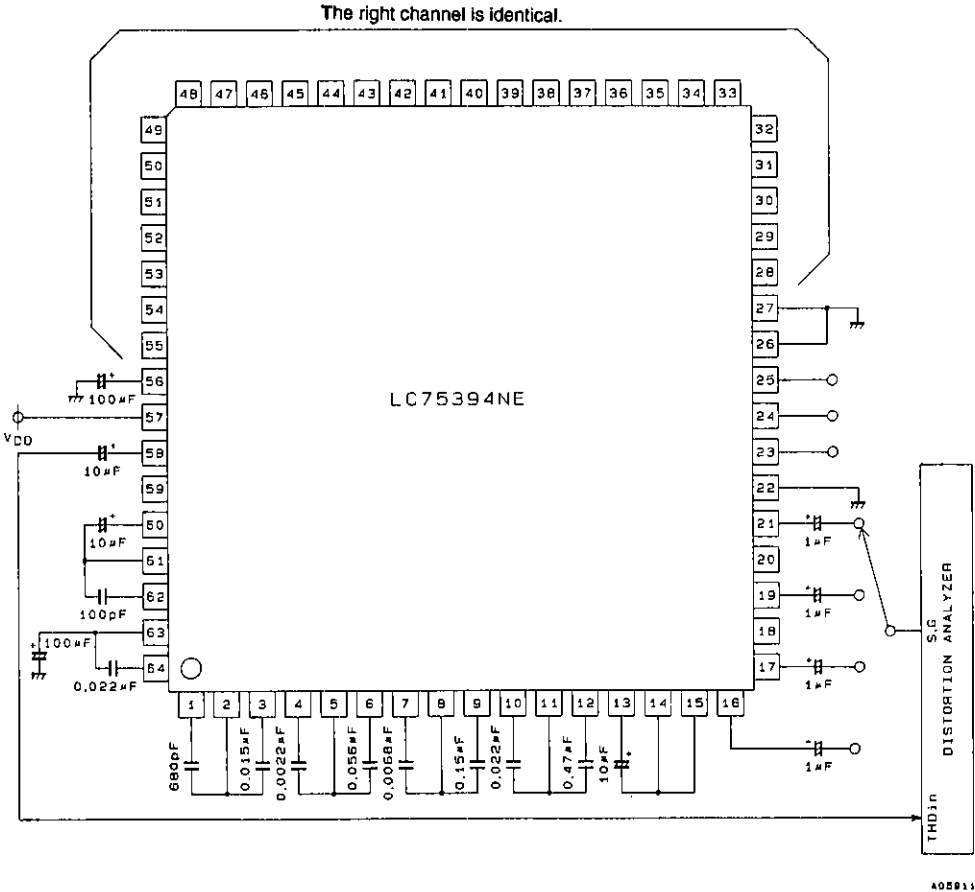


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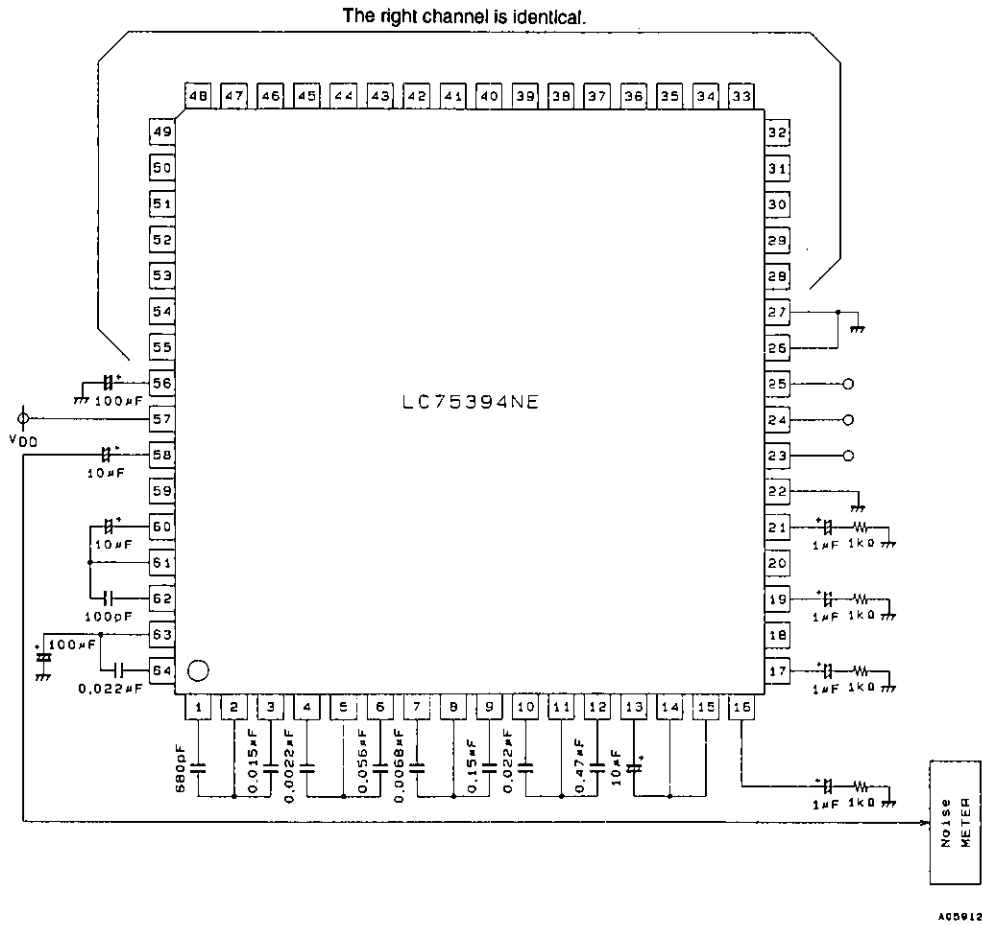
Test Circuits

1. Total Harmonic Distortion



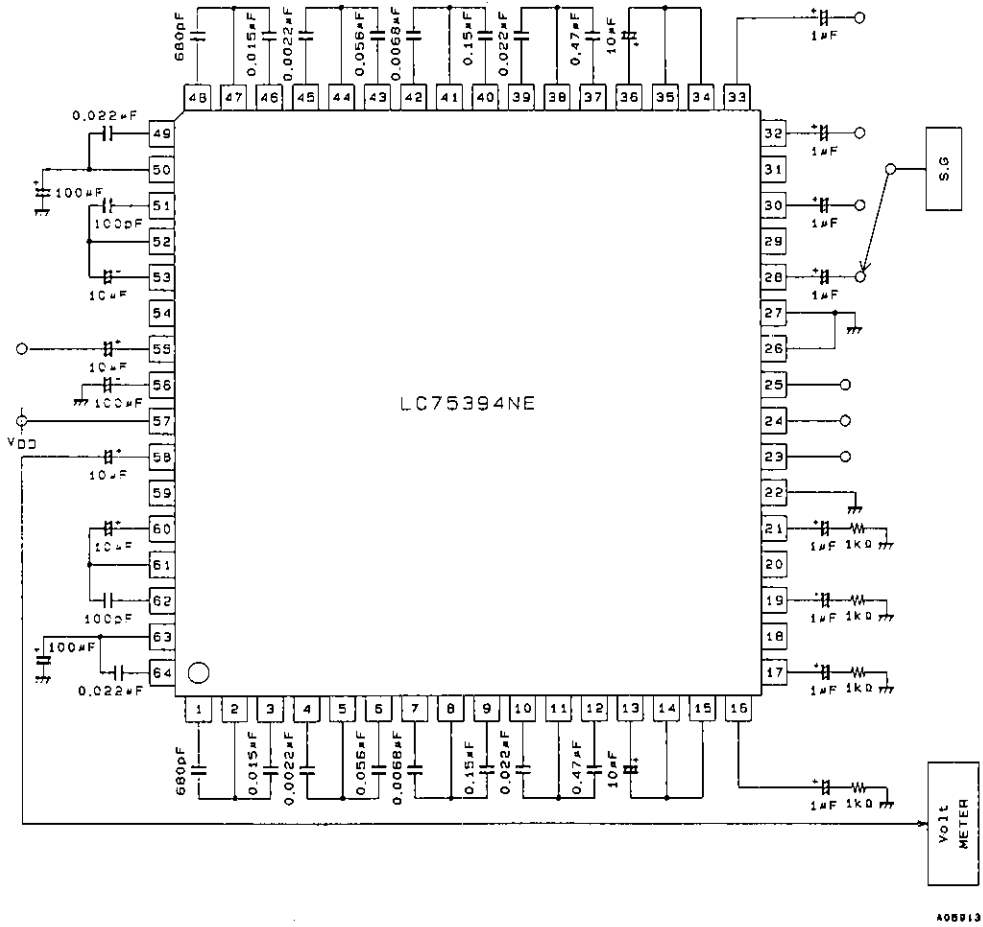
# LC75394NE

## 2. Output Noise Voltage



# LC75394NE

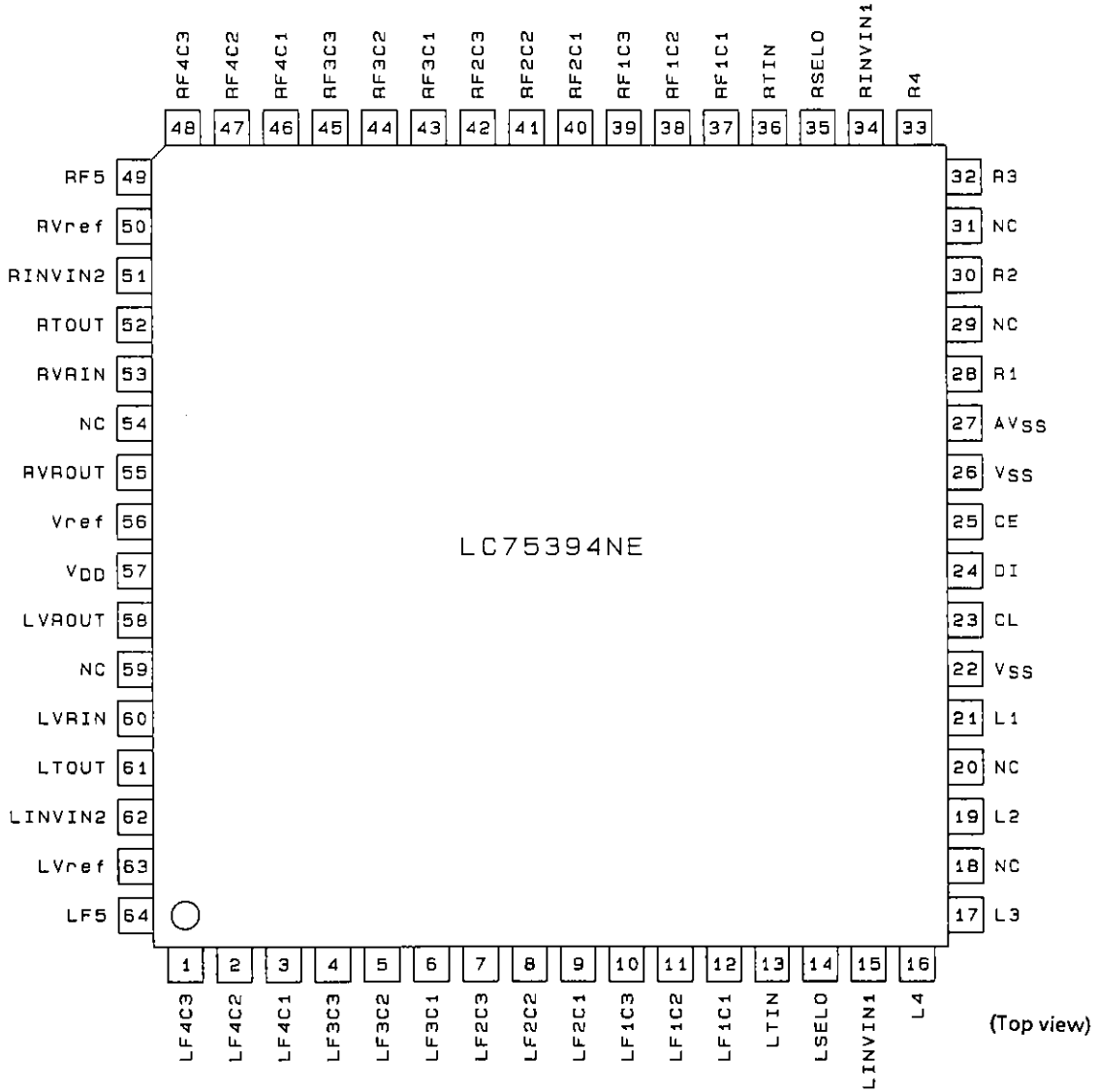
## 3. Crosstalk



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# LC75394NE

## Pin Assignment



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# LC75394NE

## Pin Functions

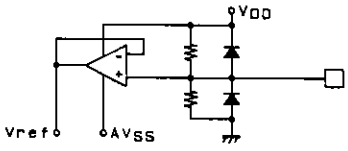
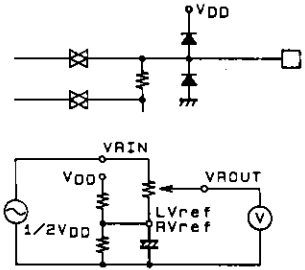
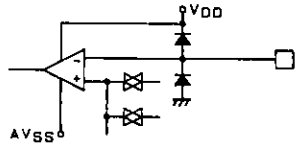
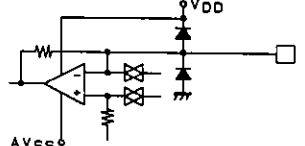
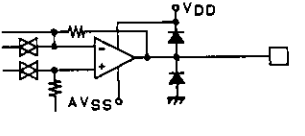
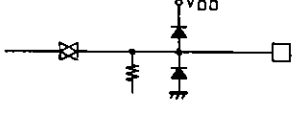
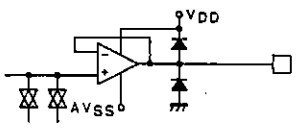
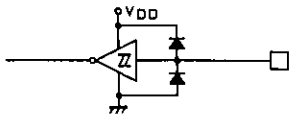
Pin No.	Symbol	Function	Note	
12 11 10	LF1C1 LF1C2 LF1C3	F1 band control block for left channel. Connect to external capacitors.	<p style="text-align: right;">A03750</p>	
37 38 39	RF1C1 RF1C2 RF1C3	F1 band control block for right channel. Connect to external capacitors.		
9 8 7	LF2C1 LF2C2 LF2C3	F2 band control block for left channel. Connect to external capacitors.		
40 41 42	RF2C1 RF2C2 RF2C3	F2 band control block for right channel. Connect to external capacitors.		
6 5 4	LF3C1 LF3C2 LF3C3	F3 band control block for left channel. Connect to external capacitors.		
43 44 45	RF3C1 RF3C2 RF3C3	F3 band control block for right channel. Connect to external capacitors.		
3 2 1	LF4C1 LF4C2 LF4C3	F4 band control block for left channel. Connect to external capacitors.		
46 47 48	RF4C1 RF4C2 RF4C3	F4 band control block for right channel. Connect to external capacitors.		
13 36	LTIN RTIN	Tone control inputs. Must be driven with low-impedance circuits.		<p style="text-align: right;">A03751</p>
14 35	LSELO RSELO	Input selector outputs		<p style="text-align: right;">A03752</p>
64 49	LF5 RF5	F5 band control block. Connect to external capacitors.	<p style="text-align: right;">A03753</p>	
21 19 17 16 28 30 32 33	L1 L2 L3 L4 R1 R2 R3 R4	Signal inputs	<p style="text-align: right;">A03754</p>	
57	V <sub>DD</sub>	Power supply connection		
22, 26	V <sub>SS</sub>	Grounds for internal logic		
27	AV <sub>SS</sub>	Ground for internal operational amplifier		

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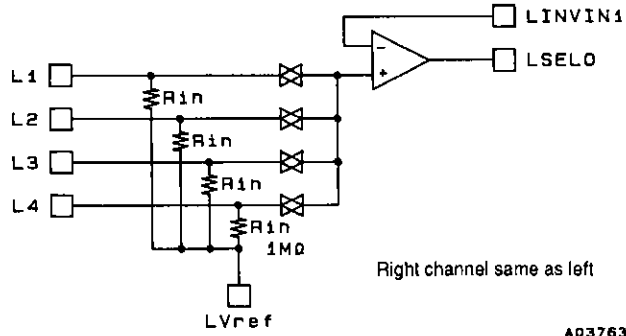


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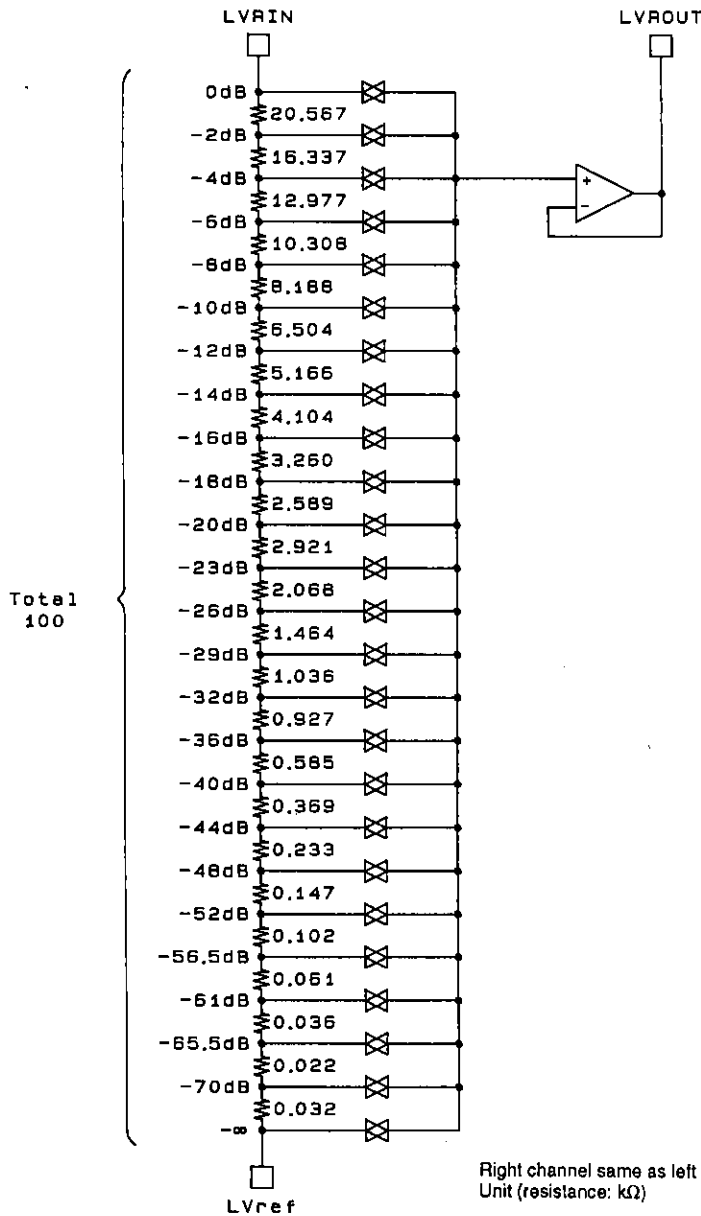
Pin No.	Symbol	Function	Note
56	Vref	$V_{DD}/2$ voltage generator block. Connect capacitors between Vref and $V_{SS}$ to minimize the effects of power supply ripple.	 <p style="text-align: right;">A03755</p>
63 50	LVref RVref	Pins common to volume control, tone control, and input selection blocks. Select the capacitors between these pins and $V_{SS}$ carefully as they contribute residual resistance when the volume is turned down. The voltage must never exceed $V_{DD}$ .	 <p style="text-align: right;">A03756</p>
15 34	LINVIN1 RINVIN1	Operational amplifier inverted input for specifying input gain.	 <p style="text-align: right;">A03757</p>
62 51	LINVIN2 RINVIN2	Operational amplifier inverted input for specifying graphic equalization. Connecting a capacitor across INVIN2 and TOUT permits the removal of unwanted bands and reduces the risk of oscillation.	 <p style="text-align: right;">A03758</p>
61 52	LTOUT RTOUT	Tone control output	 <p style="text-align: right;">A03759</p>
60 53	LVRIN RVRIN	Volume control input. Must be driven with low-impedance circuits.	 <p style="text-align: right;">A03760</p>
58 55	LVROUT RVROUT	Volume control output	 <p style="text-align: right;">A03761</p>
25	CE	Chip enable pin. The chip uses falling edge timing to write data to the internal latch and shift analog switches. The high level enables data transfer.	 <p style="text-align: right;">A03762</p>
24 23	DI CL	Serial data and clock input used for control	
18 20 29 31 54 59	NC NC NC NC NC NC	Leave unconnected	

Input Block Internal Equivalent Circuit Diagram



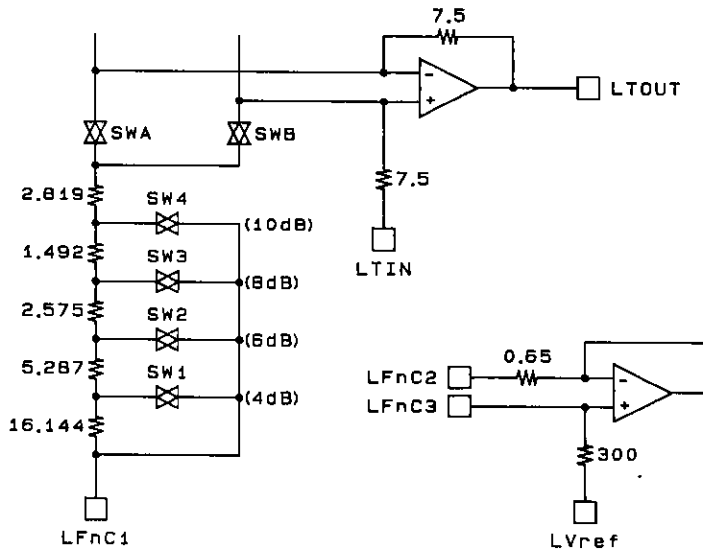
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Volume Control Block Internal Equivalent Diagram



A03764

Equalizer Control Block Internal Equivalent Circuit (Bands F1 to F4)



TOTAL=28.317

Right channel same as left  
Unit (resistance: kΩ)

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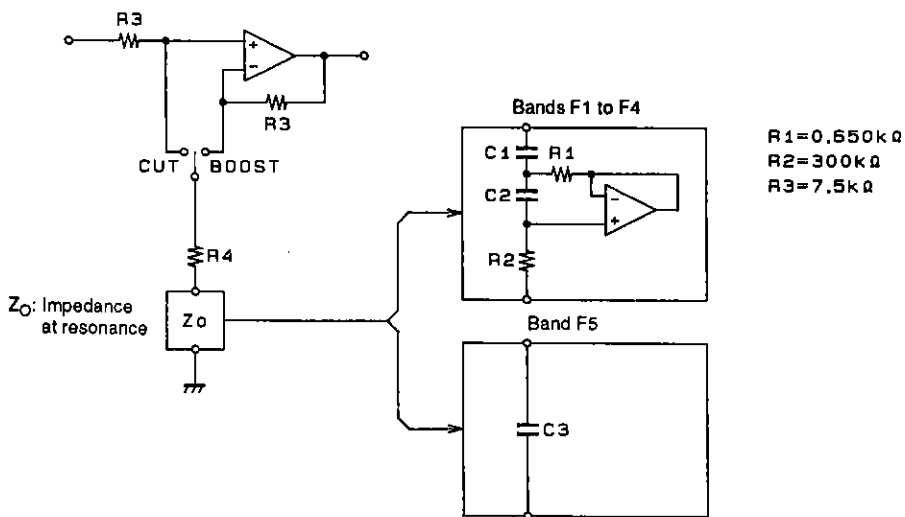
Calculating the Size of External Capacitors

The LC75394NE supports four bands with peaking characteristics and one band with shelving characteristics

1. Peaking Characteristics (bands F1 to F4)

The external capacitor functions as the structural element of a simulated inductor. The equivalent circuit and the calculations required to achieve the desired center frequency are shown below.

- Equivalent circuit for the simulated inductor



R1=0.650kΩ  
R2=300kΩ  
R3=7.5kΩ

A03766

• Calculation example

Specifications: Central frequency,  $F_O = 107 \text{ Hz}$

Q factor at maximum boost,  $Q_{+10 \text{ dB}} = 0.8$

— Calculate  $Q_O$ , the sharpness of the simulated inductance itself.

$$Q_O = (R1 + R4)/R1 \times Q_{+10 \text{ dB}} \\ \approx 4.270$$

Note: R4 is from the separately issued internal block diagram.

— Calculate C1

$$C1 = 1/2\pi F_O R1 Q_O \approx 0.536 \text{ } (\mu\text{F})$$

— Calculate C2

$$C2 = Q_O/2\pi F_O R2 \approx 0.021 \text{ } (\mu\text{F})$$

• Sample results

Central frequency $F_O$ (Hz)	C1 (F)	C2 (F)
107	0.536 $\mu$	0.021 $\mu$
340	0.169 $\mu$	6663 p
1070	0.054 $\mu$	2117 p
3400	0.017 $\mu$	666 p

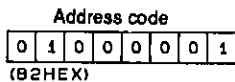
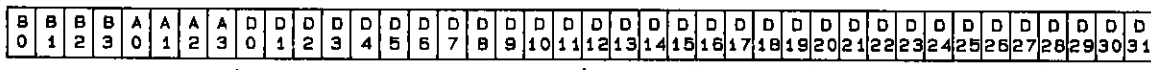
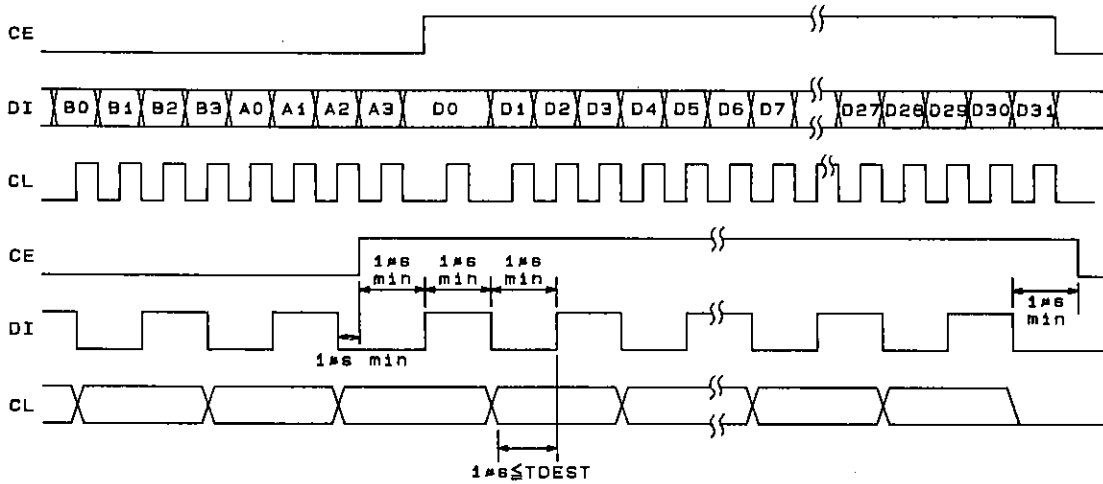
• Shelving characteristics (Band F5)

Achieving the desired control of 2-dB steps over the range between +10 dB to -10 dB requires choosing a capacitor, C3, with an impedance of 650  $\Omega$ .

# LC75394NE

## Control System Timing and Data Formats

The LC75394NE receives its control sequences via a serial interface comprised of pins CE, CL, and DI. Each sequence consists of 40 bits: an 8-bit address followed by 32 bits of data.



Volume control	Band F5 control	Band F4 control	Band F3 control	Band F2 control	Band F1 control	Input switching control
00000000 -∞	1010 +10dB	1010 +10dB	1010 +10dB	1010 +10dB	1010 +10dB	00 L1 (R1)
10000000 -70dB	0010 +8dB	0010 +8dB	0010 +8dB	0010 +8dB	0010 +8dB	10 L2 (R2)
01000000 -65.5dB	1100 +6dB	1100 +6dB	1100 +6dB	1100 +6dB	1100 +6dB	01 L3 (R3)
11000000 -61dB	0100 +4dB	0100 +4dB	0100 +4dB	0100 +4dB	0100 +4dB	11 L4 (R4)
00100000 -56.5dB	1000 +2dB	1000 +2dB	1000 +2dB	1000 +2dB	1000 +2dB	
10100000 -52dB	0000 0dB	0000 0dB	0000 0dB	0000 0dB	0000 0dB	
01100000 -48dB	1001 -2dB	1001 -2dB	1001 -2dB	1001 -2dB	1001 -2dB	
11100000 -44dB	0101 -4dB	0101 -4dB	0101 -4dB	0101 -4dB	0101 -4dB	
00010000 -40dB	1101 -6dB	1101 -6dB	1101 -6dB	1101 -6dB	1101 -6dB	
10010000 -36dB	0011 -8dB	0011 -8dB	0011 -8dB	0011 -8dB	0011 -8dB	
01010000 -32dB	1011 -10dB	1011 -10dB	1011 -10dB	1011 -10dB	1011 -10dB	
11010000 -29dB						
00110000 -26dB						
10110000 -23dB						
01110000 -20dB						
11110000 -18dB						
00001000 -16dB						
10001000 -14dB						
01001000 -12dB						
11001000 -10dB						
00101000 -8dB						
10101000 -6dB						
01101000 -4dB						
11101000 -2dB						
00011000 0dB						

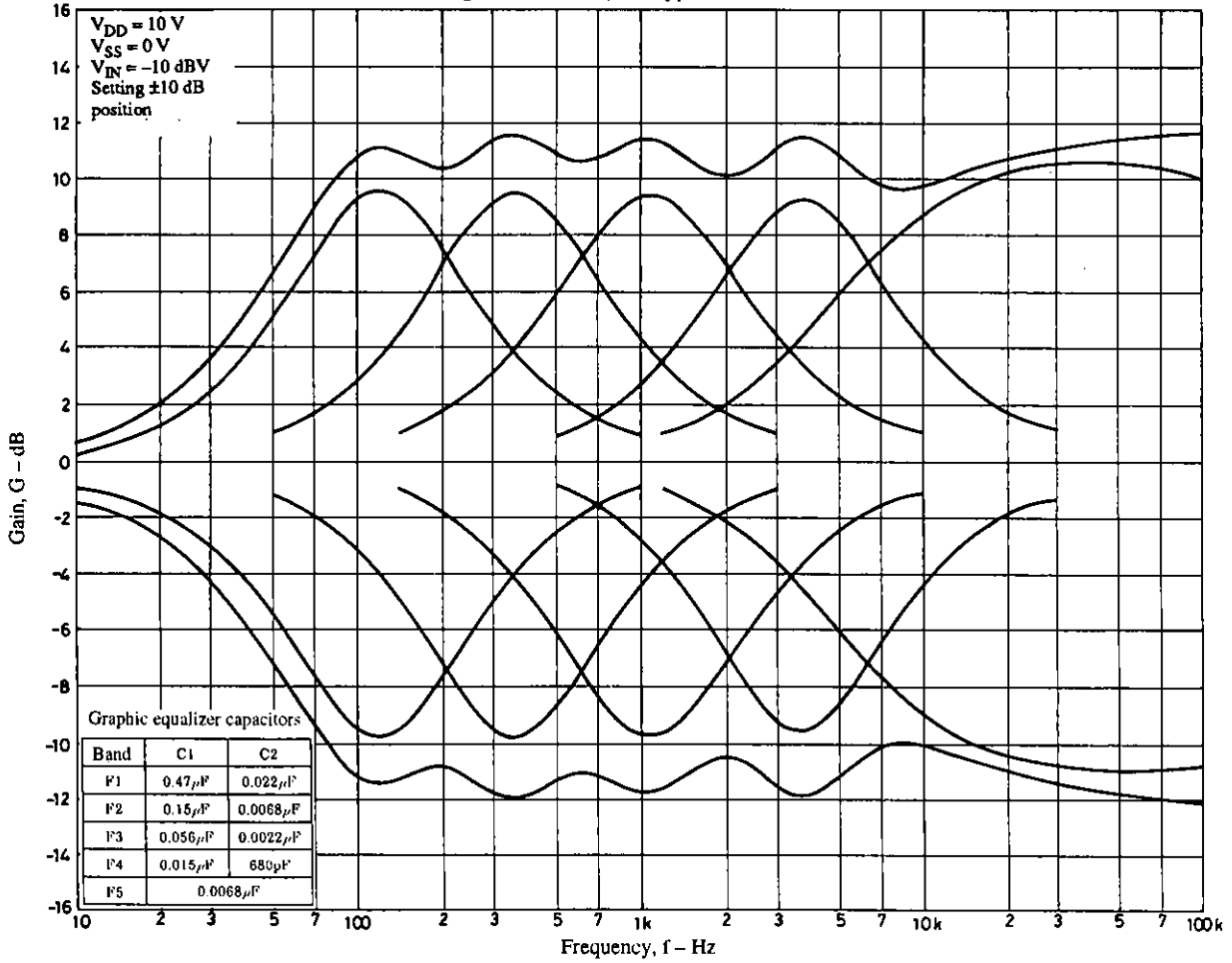
Channel selection	Control	Description
00	00	L1 (R1)
10	10	L2 (R2)
01	01	L3 (R3)
11	11	L4 (R4)

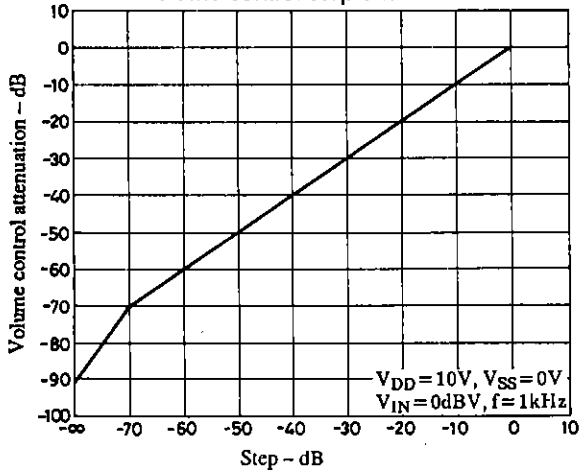
Channel selection	Control	Description
00	00	R ch
01	01	L ch
11	11	Both simultaneously

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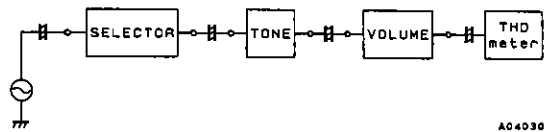
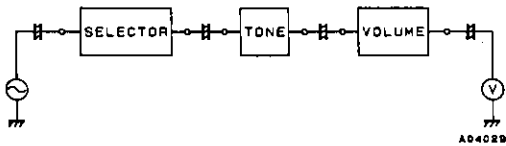
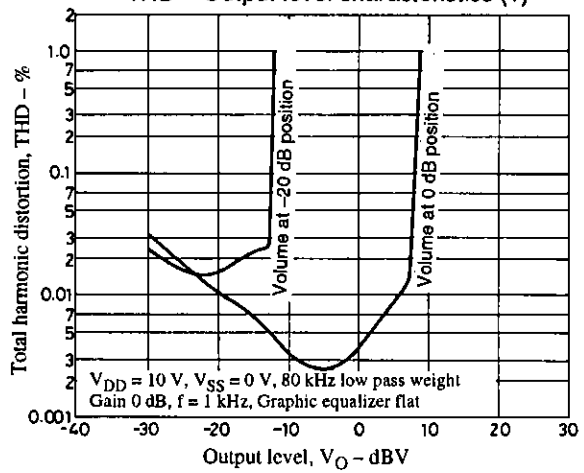
$f_0$  (central frequency) characteristic



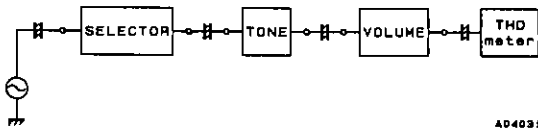
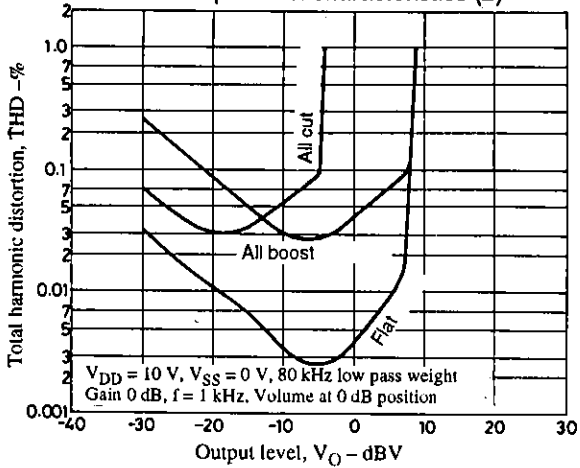
Volume control step characteristic



THD - Output level characteristics (1)

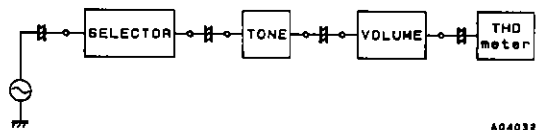
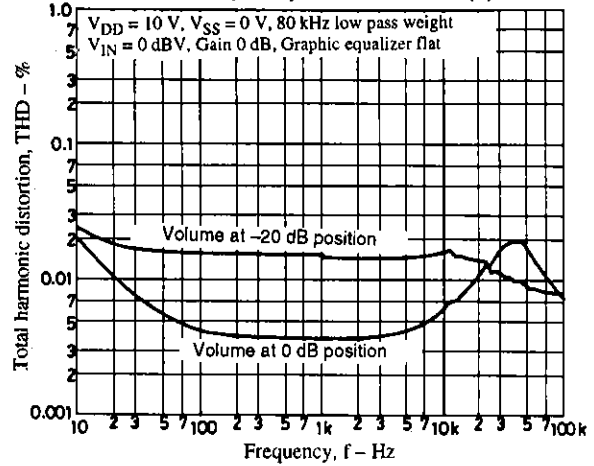


THD – Output level characteristics (2)



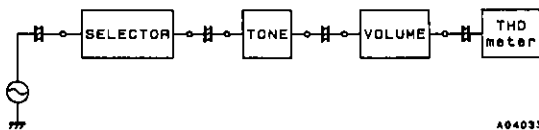
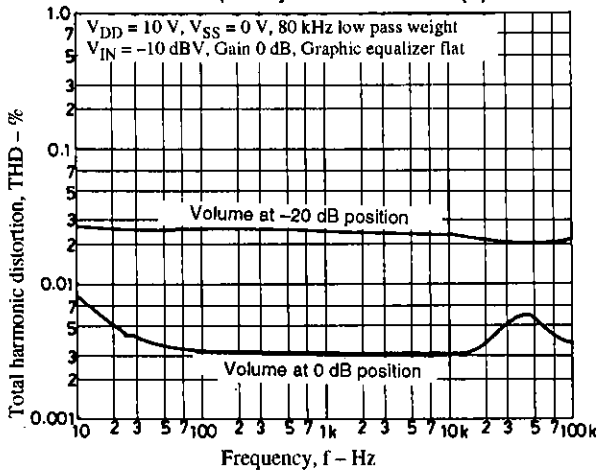
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THD – Frequency characteristics (1)



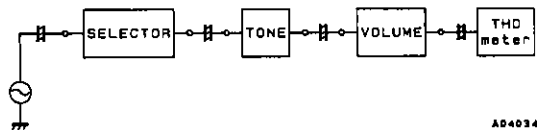
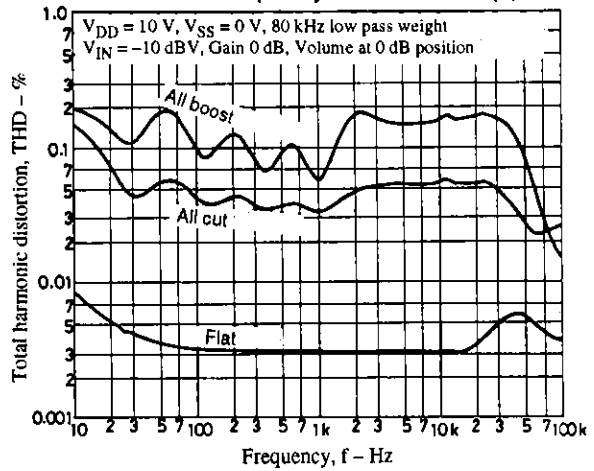
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THD – Frequency characteristics (2)

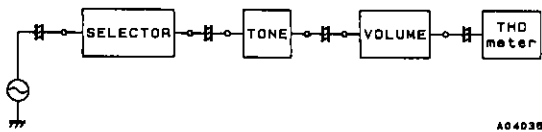
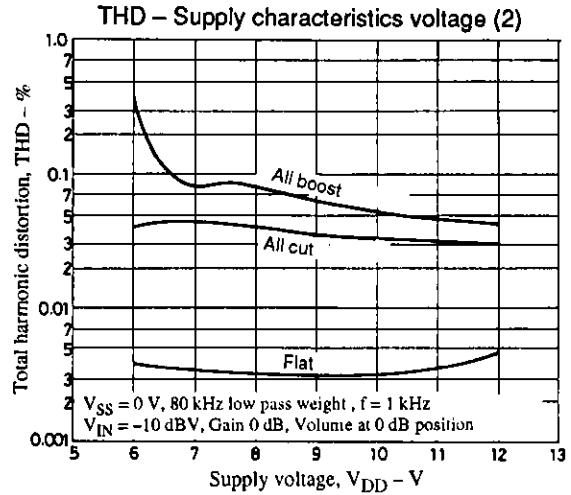
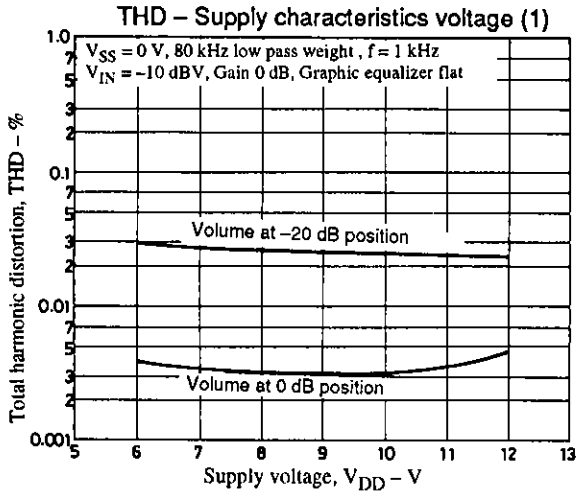


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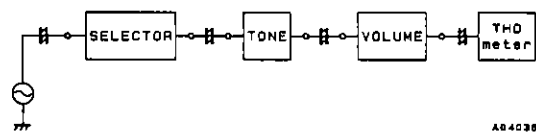
THD – Frequency characteristics (3)



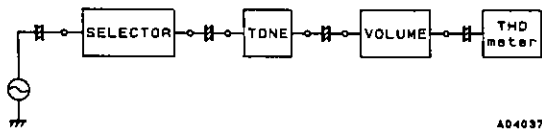
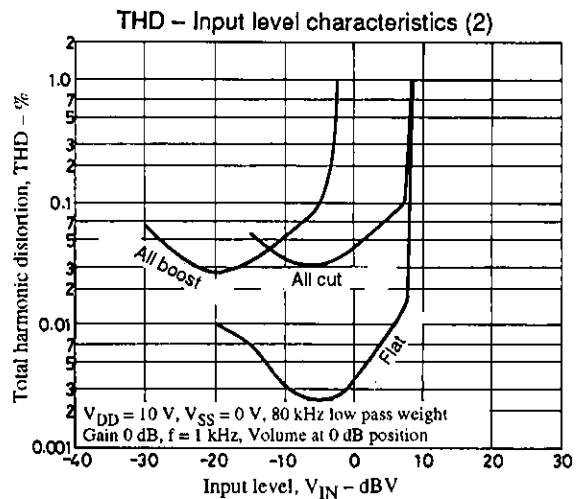
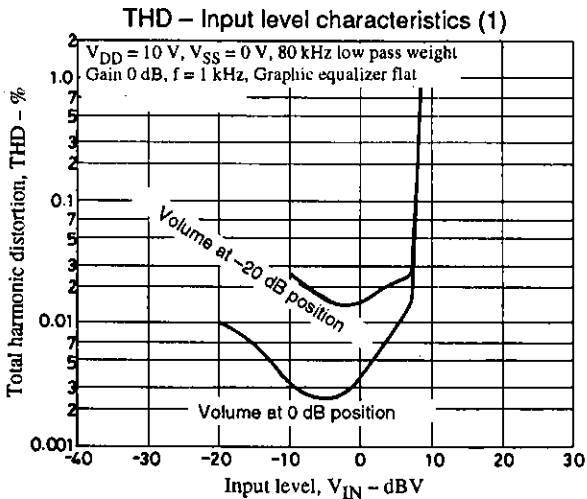
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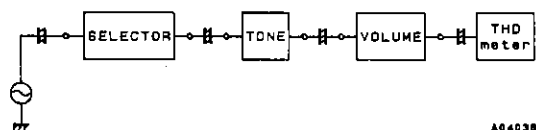
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A04037



A04038

**Usage Notes**

1. When the power is first applied, the internal analog switches are in indeterminate states. The chip therefore requires muting or other external measures until it has received the proper data.
2. Provide grounding patterns or shielding for the lines to the CL, DI, and CE pins so as to prevent their high-frequency data signals from interfering with the operation of nearby analog circuits.



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