Order this document by MC33199/D

MOTOROLA

MC33199

Advance Information

Automotive ISO 9141 Serial Link Driver

The MC33199D is a serial interface circuit used in diagnostic applications. It is the interface between the microcontroller and the special K and L Lines of the ISO diagnostic port. The MC33199D has been designed to meet the “Diagnosis System ISO 9141” specification.

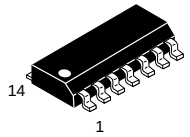
The device has a bi–directional bus K Line driver, fully protected against short circuits and over temperature. It also includes the L Line receiver, used during the wake up sequence in the ISO transmission.

The MC33199 has a unique feature which allows transmission baud rate up to 200 k baud.

- Electrically Compatible with Specification “Diagnosis System ISO 9141”
- Transmission Speed Up to 200 k Baud
- Internal Voltage Reference Generator for Line Comparator Thresholds
- TXD, RXD and LO Pins are 5.0 V CMOS Compatible
- High Current Capability of DIA Pin (K Line)
- Short Circuit Protection for the K Line Input
- Over Temperature Shutdown with Hysteresis
- Large Operating Range of Driver Supply Voltage
- Full Operating Temperature Range
- ESD Protected Pins

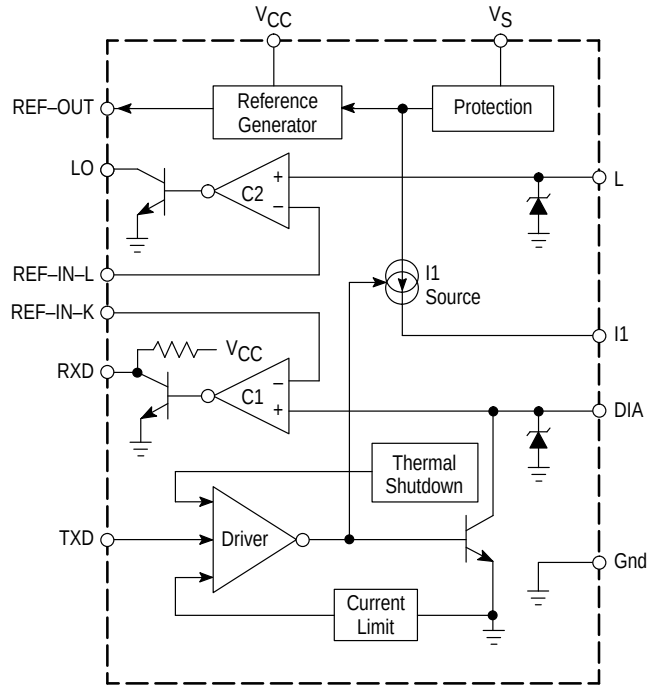
ISO 9141
SERIAL LINK DRIVER

SEMICONDUCTOR
TECHNICAL DATA



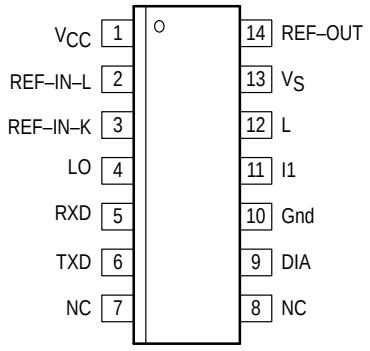
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

Simplified Application



This device contains 94 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33199D	T_A = – 40° to +125°C	SO–14

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
V_S Supply Pin DC Voltage Range Transient Pulse (Note 2)	 V_S V_{pulse}	 –0.5 to +40 –2.0 to +40	V
V_{CC} Supply DC Voltage Range	V_{CC}	–0.3 to +6.0	V
DIA and L Pins (Note 2) DC Voltage Range Transient Pulse (Clamped by Internal Diode) DC Source Current DIA Low Level Sink Current	–	 –0.5 to +40 –2.0 –50 Int. Limit	 V V mA mA
TXD DC Voltage Range	–	–0.3 to V_{CC} + 0.3	V
REF–IN DC Voltage Range $V_S < V_{CC}$ $V_S > V_{CC}$	–	 –0.3 to V_{CC} –0.3 to V_S	V
ESD Voltage Capability (Note 3)	$V_{(ESD)}$	±2000	V

NOTES: 1. The device is compatible with Specification: “Diagnosis System ISO 9141”.
2. See the test circuit (Figure 23). Transient test pulse according to ISO 76371 and DIN 40839; highest test levels.
3. Human Body Model; C = 100 pF, R = 1500 Ω.

THERMAL RATINGS

Rating	Symbol	Value	Unit
Storage Temperature	T_{stg}	–55 to +150	°C
Operating Junction Temperature	T_J	–40 to +150	°C
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	180	°C/W
Maximum Power Dissipation (@ T_A = 105°C)	P_D	250	mW

ELECTRICAL CHARACTERISTICS (– 40°C ≤ T_A ≤ 125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V, 4.5 V ≤ V_S ≤ 20 V, unless otherwise noted. Typical values reflect approximate mean at 25°C, nominal V_{CC} and V_S, at time of device characterization.)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} PIN 1					
V_{CC} Supply Voltage Range	V_{CC}	4.5	–	5.5	V
V_{CC} Supply Current (Note 1)	I_{CC}	0.5	1.0	1.5	mA
REF–IN–L PIN 2 AND REF–IN–K PIN 3					
REF–IN–L and REF–IN–K Input Voltage Range For $0 < V_S < V_{CC}$ For $V_{CC} < V_S < 40$ V	V_{inref}	 2.0 2.0	 – –	 V_{CC} – 2.0 V V_S – 1.0 V	V
REF–IN–L and REF–IN–K Inputs Currents	I_{VIN}	–5.0	–	5.0	µA
LO PIN 4					
LO Open Collector Output Low Level Voltage @ I_{out} = 1.0 mA Low Level Voltage @ I_{out} = 4.0 mA	V_{OL}	 – –	 0.34 –	 0.7 0.8	V
RXD PIN 5					
Pull–Up Resistor to V_{CC}	R_{RXD}	1.5	2.0	2.5	kΩ
Low Level Voltage @ I_{out} = 1.0 mA	V_{OL}	–	0.3	0.7	V

NOTES: 1. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load. REF–IN–L and REF–IN–K connected to REF–OUT.
2. $0 < V_{CC} < 5.5$ V, $0 < V_S < 40$ V, $0 < V_{DIA} < 20$ V, TXD high or floating.
3. When an over temperature is detected, the DIA output is forced “off”.
4. $0 < V_{CC} < 5.5$ V, $0 < V_S < 40$ V, $0 < V_L < 20$ V.
5. At static “High” or “Low” level TXD, the current source I1 delivers a current of 3.0 mA (typ). Only during “Low” to “High” transition, does this current increase to a higher value in order to charge the K Line capacitor (CL < 4.0 nF) in a short time (see Figure 3).
6. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load, REF–IN–L and REF–IN–K connected to REF–OUT.

ELECTRICAL CHARACTERISTICS (continued) ($-40°C \le T_A \le 125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, $4.5\ V \le V_S \le 20\ V$, unless otherwise noted. Typical values reflect approximate mean at 25°C, nominal V_{CC} and V_S, at time of device characterization.)

Characteristic	Symbol	Min	Typ	Max	Unit
TXD PIN 6					
High Level Input Voltage	V_{IH}	0.7 V_{CC}	2.8	–	V
Low Level Input Voltage	V_{IL}	–	2.0	0.3 V_{CC}	V
Input Current @ $0 < V_S < 40\ V$ TXD at High Level TXD at Low Level	 I_H I_L	 –200 –600	 – –	 30 –100	µA
DIA INPUT/OUTPUT PIN 9					
Low Level Output Voltage @ I = 30 mA	V_{OL}	0	0.35	0.8	V
Drive Current Limit	I_{Lim}	40	–	120	mA
High Level Input Threshold Voltage (REF–IN–K Connected to REF–OUT)	V_{IH}	V_{ref} min + 0.25 V	V_{ref} + 0.325 V	V_{ref} max + 0.4 V	V
Low Level Input Threshold Voltage (REF–IN–K Connected to REF–OUT)	V_{IL}	V_{ref} min – 0.2 V	V_{ref} – 0.125 V	V_{ref} max – 0.05 V	V
Input Hysteresis	V_{Hyst}	300	450	600	mV
Positive Clamp @ 5.0 mA	V_{Cl+}	37	40	44	V
Negative Clamp @ – 5.0 mA	$V_{Cl–}$	–1.5	–0.6	–0.3	V
Leakage Current (Note 2)	I_{Leak}	4.0	10	16	µA
Over Temperature Shutdown (Note 3)	T_{Lim}	155	–	–	°C
L INPUT PIN 12					
High Level Input Threshold Voltage (REF–IN–L Connected to REF–OUT)	V_{IH}	V_{ref} min + 0.25 V	V_{ref} + 0.325 V	V_{ref} max + 0.4 V	V
Low Level Input Threshold Voltage (REF–IN–L Connected to REF–OUT)	V_{IL}	V_{ref} min – 0.2 V	V_{ref} – 0.125 V	V_{ref} max – 0.05 V	V
Input Hysteresis	V_{Hyst}	300	450	600	mV
Leakage Current (Note 4)	I_{Leak}	4.0	10	16	µA
Positive Clamp @ 5.0 mA	V_{Cl+}	37	40	44	V
Negative Clamp @ – 5.0 mA	$V_{Cl–}$	–1.5	–0.6	–0.3	V
I1 PIN 11					
Static Source Current	$I1_S$	–4.0	–3.0	–2.0	mA
Static Saturation Voltage ($I1_S$ = – 2.0 mA)	$V_{I1(sat)}$	V_S – 1.2	V_S – 0.8	V_S	V
Dynamic Source Current (Note 5)	$I1_d$	–120	–80	–40	mA
Dynamic Saturation Voltage ($I_{I1(sat)}$ = – 40 mA)	$V_{I1(dsat)}$	V_S – 2.7	V_S – 0.85	V_S	V
VS PIN 13					
V_S Supply Voltage Range	V_S	4.5	–	20	V
V_S Supply Current (Note 6)	I_S	0.5	1.3	2.0	mA

NOTES: 1. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load. REF–IN–L and REF–IN–K connected to REF–OUT.
2. $0 < V_{CC} < 5.5\ V$, $0 < V_S < 40\ V$, $0 < V_{DIA} < 20\ V$, TXD high or floating.
3. When an over temperature is detected, the DIA output is forced “off”.
4. $0 < V_{CC} < 5.5\ V$, $0 < V_S < 40\ V$, $0 < V_L < 20\ V$.
5. At static “High” or “Low” level TXD, the current source I1 delivers a current of 3.0 mA (typ). Only during “Low” to “High” transition, does this current increase to a higher value in order to charge the K Line capacitor (CL < 4.0 nF) in a short time (see Figure 3).
6. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load, REF–IN–L and REF–IN–K connected to REF–OUT.

ELECTRICAL CHARACTERISTICS (continued) (– 40°C ≤ T_A ≤ 125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V, 4.5 V ≤ V_S ≤ 20 V, unless otherwise noted. Typical values reflect approximate mean at 25°C, nominal V_{CC} and V_S, at time of device characterization.)

Characteristic	Symbol	Min	Typ	Max	Unit
REF–OUT PIN 14					
Output Voltage 3.0 < V_S < 5.6 V and I_{RO} = ±10 µA 5.6 < V_S < 18 V and I_{RO} = ±10 µA 18 < V_S < 40 V and I_{RO} = ±10 µA	V_{ref}	 2.7 0.5 x V_S 8.5	 – – –	 3.3 0.56 x V_S 10.8	V
Maximum Output Current	I_{out}	–50	–	50	µA
Pull–Up Resistor to V_{CC}	R_{PU}	3.0	8.0	12	kΩ

NOTES: 1. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load. REF–IN–L and REF–IN–K connected to REF–OUT.
2. 0 < V_{CC} < 5.5 V, 0 < V_S < 40 V, 0 < V_{DIA} < 20 V, TXD high or floating.
3. When an over temperature is detected, the DIA output is forced “off”.
4. 0 < V_{CC} < 5.5 V, 0 < V_S < 40 V, 0 < V_L < 20 V.
5. At static “High” or “Low” level TXD, the current source I1 delivers a current of 3.0 mA (typ). Only during “Low” to “High” transition, does this current increase to a higher value in order to charge the K Line capacitor (CL < 4.0 nF) in a short time (see Figure 3).
6. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load, REF–IN–L and REF–IN–K connected to REF–OUT.

DYNAMIC CHARACTERISTICS (– 40°C ≤ T_A ≤ 125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V, 4.5 V ≤ V_S ≤ 20 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Transmission Speed	1/t Bit	0	–	200 k	Baud
High or Low Bit Time	t Bit	5.0	–	–	µs
RXD Output Low to High Transition Delay Time High to Low Transition Delay Time	 t_{RDR} t_{RDF}	 – –	 – –	 450 450	ns
LO Output Low to High Transition Delay Time High to Low Transition Delay Time	 t_{LDR} t_{LDF}	 – –	 – –	 2.0 2.0	µs
DIA Output Low to High Transition Delay Time High to Low Transition Delay Time	 t_{DDR} t_{DDF}	 – –	 – –	 650 650	ns
I1 Output (V_S – I1 > 2.7 V) Rise Time Hold Time	 t_{I1R} t_{I1F}	 – 1.5	 – –	 0.3 4.5	µs

Figure 1. TXD to DIA AC Characteristic

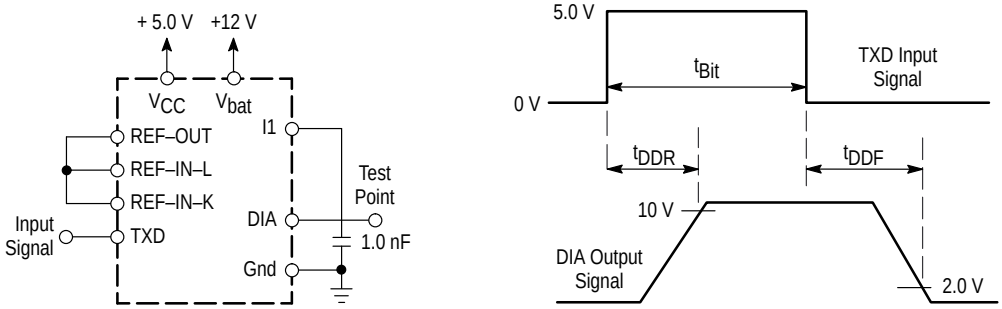


Figure 2. DIA to TXD and L to LO AC Characteristics

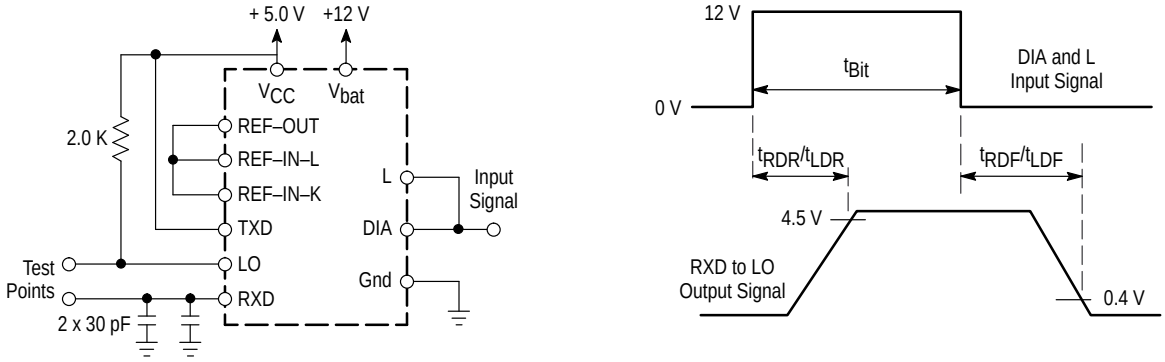


Figure 3. Current Source I1 AC Characteristics

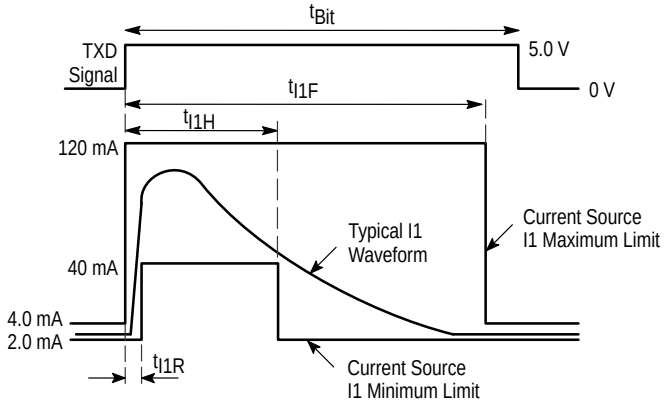
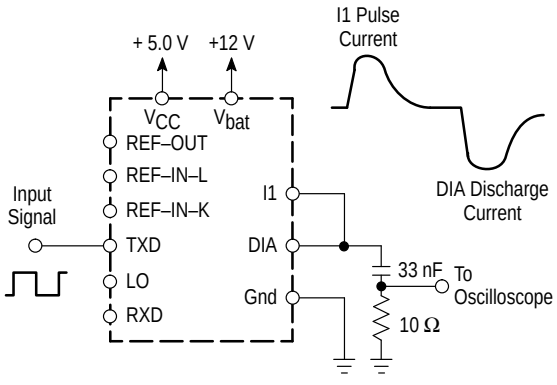


Figure 4. Current Source I1 and DIA Discharge Current Test Schematic



At static “High” or “Low” level TXD, the current source I1 delivers a current of 3.0 mA (typ). Only during “Low” to “High” transition, does this current increase to a higher value in order to charge the K Line capacitor (Cl < 4.0 nF) in a short time.

Figure 5. Logic Diagram and Application Schematic

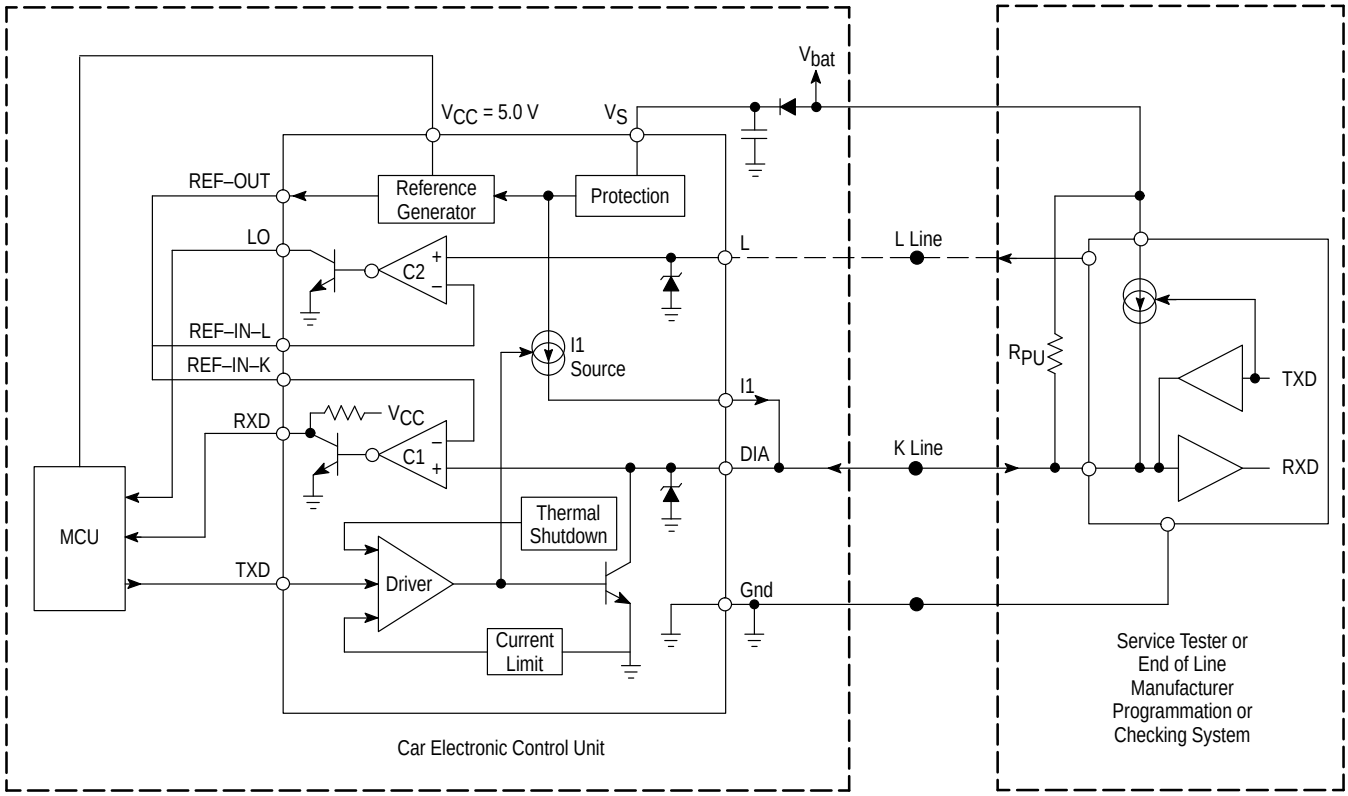


Figure 6. Typical Application with Several ECUs

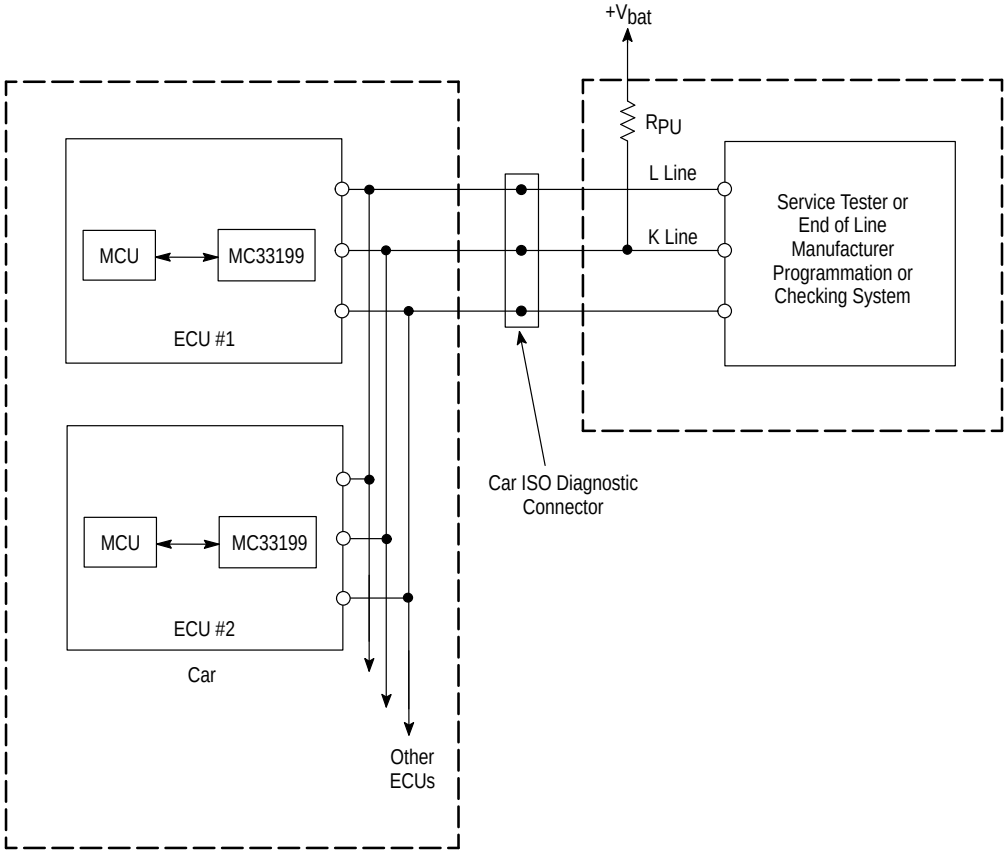


Figure 7. I_{CC} Supply Current versus Temperature

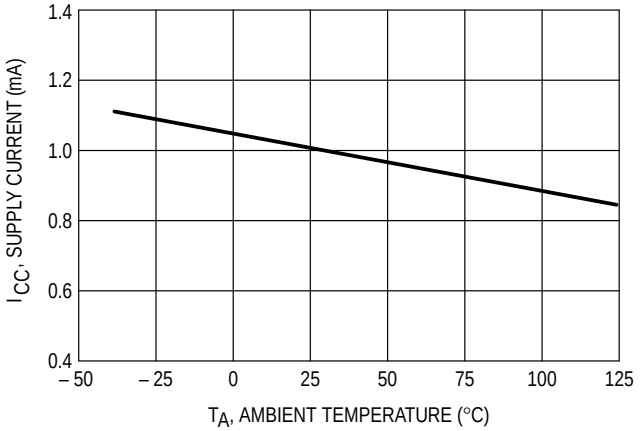


Figure 8. I_S Supply Current versus V_S Supply Voltage

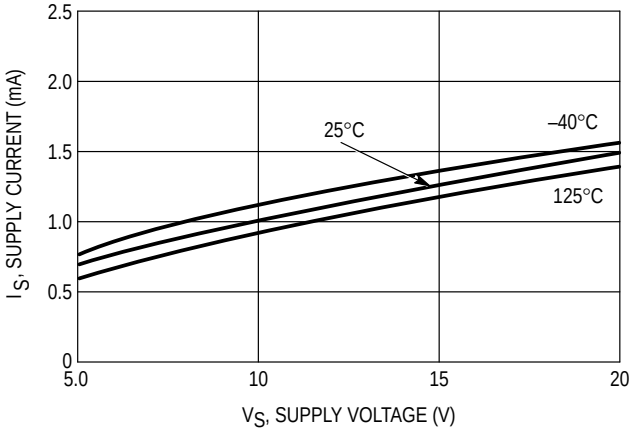


Figure 9. I_S Supply Current versus V_S Supply Voltage

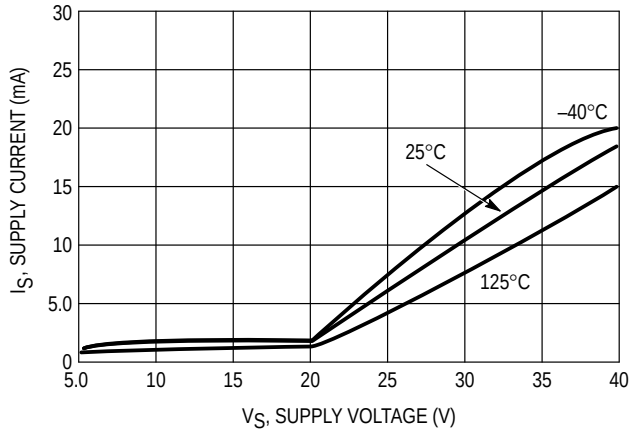


Figure 10. V_S Voltage versus I_S Current

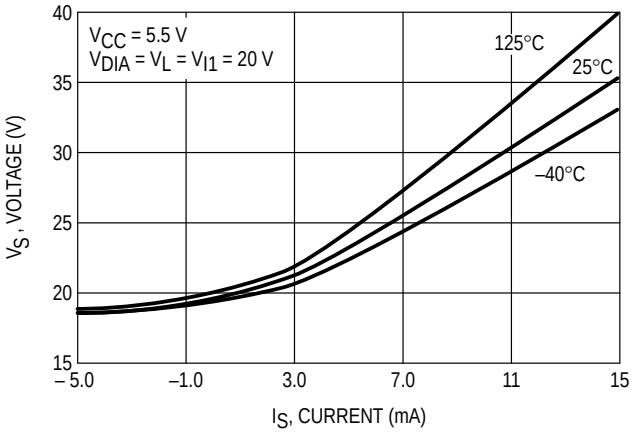


Figure 11. REF–OUT Voltage versus V_S Supply Voltage

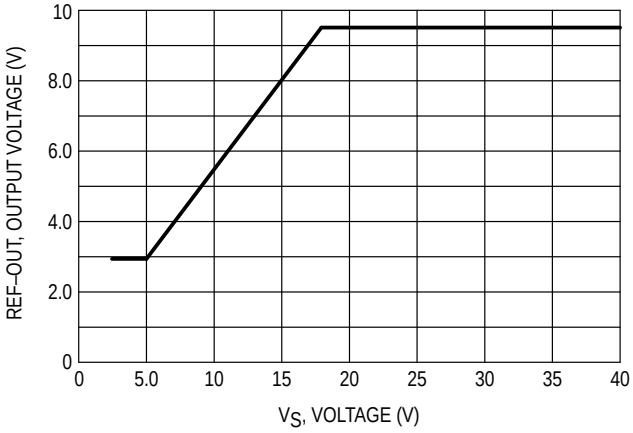


Figure 12. REF–OUT Voltage versus REF–OUT Current

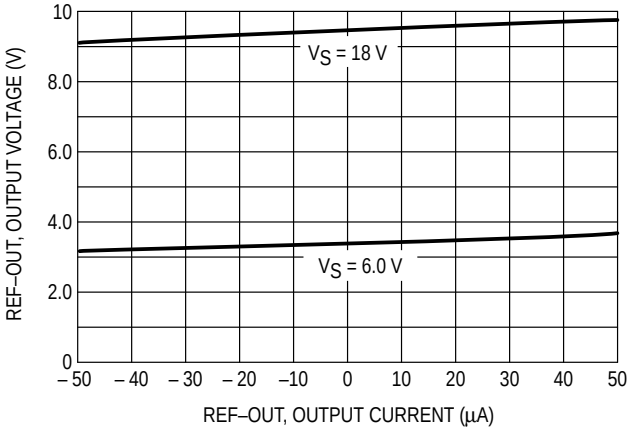


Figure 13. L and DIA Hysteresis versus Ambient Temperature

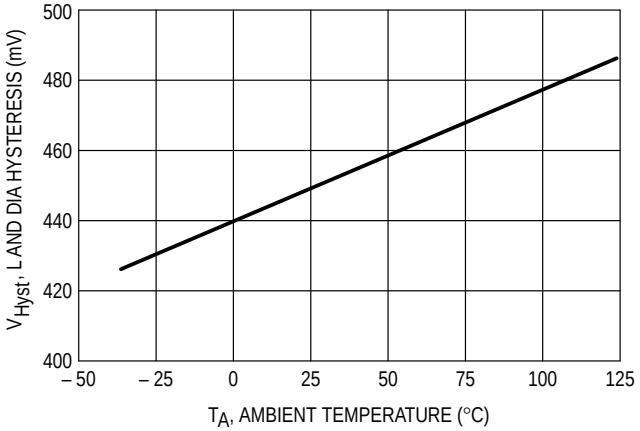


Figure 14. L and DIA Current versus L and DIA Voltage

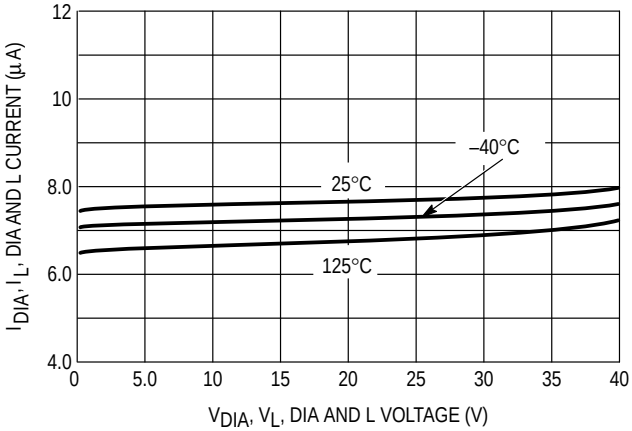


Figure 15. DIA Saturation Voltage versus Temperature

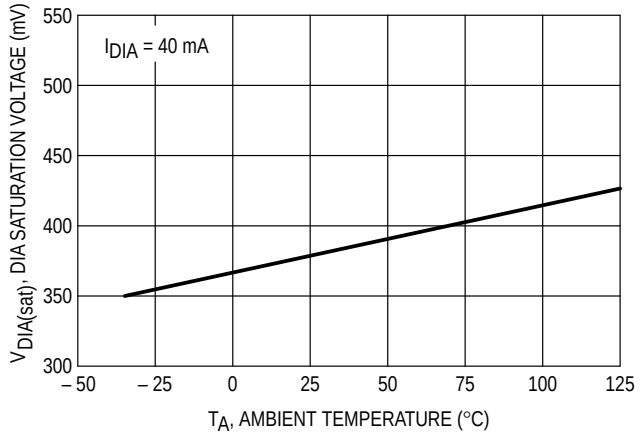


Figure 16. DIA Current Limit versus Temperature

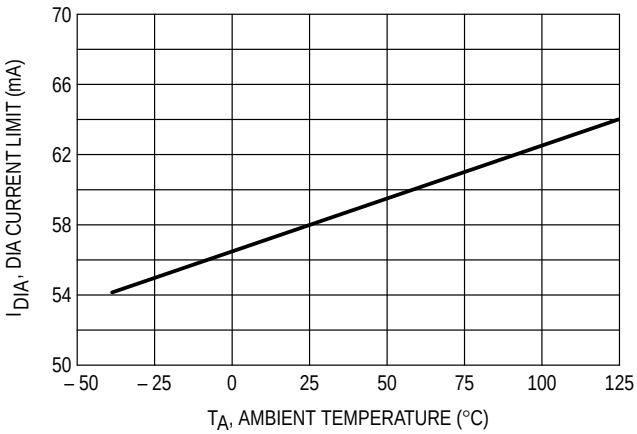


Figure 17. RXD Pull–Up Resistor versus Temperature

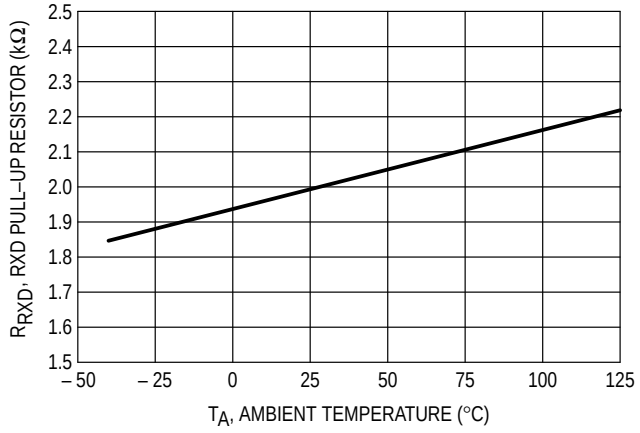


Figure 18. TXD and LO Saturation Voltage versus Temperature

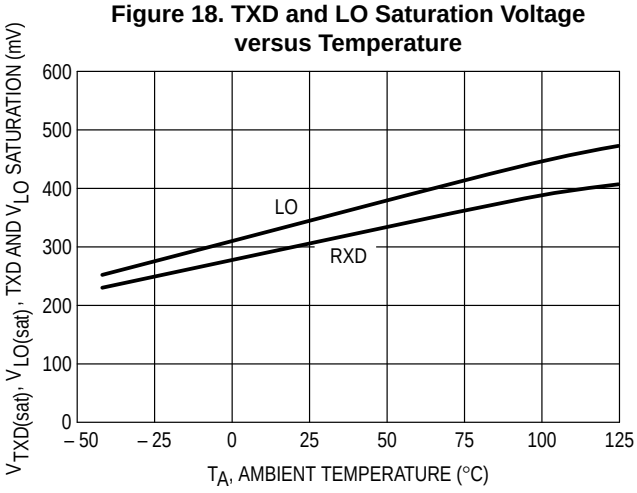


Figure 19. I1 Saturation Voltage versus Temperature

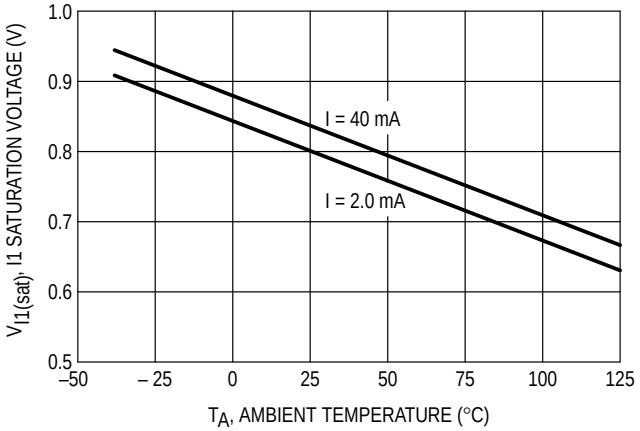


Figure 20. I1 Output DC Current versus Temperature

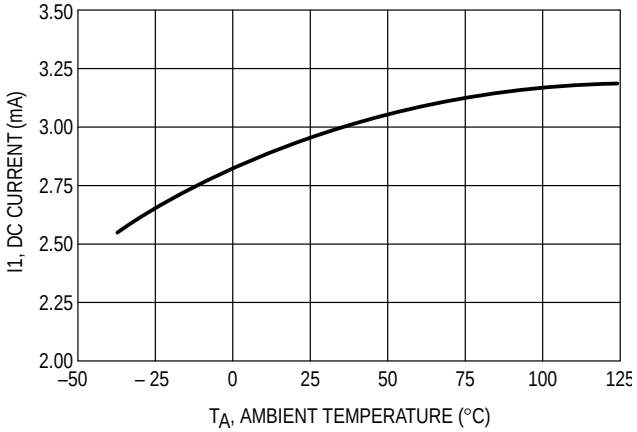


Figure 21. I1 Output Pulse Current versus V_S Supply Voltage

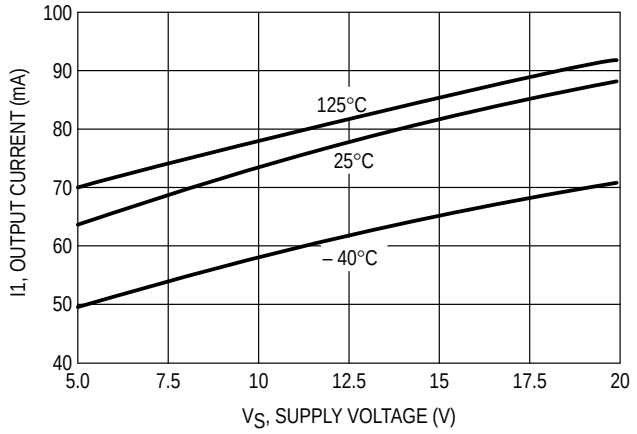


Figure 22. I1 Pulse Current Width versus Temperature

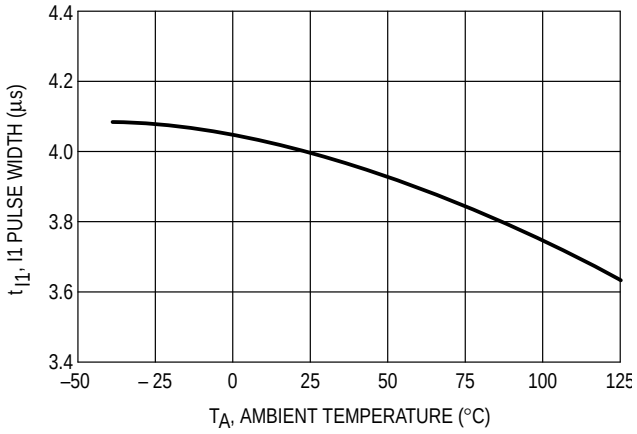
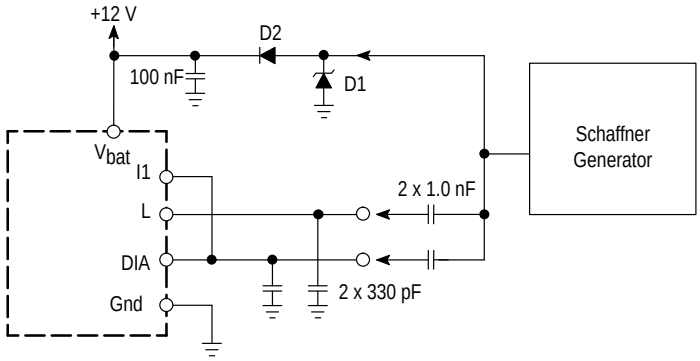


Figure 23. Transient Test Circuit Using Schaffner Generator



Test pulses are directly applied to V_S and via a capacitor of 1.0 nF to DIA and L. The voltage V_S is limited to – 2.0 V/40 V by the transient suppressor diode D1. Pulses can occur simultaneously or separately.

INTRODUCTION

The MC33199 is a serial interface circuit used in diagnostic applications. It is the interface between the microcontroller and the special K and L Lines of the ISO diagnostic port. The MC33199 has been designed to meet the “Diagnosis System ISO 9141” specification.

This product description will detail the functionality of the device (see simplified application). The power supply and reference voltage generator will be discussed followed by the path functions between MCU, K and L Lines. A dedicated paragraph will discuss the special functionality of the I1 pin in it’s ability to accommodiate high baud rate transmissions.

Power Supplies and Reference Voltage

The device requires two power supplies to be used; a 5.0 V supply, V_{CC}, which is normally connected to the MCU supply. The device V_{CC} pin is capable of sinking typically 1.0 mA during normal operation. A V_{bat} supply voltage, V_S, is normally tied to the car’s battery voltage. The V_{bat} pin can sustain up to 40 V dc. Care should be taken to provide any additional reverse battery and transient voltage protection in excess of 40 V.

The voltage reference generator is supplied from both V_{CC} and V_{bat} pins. The voltage reference generator provides a reference voltage for the K and L Line comparator thresholds. The reference voltage is dependant on the V_{bat} voltage; it is linear in relation to the V_{bat} voltage for all V_{bat} voltages between 5.6 V and 18 V. Below 5.6 V and over 18 V the reference voltage is clamped (see Figure 11). The REF–OUT pin connects the reference voltage out externally making it available for other application needs. The REF–OUT pin is capable of supplying a current of 50 μA (see Figure 12).

Path Functions Between MCU, K and L Lines

The path function from the MCU to the K Line uses a driver to interface directly with the MCU through the TXD pin. The TXD pin is CMOS compatible. This driver controls the On–Off conduction of the power transistor. When the power transistor is On, it pulls the DIA pin low. This pin is known as K Line in the ISO 9141 specification. The DIA pin structure is open collector and requires an external pull–up resistor for use. Having an open collector without an internal pull–up resistor allows several MC33199 to be connected to the K Line while using a single pull–up resistor for the system (see Figure 6). In order to protect the DIA pin against short circuits to V_{bat}, the MC33199 incorporates an internal current limit (see Figure 16) and thermal shutdown circuit. The current limit feature makes it possible for the device to drive a K Line bus having a large parasitic capacitor value (see Special Functionality of I1 pin below).

The path from the DIA pin, or K Line, to the MCU is done through a comparator. The comparator threshold voltage is connected to REF–IN–K pin. It can be tied to the REF–OUT voltage if a V_{bat} dependant threshold is required in the application. The second input of this comparator is connected internally to DIA pin. The output of this comparator is available at the RXD output pin and normally connects to an MCU I/O port. RXD pin has a 2.0 kΩ internal pull–up resistor.

The path from the L Line, used during a wake–up sequence of the transmission, to the MCU is done through a second comparator. The comparator threshold voltage is connected to REF–IN–L pin. The REF–IN–K pin can be tied to the REF–OUT voltage if a V_{bat} dependant threshold is required in the application. The second input of this comparator is internally connected to L pin. The output of this comparator is available on LO output pin, which is also an open collector structure. The LO pin is normally connected to an MCU I/O port.

The DIA and L pins can sustain up to 40 V dc. Care should be taken to protect these pins from reverse battery and transient voltages exceeding 40 V.

The DIA and L pins both have internal pull–down current sources of typically 7.5 μA (see Figure 14). The L Line exhibits a 10 μA pull–down current. The DIA pin has the same behavior when it is in “off” state, that is when TXD is at logic high level.

Special Functionality of I1 Pin

The MC33199 has a unique feature which accommodates transmission baud rates of up to 200 k baud. In practice, the K Line can be several meters long and have a large parasitic capacitance value. Large parasitic capacitance values will slow down the low to high transition of the K Line and limit the baud rate transmission. For the K Line to go from low to high level, the parasitic capacitor must first be charged, and can only be charged through the pull–up resistor. A low pull–up resistor value would result in fast charge time of the capacitor but also large output currents to be supplied causing a high power dissipation in the driver.

To avoid this problem, the MC33199 incorporates a dynamic current source which is temporarily activated at the low to high transition of the TXD pin when the DIA pin or K Line switches from a low to high level (see Figures 3 and 4).

This current source is available at the I1 pin. The I1 pin has a typical current capability of 80 mA. It is activated for 4.0 μs (see Figures 21 and 22) and is automatically disabled after this time. During this time it will charge the K Line parasitic capacitor. This extra current will quickly increase the K Line voltage up to V_{bat}, resulting in a reduced rise time of the K Line. With this feature, the MC33199 ensures baud rate transmission of up to 200 k baud.

During high to low transitions of the K Line, the parasitic capacitor of the line will be discharged by the output transistor of the DIA pin. In this case, the total current may exceed the internal current limitation of the DIA pin. If so, the current limit circuit will activate, limiting the discharge current to typically 60 mA (see Figures 4 and 16).

If a high baud rate is necessary, the I1 pin should be connected to the DIA as shown in the typical application circuit shown in Figure 5. The I1 pin can be left open, if the I1 functionality and high baud rate are not required for the application.

PIN DESCRIPTION

Pin 1: V_{CC}

Power Supply pin; typically 5.0 V and requiring less than 1.5 mA.

Pin 2: REF–IN–L

Input reference for C2 comparator. This input can be connected directly to REF–OUT with or without a resistor network or to an external reference.

Pin 3: REF–IN–K

Input reference for C1 comparator. This input can be connected directly to REF–OUT with or without a resistor network or to an external reference.

Pin 4: LO

Output of C2 comparator and normally connected to a microcontroller I/O. If L input > (REF–IN–L + Hyst/2); output LO is in high state. If L< (REF–IN–L – Hyst/2); output LO is in low state and the output transistor is “on”. This pin is an open collector structure and requires a pull–up resistor to be connected to V_{CC}. Output drive capability of this output is 5.0 mA.

Pin 5: RXD

Receive output normally connected to a microcontroller I/O. If DIA input > (REF–IN–L + Hyst/2); output LO is in high state. If DIA < (REF–IN–L – Hyst/2); output LO is in low state and the output transistor is “on”. This pin has an internal pull–up resistor (typically 2.0 kΩ) connected to V_{CC}. Drive capability of this output is 5.0 mA.

Pin 6: TXD

Transmission input normally connected to a microcontroller I/O. This pin controls the DIA output. If TXD is high, the output DIA transistor is in the “off” state. If TXD is low, the DIA output transistor is “on”.

Pin 9: DIA

Input/Output Diagnosis Bus line pin. This pin is an open collector structure and is protected against overcurrent and circuit shorts to V_{bat} and V_S. Whenever the open collector transistor turns “on” (TXD low), the Bus line is pulled to ground and the DIA pin current is internally limited to nominal value of 60 mA. The internal power transistor incorporates a thermal shutdown circuit which forces the DIA output “off” in the event of an over temperature condition. The DIA pin is also the C1 comparator input. It is protected against both positive and negative overvoltages by an internal 40 V zener diode. This pin exhibits a constant input current of 7.5 μA.

Pin 10: Gnd

Ground reference for the entire device.

Pin 11: I1

Bus source current pin. It is normally tied to DIA pin and to the Bus line. The current source I1 delivers a nominal current of 3.0 mA at static “High” or “Low” levels of TXD. Only during “Low” to “High” transitions, does this current increase to a higher value so as to charge the key line capacitor (Cl < 4.0 nF) in a short time (see Figures 3 and 4).

Pin 12: L

Input for C2 comparator. This pin is protected against both positive and negative overvoltage by a 40 V zener diode. This L Line is a second independent input. It can be used for wake up sequence in ISO diagnosis or as an additional input bus line. This pin exhibits a constant input current of 7.5 μA.

Pin 13: V_S

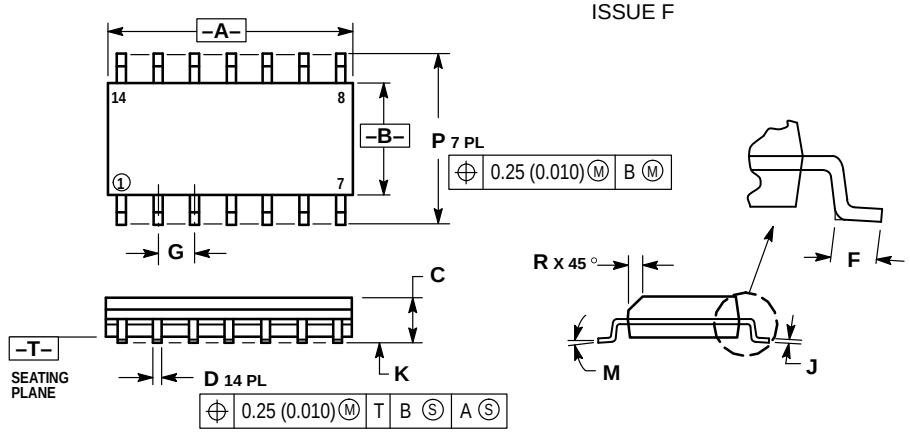
12 V typical, or V_{bat} supply pin for the device. This pin is protected against overvoltage transients.

Pin 14: REF–OUT

Internal reference voltage generator output pin. Its value depends on V_S (V_{bat}) values. This output can be directly connected to REF–IN–L and REF–IN–K, or through a resistor network. Maximum current capability is 50 μA.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MOTOROLA

◊ 1PHX36048–0 PRINTED IN USA 10/95 IMPERIAL LITHO 20314 4,500 LIN/INT YCAAAA

MC33199/D