

**DUAL 5.1V REGULATOR WITH DISABLE AND RESET**

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT VOLTAGES  
5.1V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH  
OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE

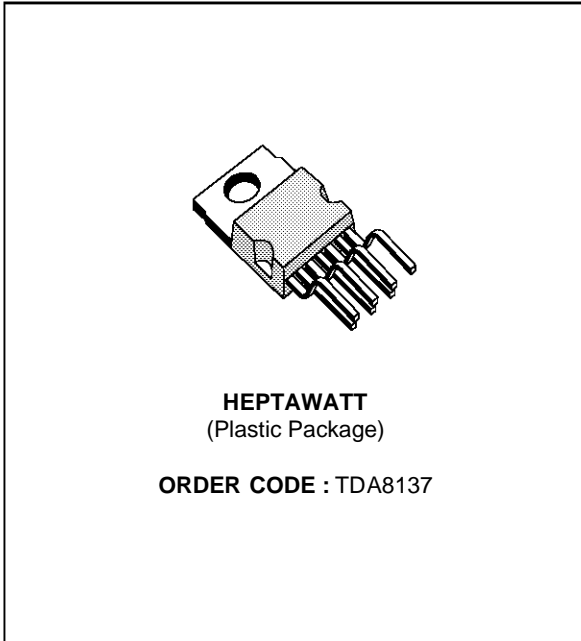
**DESCRIPTION**

The TDA8137 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V at currents up to 1A.

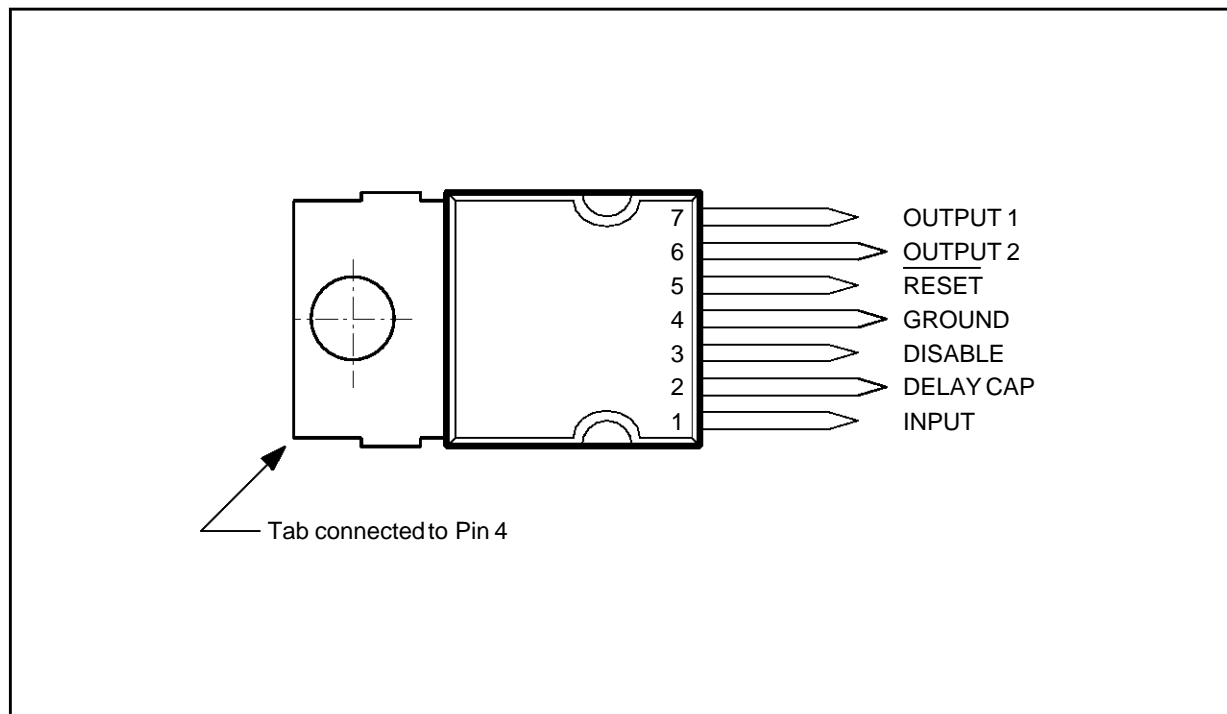
An internal reset circuit generates a reset pulse when the output 1 decreases below the regulated voltage value.

Output 2 can be disabled by TTL input.

Short circuit and thermal protections are included.



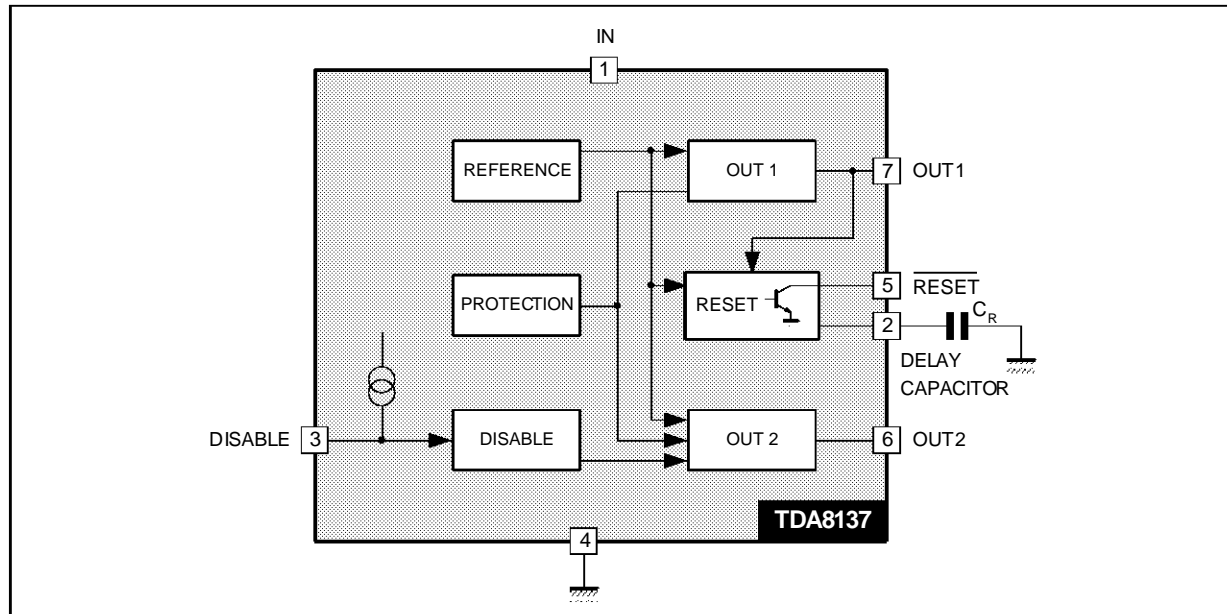
**PIN CONNECTION (top view)**



8137-01.EPS

# TDA8137

## BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN}$	DC Input Voltage Pin 1	20	V
$V_{DIS}$	Disable Input Voltage Pin 3	20	V
$V_{RST}$	Output Voltage at Pin 5	20	V
$I_{O1, 2}$	Output Currents	Internally Limited	
$P_t$	Power Dissipation	Internally Limited	
$T_{STG}$	Storage Temperature	- 65 to + 150	°C
$T_j$	Junction Temperature	0 to + 150	°C

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## THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	3	°C/W
$T_j$	Recommended Junction Temperature	0 to + 150	°C

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## ELECTRICAL CHARACTERISTICS ( $V_{IN} = 7V$ ; $T_j = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{O1, 2}$	Output Voltage	$I_{O1, 2} = 10mA$	5	5.1	5.2	V
		$7V < V_{IN} < 14V, 5mA < I_0 < 750mA$	4.9		5.3	V
$V_{I01, 2}$	Dropout Voltage	$I_{O1, 2} = 750mA$			1.4	V
		$I_{O1, 2} = 1A$			2	V
$\Delta V_{O1, 2LI}$	Line Regulation	$7V < V_{IN} < 14V, I_{O1, 2} = 200mA$			50	mV
$\Delta V_{O1, 2LO}$	Load Regulation	$5mA < I_{O1, 2} < 0.6A$			100	mV
$I_Q$	Quiescent Current	$I_{O1} = 10mA, \text{Output 2 Disabled}$			2	mA
$V_{O1RST}$	Reset Threshold Voltage	$(K = V_{O1})$	K-0.4	K-.25	K-0.1	V
$V_{RTH}$	Reset Threshold Hysteresis	(see circuit description)	20	50	75	mV
$t_{RD}$	Reset Pulse Delay at Pin 5	$C_e = 100nF$ (see circuit description)		25		ms
$V_{RL}$	Saturation Volt. at Pin 5 in Reset Condition	$I_5 = 5mA$			0.4	V

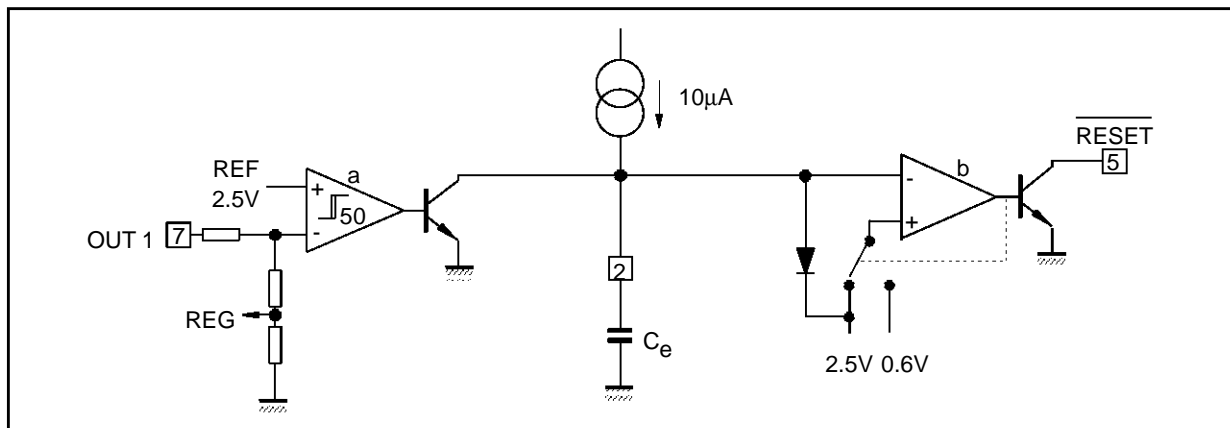
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**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 7V$  ;  $T_j = 25^\circ C$  unless otherwise specified) (continued)

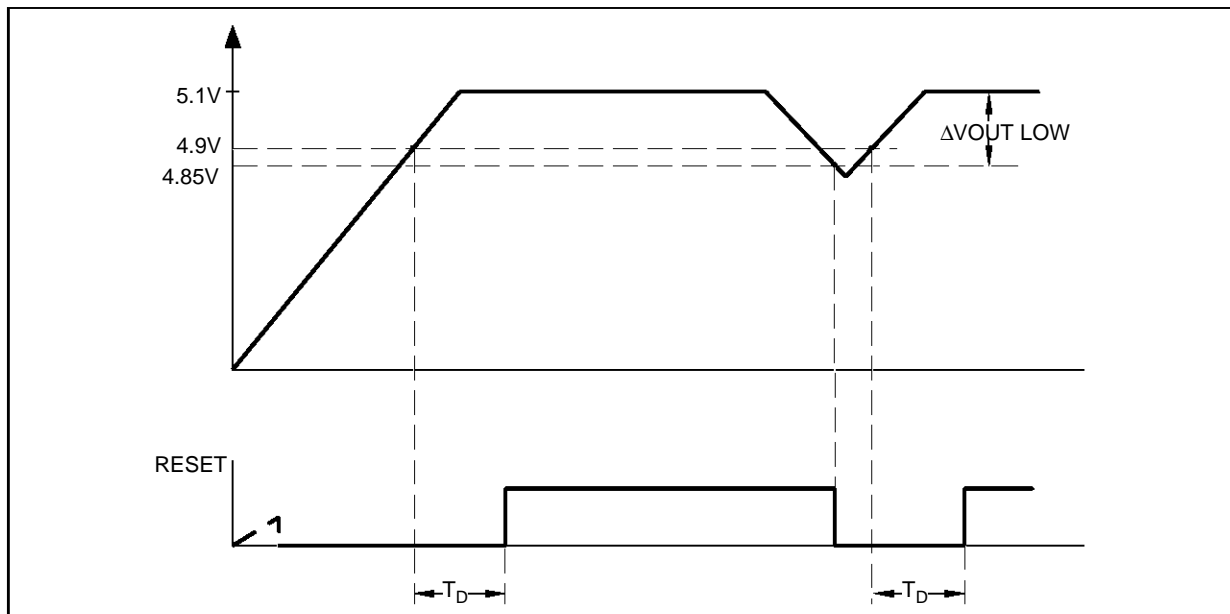
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{RH}$	Leakage Current at Pin 5 in Normal Condition	$V_5 = 10V$			10	$\mu A$
$K_{0,2}$	Output Volt. Thermal Drift	$K_0 = \frac{\Delta V_o \cdot 10^6}{\Delta T \cdot V_o}$ $T_j = 0 \text{ to } +125^\circ C$		100		ppm/ $^\circ C$
$I_{01,2SC}$	Short Circ. Output Current	$V_{IN} = 7V$			1.6	A
		$V_{IN} = 16V$ , (see note 1)			1	A
$V_{DISH}$	Disable Volt. at Pin 3 High (out 2 active)		2			V
$V_{DISL}$	Disable Volt. at Pin 3 Low (out 2 disabled)				0.8	V
$I_{DIS}$	Disable Bias Current at Pin 3	$0V < V_{DIS} < 7V$	-100		2	$\mu A$
$T_{jsd}$	Junction Temp. for Thermal Shut Down			145		$^\circ C$

**Note 1:** The output short circuit currents are tested one channel at time. During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value. Safe permanent short-circuit is only guaranteed for input voltages up to 16V.

**Figure 1**



**Figure 2**



## TDA8137

### CIRCUIT DESCRIPTION

The TDA8137 is a dual voltage regulator with Reset and Disable.

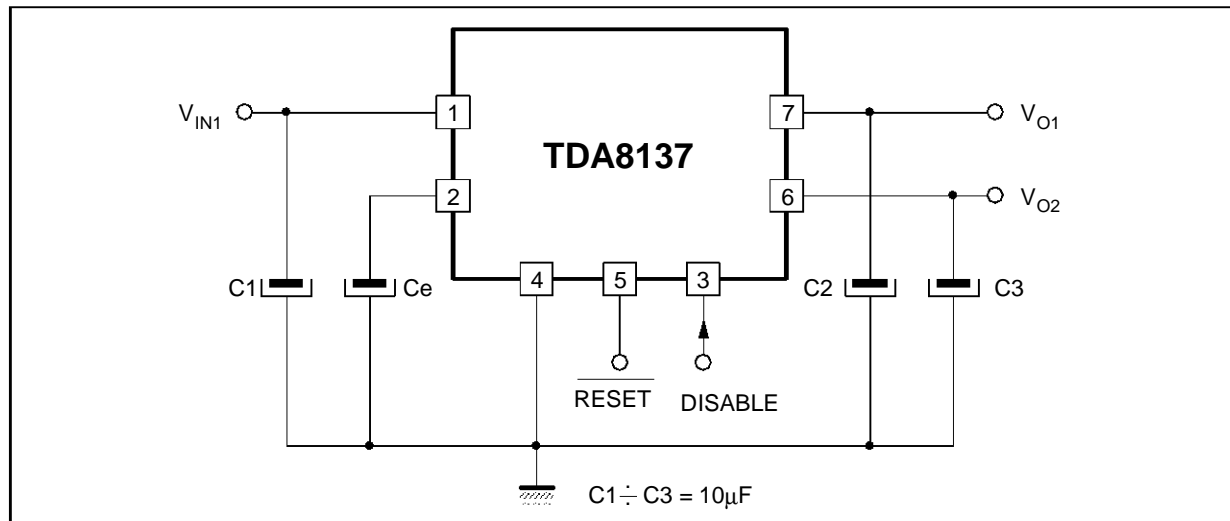
The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at Pin 1 ( $V_{IN1}$ ), the regulator 2 will not work if the Pin 1 is not supplied.

The outputs stages have been realized in darlington configuration with a drop typical of 1.2V.

The disable circuit, switches off the output 2 if a voltage lower than 0.8V is applied at pin 3.

The Reset circuit checks the voltage at the output 1. If this one goes below  $V_{OUT} - 0.25V$  (4.85V Typ.), the comparator "a" (see Figure 1) discharges rapidly the capacitor  $C_e$  and the reset output goes at once low. When the voltage at the OUT 1 rises above  $V_{OUT} - 0.2V$  (4.9V Typ.), the voltage  $V_{C_e}$  increases linearly to 2.5V corresponding to a delay  $t_d$  following the low :  $t_d = \frac{C_e \cdot 2.5V}{10\mu A}$  (see figure 2), then the reset output goes high again. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9V).

### TYPICAL APPLICATION



8137-05.EPS

