DATA SHEET

TDA8444
Octuple 6-bit DAC with I^2C-bus

Product specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

Octuple 6-bit DAC with I²C-bus

TDA8444

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$.

At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38); SOT38-1; 1996 July 23.

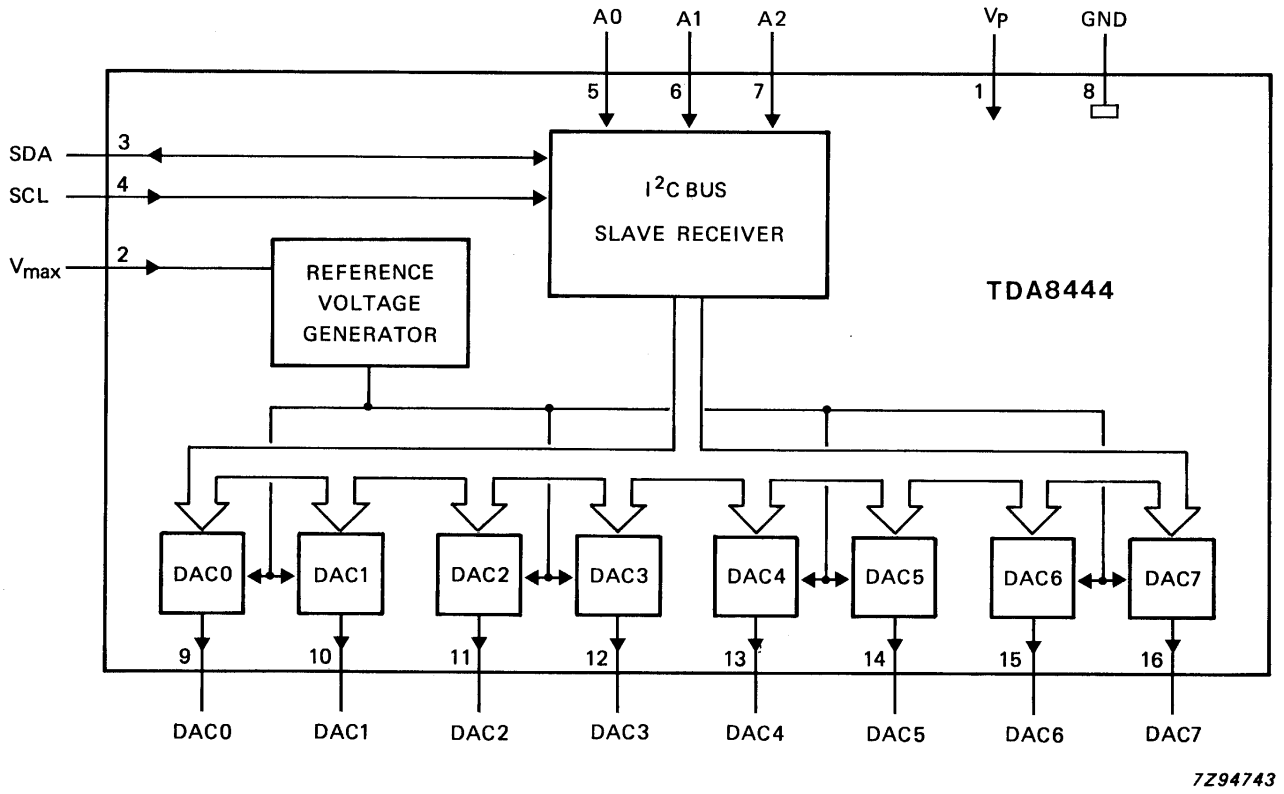


Fig.1 Block diagram.

PINNING

PIN	SYMBOL	DESCRIPTION
1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for I²C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

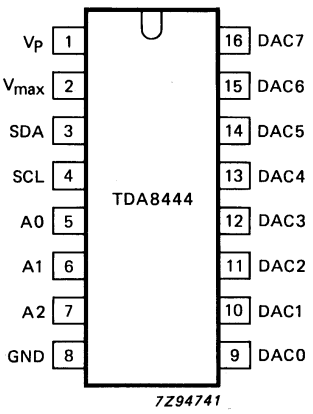


Fig.2 Pinning diagram

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I2C-bus interface is a receive-only slave. Data is accepted from the I2C-bus in the following format:

S	0	1	0	0	A2	A1	A0	0	A	I3	I2	I1	I0	SD	SC	SB	SA	A	X	X	D5	D4	D3	D2	D1	D0	A	P
	<----- address byte ---->									<----- instruction byte ---->									<----- first data byte ---->								

Where:

S = start condition
P = stop condition
A = acknowledge
X = don't care
A2, A1, A0 = programmable address bits
I3, I2, I1, I0 = instruction bits
SD, SC, SB, SA = subaddress bits
D5, D4, D3, D2, D1, D0 = data bits

Fig.3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications. Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to V_P for An = 1. If the inputs are left floating, An = 1 will result.

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	$V_P = V_1$	–0.5	18	V
Supply current (source)	$I_P = I_1$	–	–10	mA
	$I_P = I_I$	–	40	mA
I2C-bus line voltage	$V_{3,4}$	–0.5	5.9	V
Input voltage	V_I	–0.5	$V_P + 0.5$	V
Output voltage	V_O	–0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)	$\pm I_{max}$	–	10	mA
Total power dissipation	P_{tot}	–	500	mW
Operating ambient temperature range	T_{amb}	–20	+70	°C
Storage temperature range	T_{stg}	–55	+150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	75	K/W

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	–10	µA
	V_2 = VP	I_2	–	–	10	µA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	–10	µA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	µA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_{OL}	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0		5	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	–7	–12	µA
Input current HIGH		I_{IH}	–	–	1	µA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P – 0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	VOmin	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at Vmax = VP		V_{Omax}	10	10.5	11.5	V
at 1 < Vmax < 10.5 V		V_{Omax}		see note 1		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0 V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; -2 < I_O < +2 mA	Z_O	–	4	50	Ω
Step value of 1 LSB	V_{max} = V_P; I_O = -2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = -2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = -2 mA; N = 32		0	–	70	mV

Note to the Characteristics

1. $V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

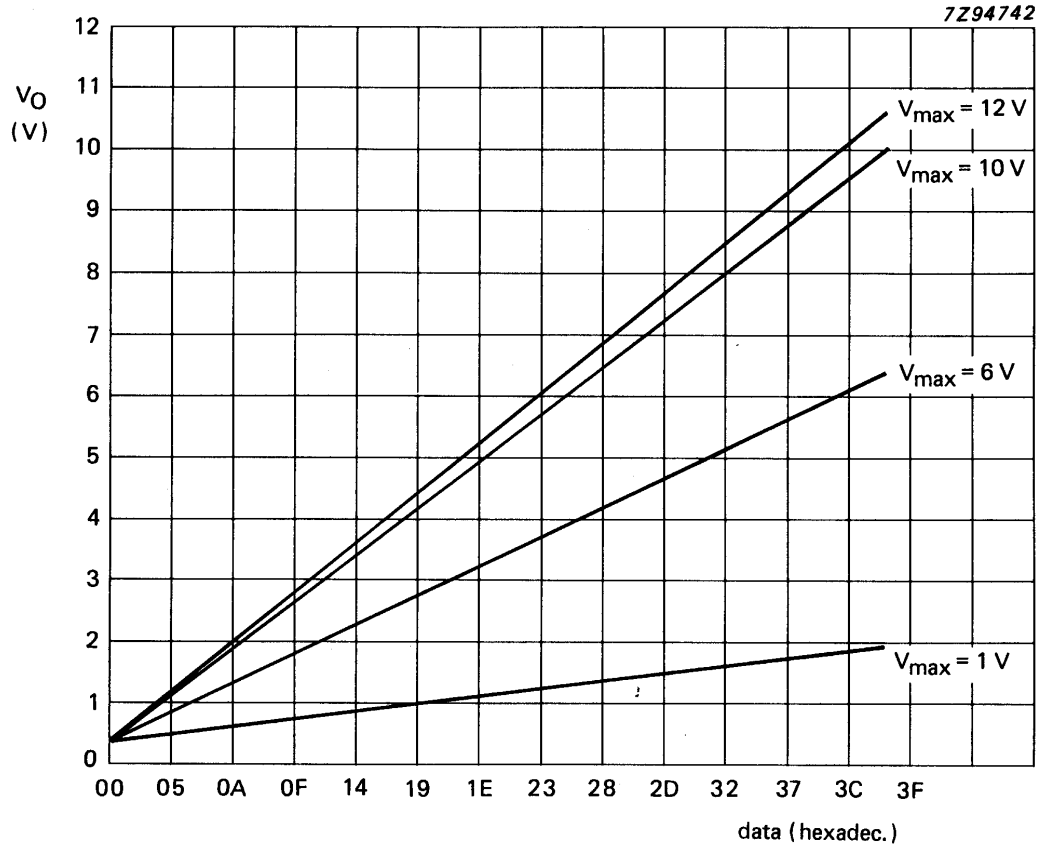
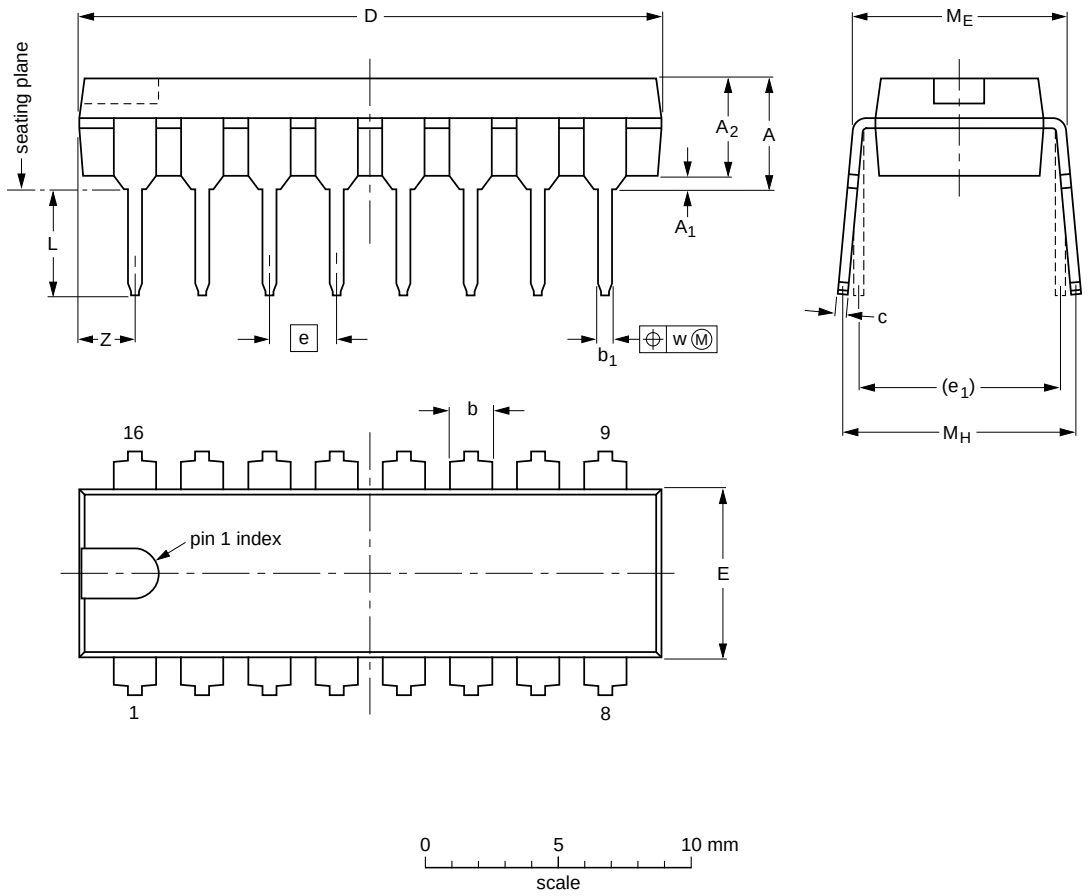


Fig.4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

PACKAGE OUTLINE

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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