

# DATA SHEET

## **TDA8442** I<sup>2</sup>C-bus interface for colour decoders

Product specification  
File under Integrated Circuits, IC01

March 1991

# I<sup>2</sup>C-bus interface for colour decoders

# TDA8442

## GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I<sup>2</sup>C-bus.



## Features

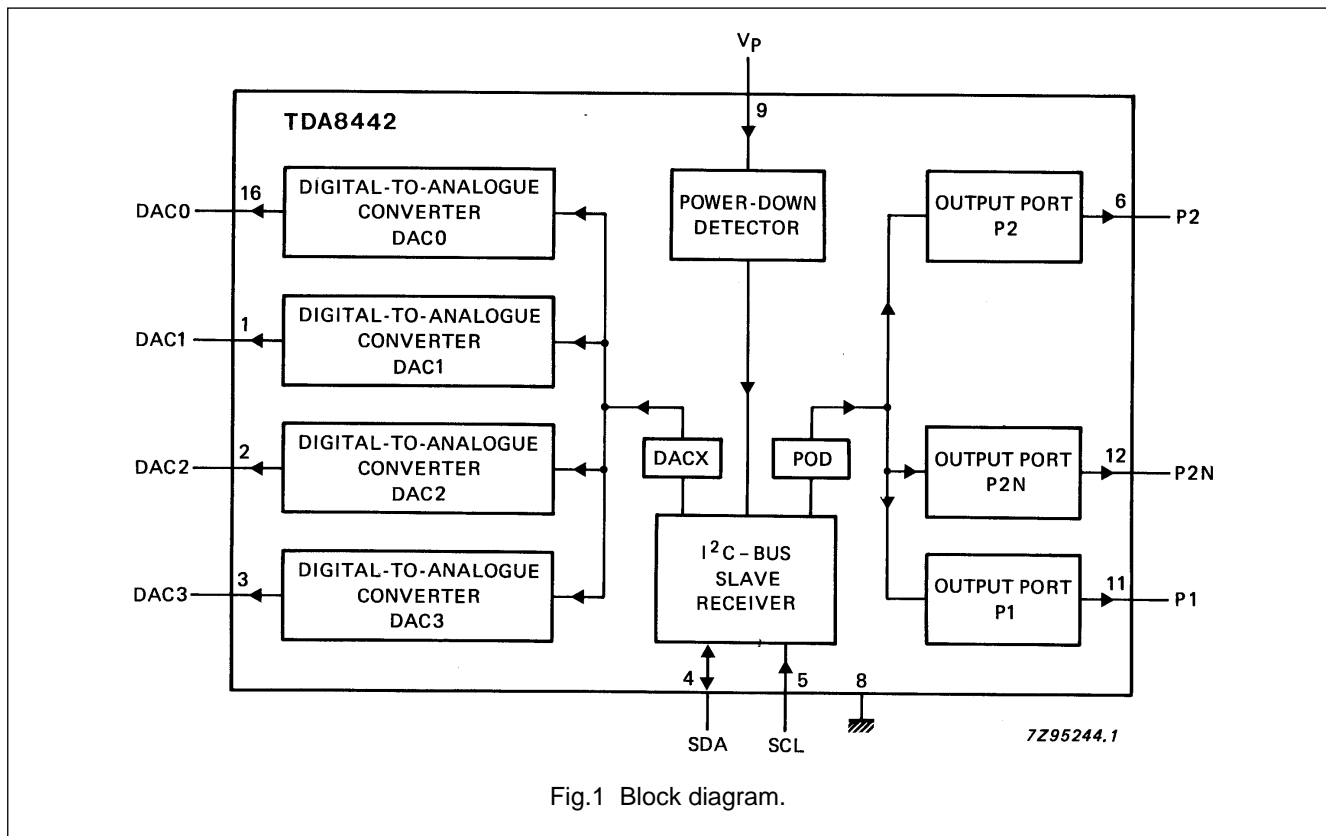
- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I<sup>2</sup>C-bus slave receiver
- Power-down reset.

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT38); SOT38-1; 1996 July 23.

## QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX	UNIT
Supply voltage (pin 9)		V <sub>P</sub>	10.8	12.0	13.2	V
Supply current	no outputs loaded	I <sub>P</sub>	8	13	18	mA
Total power dissipation	no outputs loaded	P <sub>tot</sub>	–	–	1	W
Operating ambient temperature range		T <sub>amb</sub>	–20	–	+ 70	°C

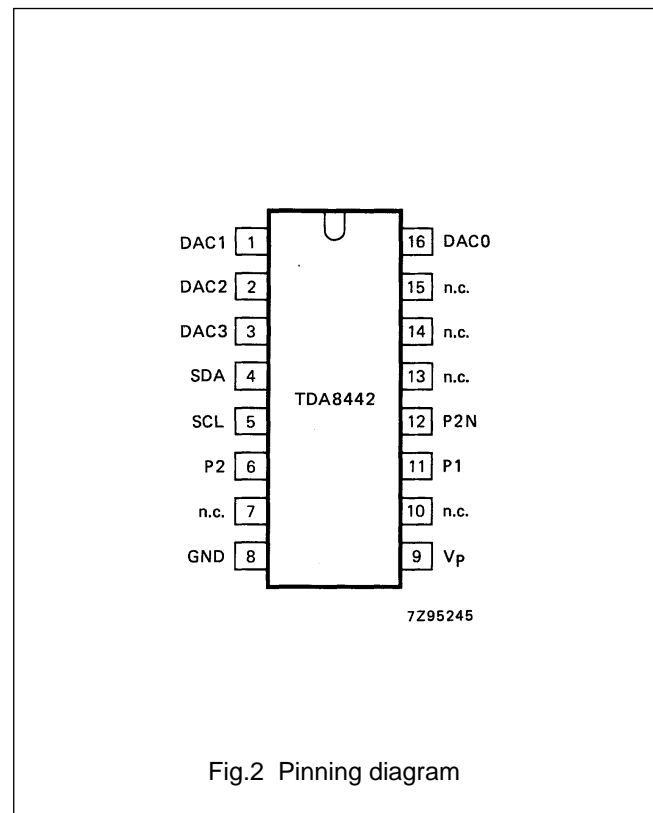


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## PINNING

PIN	SYMBOL	DESCRIPTION
1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue output 3
4	SDA	serial data line; I <sup>2</sup> C-bus
5	SCL	serial clock line; I <sup>2</sup> C-bus
6	P2	Port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V <sub>P</sub>	positive supply voltage
10	n.c.	not connected
11	P1	Port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0



## FUNCTIONAL DESCRIPTION

## Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I<sup>2</sup>C-bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open npn emitter output capable of sourcing 14 mA (min.).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typ.). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the other output is switched off, and vice versa.

## Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8.5 V (typ.) and resets all registers to a defined state.

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## OPERATION

### Write

The TDA8442 is controlled via the I<sup>2</sup>C-bus (specifications for the I<sup>2</sup>C-bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig.3.

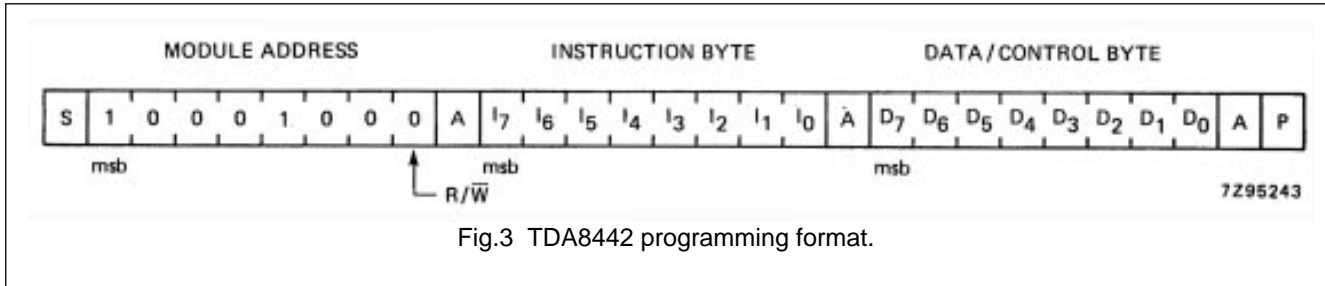


Fig.3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode ( $V_P > 8.5$  V (typ.)).

### Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) together with the corresponding data/control bytes (see Fig.4).

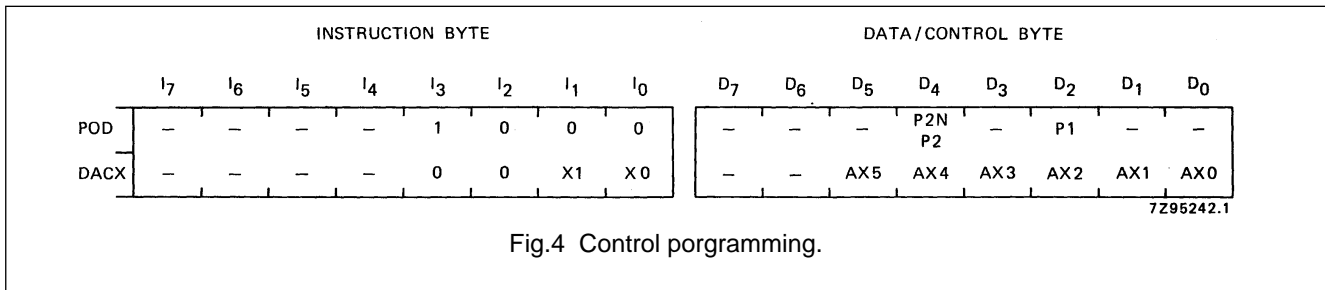


Fig.4 Control programming.

### POD bit P1

If a logic 1 is programmed, the P1 output is switched on. If a logic 0 is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

### POD bit P2/P2N

If a logic 1 is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a logic 0 is programmed or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

### DAX bits AX5 to AX0

The digital-to-analogue converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at logic 0 or when power-down-reset has been activated.

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage range (pin 9)	$V_P$	-0.3	+13.2	V
Input/output voltage ranges				
pin 4	$V_{SDA}$	-0.3	+13.2	V
pin 5	$V_{SCL}$	-0.3	+13.2	V
pin 6	$V_{P2}$	-0.3	$V_P$ ; note 1	V
pin 11	$V_{P1}$	-0.3	$V_P$ ; note 1	V
pin 12	$V_{P2N}$	-0.3	$V_P$ ; note 1	V
pin 1 to 3 and pin 16	$V_{DAX}$	-0.3	$V_P$ ; note 1	V
Total power dissipation	$P_{tot}$	-	1	W
Operating ambient temperature range	$T_{amb}$	-20	+70	°C
Storage temperature range	$T_{stg}$	-55	+150	°C

**Note**

- Pin voltage may exceed  $V_P$  if the current in that pin is limited to 10 mA.

**CHARACTERISTICS** $V_P = 12$  V;  $T_{amb} = +25$  °C; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
Supply voltage (pin 9)		$V_P$	10.8	12.0	13.2	V
Supply current (pin 9)	no outputs loaded	$I_P$	8	13	18	mA
<b>I<sup>2</sup>C-bus inputs</b>						
SDA (pin 4); SCL (pin 5)						
Input voltage HIGH	note 1	$V_{IH}$	3.0	-	$V_P - 1$	V
Input voltage LOW		$V_{IL}$	-0.3	-	1.5	V
Input current HIGH	note 1	$I_{IH}$	-	-	10	μA
Input current LOW	note 1	$I_{IL}$	-	-	10	μA
<b>I<sup>2</sup>C-bus output</b>						
SDA (pin 4)						
Output voltage LOW	open collector $I_{OL} = 3.0$ mA	$V_{OL}$	-	-	0.4	V
Maximum output sink current		$I_{OL}$	3	5	-	mA

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>Ports P2 and P2N</b>						
(pins 6 and 12)	npn collector output with pull-up resistor to $V_P$					
Internal pull-up resistor to $V_P$		$R_O$	5	10	15	k $\Omega$
Output voltage switched on (LOW)	$I_{OL} = 2$ mA	$V_{OL}$	–	–	0.4	V
Maximum output sink current		$I_{OL}$	2	5	–	mA
Leakage current output switched off		$-I_{leak}$	–	–	25	$\mu$ A
<b>Port P1 (pin 11)</b>						
	open npn emitter output					
Output current switched on	$V_O = 0$ to 5 V	$I_O$	14	–	–	mA
Leakage current switched off	$V_O = 0$ to $V_P$ note 2	$\pm I_{leak}$	–	–	100	$\mu$ A
<b>Digital-to-analogue outputs</b>						
<b>DAC0 (pin 16)</b>						
Maximum output voltage	unloaded; note 3	$V_{O\ max}$	3.0	–	4.25	V
Minimum output voltage	unloaded; note 3	$V_{O\ min}$	0.15	–	1.0	V
Positive value of smallest step	$I_O = 2$ mA (1 lsb); note 3	$V_{O\ lsb}$	16	–	72	mV
Deviation from linearity	$I_O = 2$ mA	$\Delta V$	–	–	45	mV
Output impedance	$I_O = -2$ to +2 mA	$Z_O$	–	–	30	$\Omega$
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		$I_{OL}$	2	8	–	mA
<b>DAC1 (pin 1)</b>						
Maximum output voltage	unloaded; note 3	$V_{O\ max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\ min}$	1.0	–	1.7	V
Positive value of smallest step	$I_O = 2$ mA (1 lsb); note 3	$V_{O\ lsb}$	18	–	86	mV
Deviation from linearity	$I_O = 2$ mA	$\Delta V$	–	–	50	mV
Output impedance	$I_O = -2$ to +2 mA	$Z_O$	–	–	30	$\Omega$
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		$I_{OL}$	2	8	–	mA

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>DAC2 (pin 2)</b>						
Maximum output voltage	unloaded; note 3	$V_{O\ max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\ min}$	1.0	–	1.7	V
Positive value of smallest step	$I_O = 2\ \text{mA}$ (1 lsb); note 3	$V_{O\ lsb}$	18	–	86	mV
Deviation from linearity	$I_O = 2\ \text{mA}$	$\Delta V$	–	–	50	mV
Output impedance	$I_O = -2\ \text{to}\ +2\ \text{mA}$	$Z_O$	–	–	30	$\Omega$
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		$I_{OL}$	2	8	–	mA
<b>DAC3 (pin 3)</b>						
Maximum output voltage	unloaded; note 3	$V_{O\ max}$	10.0	–	11.2	V
Minimum output voltage	unloaded; note 3	$V_{O\ min}$	0.1	–	1.0	V
Positive value of smallest step	$I_O = 2\ \text{mA}$ (1 lsb); note 3	$V_{O\ lsb}$	70	–	250	mV
Deviation from linearity	$I_O = 2\ \text{mA}$	$\Delta V$	–	–	150	mV
Output impedance	$I_O = -2\ \text{to}\ +2\ \text{mA}$	$Z_O$	–	–	30	$\Omega$
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		$I_{OL}$	2	8	–	mA
<b>Power-down reset</b>						
Maximum value of $V_P$ at which power-down reset is active		$V_{PD}$	6	–	10	V
Rise time of $V_P$ during power-on	$V_P$ rising from 0 V to $V_{PD}$	$t_r$	5	–	–	$\mu\text{s}$

**Notes to the Characteristics**

1. If  $V_P < 1\ \text{V}$ , the input current is limited to 10  $\mu\text{A}$  at input voltages up to 13.2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to  $V_P$ .

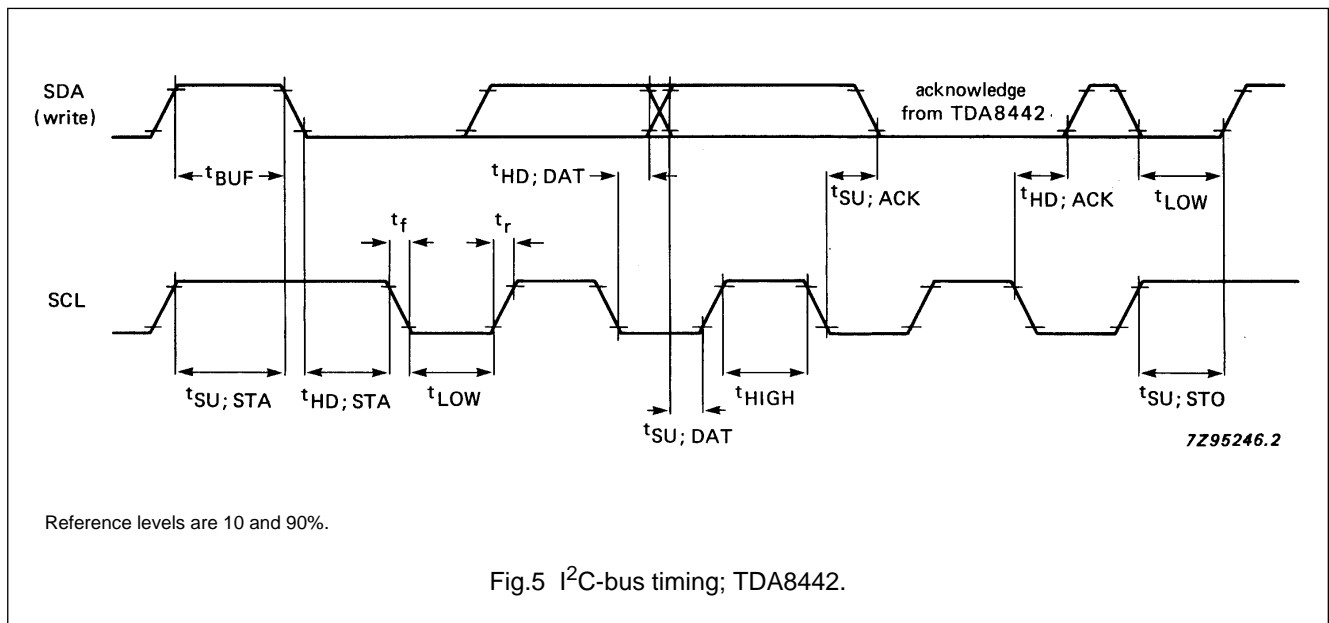
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## I<sup>2</sup>C-BUS TIMING

Bus loading conditions: 4kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.  
 All values are referred to V<sub>IH</sub> = 3 V and V<sub>IL</sub> = 1.5 V.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Bus free before start	t <sub>BUF</sub>	4.0	–	–	μs
Start condition set-up time	t <sub>SU; STA</sub>	4.0	–	–	μs
Start condition hold time	t <sub>HD; STA</sub>	4.0	–	–	μs
LOW period SCL, SDA	t <sub>LOW</sub>	4.0	–	–	μs
HIGH period SCL	t <sub>HIGH</sub>	4.0	–	–	μs
Rise time SCL, SDA	t <sub>r</sub>	–	–	1.0	μs
Fall time SCL, SDA	t <sub>f</sub>	–	–	0.30	μs
Data set-up time (write)	t <sub>SU; DAT</sub>	1	–	–	μs
Data hold time (write)	t <sub>HD; DAT</sub>	1	–	–	μs
Acknowledge (from TDA8442) set-up time	t <sub>SU; ACK</sub>	–	–	3.5	μs
Acknowledge (from TDA8442) hold time	t <sub>HD; ACK</sub>	0	–	–	μs
Stop condition set-up time	t <sub>SU; STO</sub>	4.0	–	–	μs





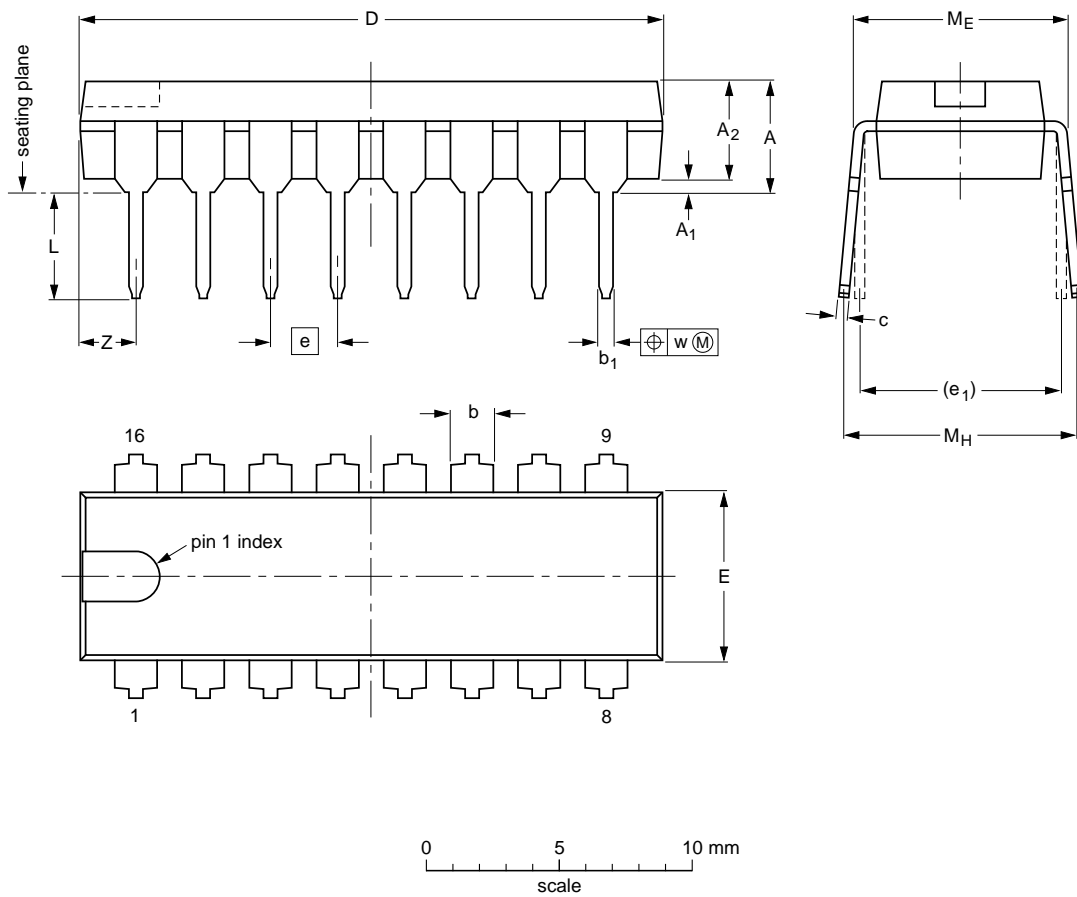
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PACKAGE OUTLINE

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				92-10-02 95-01-19

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

### LIFE SUPPORT APPLICATIONS

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