

SANYO

No.2403

LA7300M

Monolithic Linear IC

VHS VTR PLAYBACK HEAD AMP, RECORDING AMP

Functions

- . 3-channel playback head amp
- . Single-channel recording amp
- . PB: One head select switch, two mode select switches
- . REC: Two head select switches

Features

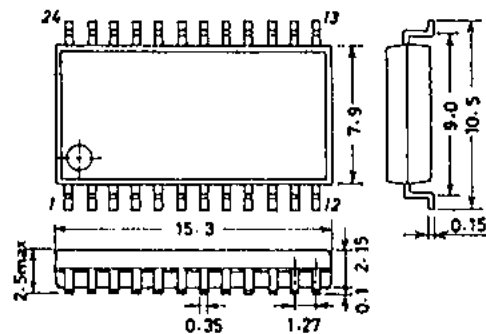
- . No more than one IC required for 3-head/2-head use
- . On-chip driver transistor permitting direct recording
- . On-chip head select switches (3 types) facilitating the pattern design of a set

Maximum Ratings at Ta=25°C

			unit
Maximum Supply Voltage	V _{CC} max	(PB) 7.0 (REC) 13.5	V
Allowable Power Dissipation	P _d max	480	mW
Operating Temperature	T _{opg}	-10 to +65	°C
Storage Temperature	T _{stg}	-40 to +125	°C

Operating Conditions at Ta=25°C

			unit
Supply Voltage	V _{CC}	(PB) 5.0 (REC) 12.0	V
Operating Voltage Range	V _{CC} ops	(PB) 4.75 to 5.6 (REC) 8.5 to 13.0	V

Case Outline 3045B-M24IC
(unit:mm)

The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass-produced.

The information herein is believed to be accurate and reliable. However, no responsibility is assumed by SANYO for its use, nor for any infringements of patents or other rights of third parties which may result from its use.

These specifications are subject to change without notice.

SANYO ELECTRIC CO., LTD. SEMICONDUCTOR DIVISION
15-13, 6-CHOME, SOTOKANDA, CHIYODA-KU, TOKYO 101 JAPAN

4067TA No.2403-1/3

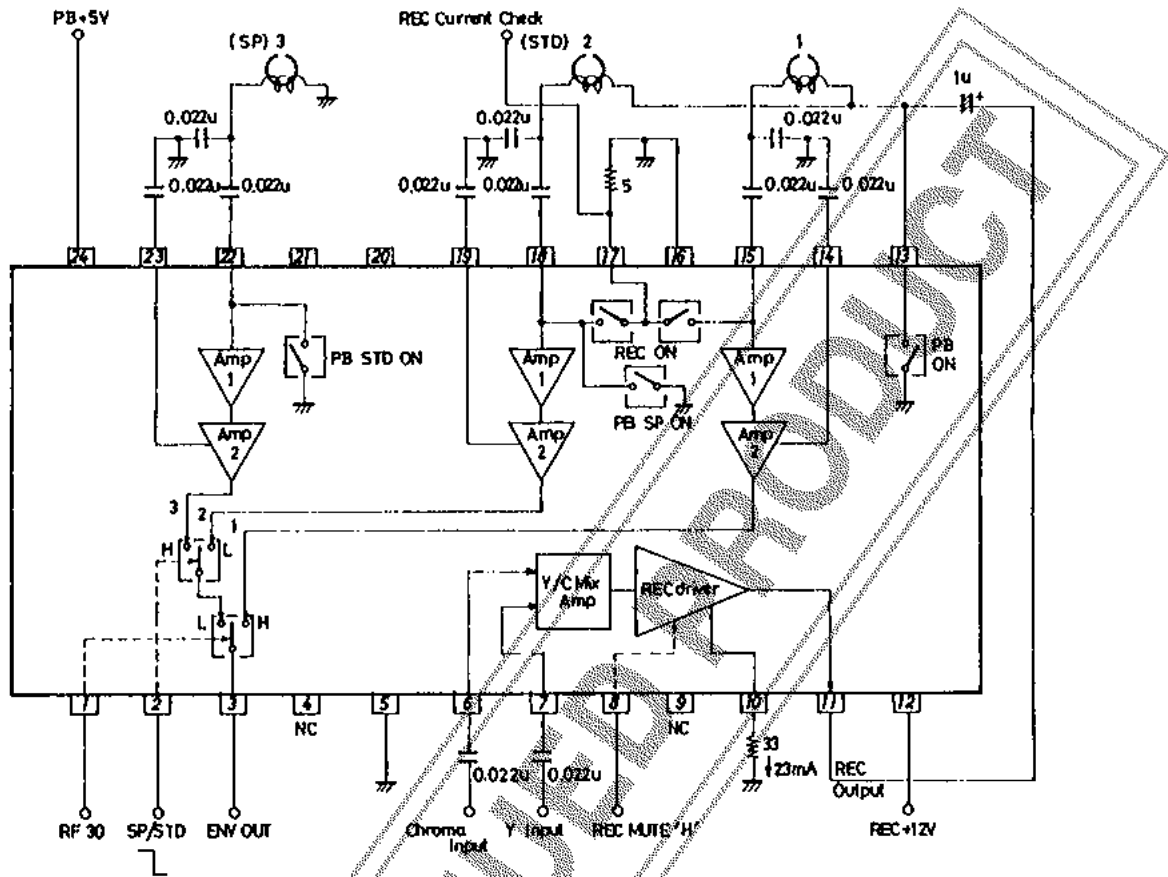
LA7300M

Electrical Characteristics at Ta=25°C

Characteristic	Symbol	Test Conditions		Limits			unit				
		Input	Output	SW1	SW2	SW3		min	typ	max	
(PB mode)		T24		PB+5V	RF	SP/STD	REC				
Current Dissipation	I _{CCP}	T24		Pin24 flow-in current	1	1		12.0	16.0	20.0	mA
Voltage Gain	CH1 2 3 G _{VP} (1) (2) (3)	T15 T18 T22	T3 T3 T3	V _i =38mVpp f=1MHz	1 2 2	1 2 1		56.5	59.5	62.5	dB
Voltage Gain Difference 1	STD ΔG _{VP} (1)			G _{VP} (1)-G _{VP} (2)				-1.0	0	-1.0	dB
Voltage Gain Difference 2	SP ΔG _{VP} (2)			G _{VP} (1)-G _{VP} (3)				-1.0	0	-1.0	dB
Equivalent Input Noise Voltage	CH1 2 3 V _{NIN} (1) (2) (3)		T3 T3 T3	V _{out} G _{VP} (1),(2),(3) after 1.1MHz L.P.F	1 2 2	1 2 1			1.1	1.5	uVrms
Frequency Characteristic	CH1 2 3 ΔV _{FP} (1) (2) (3)	T15 T18 T22	T3 T3 T3	V _i =38mVpp f=100kHz, 7MHz 7M/100K output ratio	1 2 2	1 2 1		-2.5	0		dB
Second Harmonic Distortion	CH1 2 3 V _{HDP} (1) (2) (3)	T15 T18 T22	T3 T3 T3	V _i =38mVpp f=4MHz 8M/4M output ratio	1 2 2	1 2 1			-40	-35	dB
Maximum Output Level	CH1 2 3 V _{OMP} (1) (2) (3)	T15 T18 T22	T3 T3 T3	f=1MHz Output level when 3rd harmonic distortion is -30dB	1 2 2	1 2 1		0.8	1.0		Vpp
Crosstalk 1 STD	CH1 2 V _{CR1} (1) (2)	T18 T15	T3 T3	V _i =38mVpp, f=1MHz V _{out} /G _{VP} (1),(2) output ratio	1 2	1 2			-40	-35	dB
Crosstalk 2 SP	CH1 3 V _{CR2} (1) (3)	T22 T15	T3 T3	V _i =38mVpp, f=1MHz V _{out} /G _{VP} (1),(3) output ratio	1 2	1 1			-40	-35	dB
Output DC Offset 1	ΔV _{ODC1}	-	Pin3	Output DC difference (STD)	1+2	2		-100	0	100	mV
Output DC Offset 2	ΔV _{ODC2}	-	Pin3	Output DC difference (SP)	1+2	1		100	0	100	mV
(REC mode)		T12		REC+12V	RF	SP/STD	REC				
Current Dissipation	I _{CCR}	T12		Pin12 flow-in current			2	25.0	37.0	49.0	mA
Voltage Gain	C Y G _{VR} (C) (Y)	T6 T7	T11 T11	V _i =0.3Vpp f=1MHz			2 2	16.0	19.0	22.0	dB
Voltage Gain Difference	ΔG _{VR}			G _{VR} (C) - (Y)				-1.0	0	1.0	dB
Frequency Characteristic	C Y ΔV _{FR} (C) (Y)	T6 T7	T11 T11	V _i =0.3Vpp, f=1MHz 7MHz			2 2	-1.0	0		dB
Second Harmonic Distortion	C Y V _{HDR} (C) (Y)	T6 T7	T11 T11	V _i =0.3Vpp, f=4MHz 8M/4M output ratio			2 2		-50	-40	dB
Maximum Output Level	C Y V _{OMH} (C) (Y)	T6 T7	T11 T11	f=1MHz Output level when 3rd harmonic distortion is -30dB			2 2	3.5	4.0		Vpp
Mute Attenuation	C Y V _{MR} (C) (Y)	T6 T7	T11 T11	V _i =0.3Vpp, f=1MHz V _{out} /G _{VR} (C) (Y) output ratio			1 1		-60	-50	dB
Cross Modulation Relative Level	V _{CY}	T6 T7	T11 T11	T6 V _i =40mVpp, f=630kHz T7 V _i =0.3Vpp, f=4MHz 4±0.63M 4MHz output ratio			2 2		-50	-40	dB

LA7300M

Block Diagram



Test Circuit

