# SN74LS164

# Serial-In Parallel-Out Shift Register

The SN74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all ON Semiconductor TTL products.

- Typical Shift Frequency of 35 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

**GUARANTEED OPERATING RANGES**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| $T_A$ | Operating Ambient Temperature Range | 0 | 25 | 70 | °C |
| $I_{OH}$ | Output Current – High | | | –0.4 | mA |
| $I_{OL}$ | Output Current – Low | | | 8.0 | mA |

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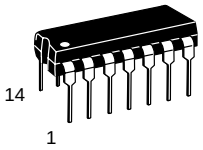
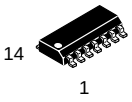
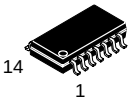
**LOW POWER SCHOTTKY**




**PLASTIC**
**N SUFFIX**
**CASE 646**




**SOIC**
**D SUFFIX**
**CASE 751A**



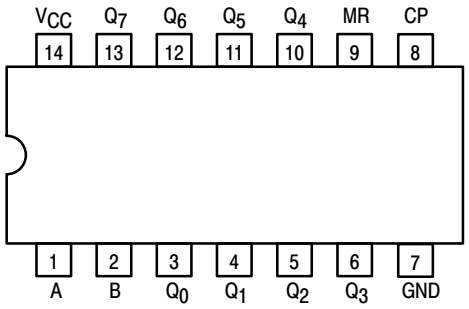

**SOEIAJ**
**M SUFFIX**
**CASE 965**

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| SN74LS164N | 14 Pin DIP | 2000 Units/Box |
| SN74LS164D | SOIC–14 | 55 Units/Rail |
| SN74LS164DR2 | SOIC–14 | 2500/Tape & Reel |
| SN74LS164M | SOEIAJ–14 | See Note 1 |
| SN74LS164MEL | SOEIAJ–14 | See Note 1 |

1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

**CONNECTION DIAGRAM DIP** (TOP VIEW)

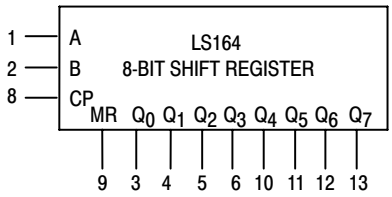



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

| PIN NAMES | | LOADING (Note a) HIGH | LOW |
|---|---|---|---|
| A, B | Data Inputs | 0.5 U.L. | 0.25 U.L. |
| $\overline{CP}$ | Clock (Active HIGH Going Edge) Input | 0.5 U.L. | 0.25 U.L. |
| MR | Master Reset (Active LOW) Input | 0.5 U.L. | 0.25 U.L. |
| $Q_0 - Q_7$ | Outputs | 10 U.L. | 5 U.L. |

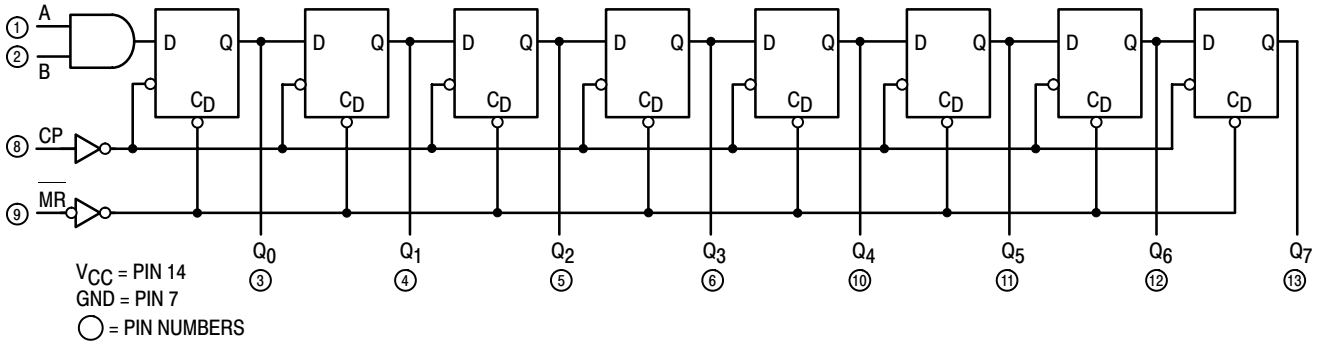
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

**LOGIC SYMBOL**




$V_{CC}$ = PIN 14
GND = PIN 7

## LOGIC DIAGRAM




## FUNCTIONAL DESCRIPTION

The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into $Q_0$ the logical AND of the two data inputs (A•B) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

## MODE SELECT — TRUTH TABLE

| OPERATING MODE | INPUTS | | | OUTPUTS | |
|---|---|---|---|---|---|
| | $\overline{MR}$ | A | B | $Q_0$ | $Q_1$–$Q_7$ |
| Reset (Clear) | L | X | X | L | L – L |
| Shift | H | l | l | L | $q_0$ – $q_6$ |
| | H | l | h | L | $q_0$ – $q_6$ |
| | H | h | l | L | $q_0$ – $q_6$ |
| | H | h | h | H | $q_0$ – $q_6$ |

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
$q_n$ = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| Symbol | Parameter | Limits | | | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs | |
| $V_{IK}$ | Input Clamp Diode Voltage | | –0.65 | –1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = –18 mA | |
| $V_{OH}$ | Output HIGH Voltage | 2.7 | 3.5 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | |
| $V_{OL}$ | Output LOW Voltage | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table |
| | | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA | |
| $I_{IH}$ | Input HIGH Current | | | 20 | μA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V | |
| | | | | 0.1 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | |
| $I_{IL}$ | Input LOW Current | | | –0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | |
| $I_{OS}$ | Short Circuit Current (Note 2) | –20 | | –100 | mA | $V_{CC}$ = MAX | |
| $I_{CC}$ | Power Supply Current | | | 27 | mA | $V_{CC}$ = MAX | |

2. Not more than one output should be shorted at a time, nor for more than 1 second.

**AC CHARACTERISTICS** ($T_A$ = 25°C)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $f_{MAX}$ | Maximum Clock Frequency | 25 | 36 | | MHz | $V_{CC}$ = 5.0 V<br>$C_L$ = 15 pF |
| $t_{PHL}$ | Propagation Delay<br>MR to Output Q | | 24 | 36 | ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Clock to Output Q | | 17<br>21 | 27<br>32 | ns | |

**AC SETUP REQUIREMENTS** ($T_A$ = 25°C)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $t_W$ | CP, $\overline{MR}$ Pulse Width | 20 | | | ns | $V_{CC}$ = 5.0 V |
| $t_s$ | Data Setup Time | 15 | | | ns | |
| $t_h$ | Data Hold Time | 5.0 | | | ns | |
| $t_{rec}$ | $\overline{MR}$ to Clock Recovery Time | 20 | | | ns | |

## AC WAVEFORMS

*The shaded areas indicate when the input is permitted to change for predictable output performance.

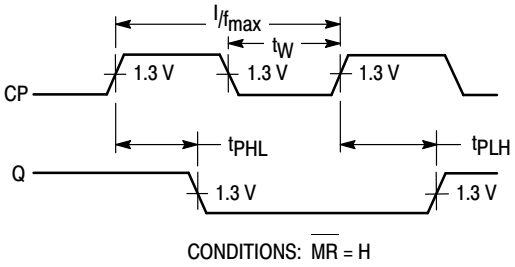



**Figure 1. Clock to Output Delays and Clock Pulse Width**

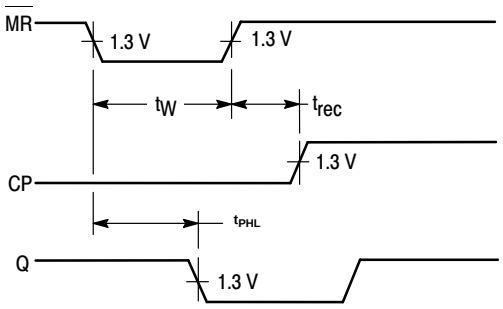



**Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**

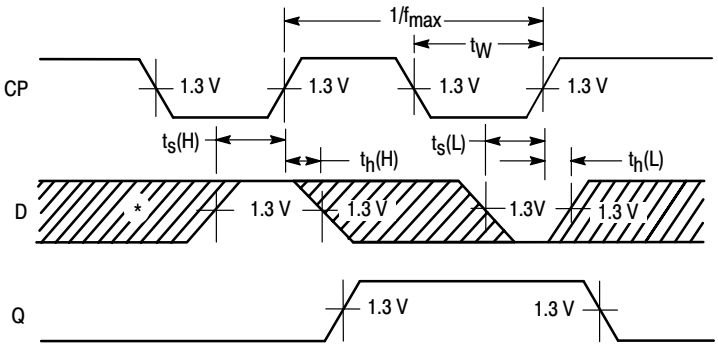
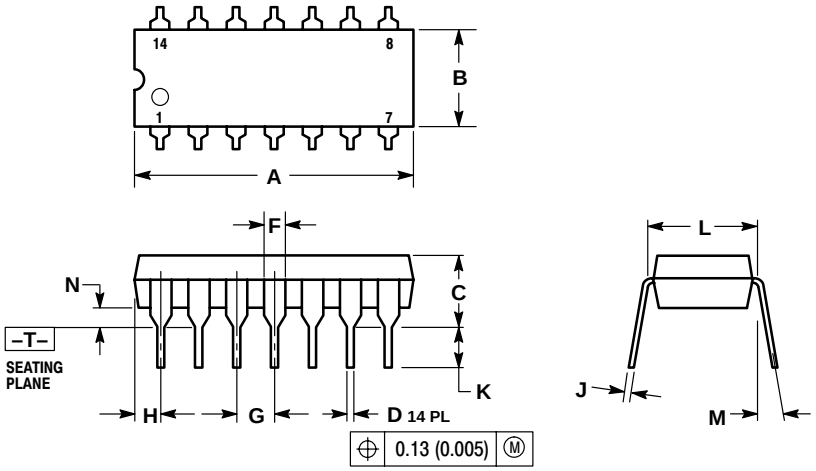



**Figure 3. Data Setup and Hold Times**

## PACKAGE DIMENSIONS

**N SUFFIX**
PLASTIC PACKAGE
CASE 646–06
ISSUE M

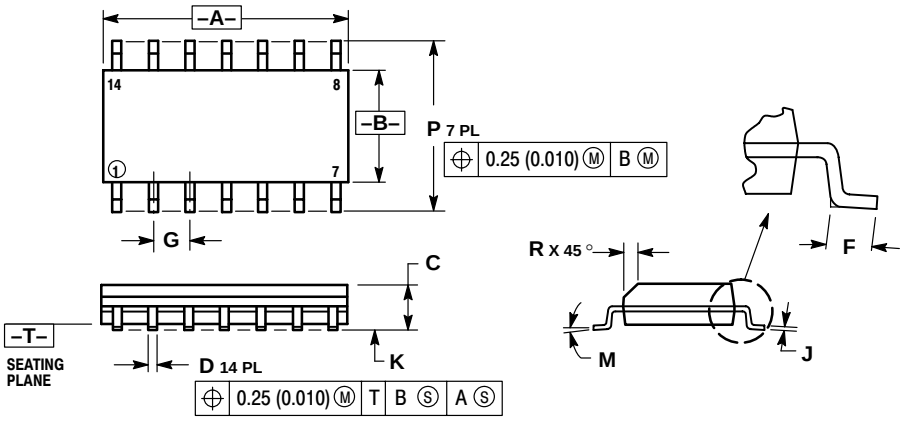



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 18.80 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | --- | 10° | --- | 10° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

## PACKAGE DIMENSIONS

**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F

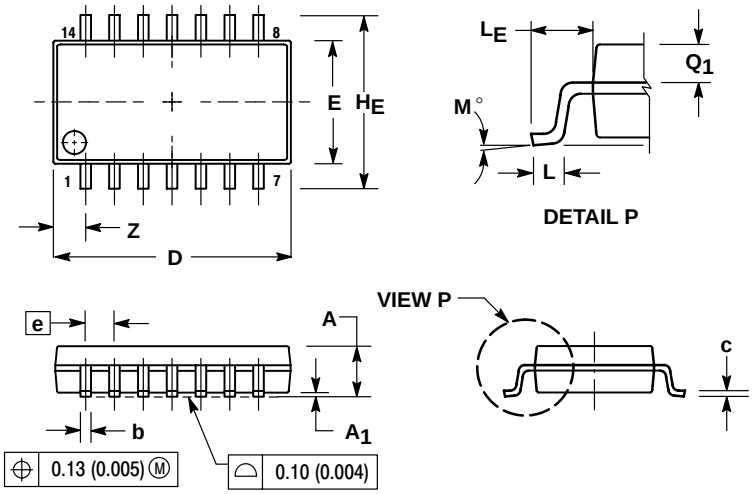



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

## PACKAGE DIMENSIONS

**M SUFFIX**
SOEIAJ PACKAGE
CASE 965–01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| 0.50 | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |



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